



Firing circuits for three-phase power electronic circuits
by Tai-Ming Timmious Lee

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in
Electrical Engineering
Montana State University
© Copyright by Tai-Ming Timmious Lee (1988)

Abstract:

This thesis reports upon the design of three different firing angle controller circuits for controlling three-phase voltages and compares them. These circuits will be used by the students to do controlled experiments in the Power Electronics Laboratory of the Electrical Engineering Department at Montana State University. The three circuits are a phase-shifter-based three-phase voltage controller; a ramp-comparator-based three-phase voltage controller and a phase-locked-loop based three-phase voltage controller. The phase-shifter-based controller is a nonlinear firing angle controller, and the other two controller circuits are linear firing angle controllers. All operate at 60Hz controllers. With the aid of a SPICE simulation, the error of the ramp-comparator circuit has been minimized by means of an error blocking circuit added to block the discharging error of the ramp-comparator circuit. The ramp-comparator-based controller may have different errors for each channel. The phase-locked-loop controller consists of a ramp-comparator circuit and a phase-locked-loop circuit. It has the advantage of equal error per channel, and the error may be reduced by changing the free running frequency of the phase-locked-loop. The firing angle can be controlled linearly by changing the reference voltage of the ramp-comparators. For the phase-locked-loop based voltage controller, the possible range of the firing angle may be from 0° to 180° with much less than 1° error. The theoretical error formulas are derived, and the experimental results of the designed controllers are presented. The application of phase-locked-loop in three-phase inverter design is also discussed in this thesis.

FIRING CIRCUITS FOR THREE-PHASE
POWER ELECTRONIC CIRCUITS

by

Tai-Ming Timmious Lee

A thesis submitted in partial fulfillment
of the requirements for the degree

of

Master of Science

in

Electrical Engineering

MONTANA STATE UNIVERSITY
Bozeman, Montana
November, 1988.

N378
L5154

APPROVAL

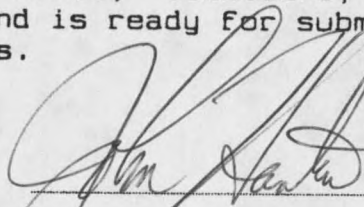
of a thesis submitted by

Tai-Ming Timmious Lee

This thesis has been read by each member of the thesis committee and has been found to be satisfactory regarding content, English usage, format, citations, bibliographic style, and consistency, and is ready for submission to the College of Graduate Studies.

11-28-88

Date

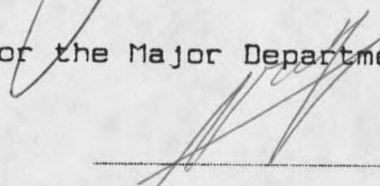


Chairperson, Graduate committee

Approved for the Major Department

11-28-88

Date

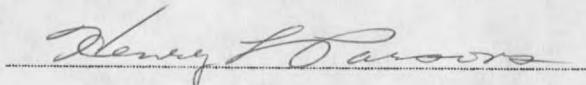


Head, Major Department

Approved for the College of Graduate Studies

12/21/88

Date



Graduate Dean

STATEMENT OF PERMISSION TO USE

In presenting this thesis in partial fulfillment of the requirements for a master's degree at Montana State University, I agree that the Library shall make it available to borrowers under the rules of the Library. Brief quotations from this thesis are allowable without special permission, provided that accurate acknowledgement of sources is made.

Permission for extensive quotations from or reproduction of this thesis may be granted by my major professor, or in his absence, by the Director of Libraries when, in the opinion of either, the proposed use of the material is for the scholarly purpose. Any copying or use of the material in this thesis for financial gain shall not be allowed without my written permission.

Signature

Lee Tai Hing

Date

11/28/88

DEDICATION

I dedicate this thesis as a memorial to my grandfather,
Mr. Ying-Fu Lee.

ACKNOWLEDGEMENTS

The author would like to thank Dr. P. Kalra, Dr. M. Kejariwal and Dr. J. Hanton for their guidance and encouragement with this research. I also wish to thank Dr. D. A. Pierre and Professor N. Shrauger for their help and valuable suggestions. I want to thank Garth Stevens, who was a senior work-study student, for connecting and testing my designs.

Finally the author wishes to thank his grandmother, Madame Kwai-Yee Lok, and his parents for their encouragement.

TABLE OF CONTENTS

	page
LIST OF FIGURES	viii
LIST OF TABLE	xiii
ABSTRACT	xiv
CHAPTER	
1. INTRODUCTION	1
2. PHASE-SHIFTER-BASED FIRING ANGLE CONTROLLER DESIGN	6
Introduction	6
Basic Phase Shifter Circuit	6
Application of Phase Shifter in Firing Circuit Design	8
Phase-Shifter-Based Three-Phase Firing Circuit	10
Application of Phase-Shifter-Based Three-Phase Firing Circuit	13
An Experiment of a Phase-Shifter-Based Three-Phase Voltage Controller (PSBTPVC)	14
Experimental Results of the PSBTPVC	20
Conclusions	26
3. RAMP-COMPARATOR-BASED FIRING CIRCUIT DESIGN	27
Introduction	27
Basic Ramp-Comparator Circuit	28
An Error Blocking Circuit	29
Correction of the Error Due to Saturation of the Transistor	32
Improve Performance of the Ramp Generator by Using a SPICE Simulation	33
Error Analysis of the Ramp-Comparator Circuit	36
Error Analysis of the Pulse Driver Circuit	38
Error Analysis of a Zero Crossing Detector Circuit	39
Experimental Results of a Ramp Generator ...	40

TABLE OF CONTENTS--Continued

	Page
Application of Ramp-Comparator Circuit in Firing Controller	41
An Experiment of a Ramp-Comparator-Based Three-Phase Voltage Controller (RCBTPVC) ..	44
Experimental Results of the RCBTPVC	46
Conclusions	51
 4. PHASE-LOCKED-LOOP-BASED FIRING CONTROLLER	
DESIGN	52
Introduction	52
Basic Phase-Locked Loop	53
Phase-Locked-Loop-Based Firing Controller ...	55
An Experiment of a PLL-Based DC to Three-Phase Inverter (PLLBTPIC)	59
Experimental Results of the PLLBTPIC	62
An Experiment of a PLL-Based Three-Phase Voltage Controller (PLLBTPVC)	64
Conclusions	65
 5. DISCUSSION	67
Comparison of Three Different Controllers ...	67
Comments	68
 6. CONCLUSION	69
Suggested Future Work	71
 REFERENCES CITED	73
 APPENDICES	76
A. Derivation of the Phase Shifter Circuit Transfer Function	77
B. SPICE Program Listing of Ramp Generator Simulation	79
C. Phase-Locked-Loop Circuit Design Using LM565 Chip	80

LIST OF FIGURES

Figure	Page
1. Phase shifter circuit from Le and Berg [1].	7
2. Single operational amplifier phase shifter.	8
3. A block diagram of a single phase phase-shifter-based firing circuit.	9
4. A block diagram of three-phase phase-shifter-based firing circuit.	11
5. A three-phase phase-shifter-based firing circuit.	12
6. A three-phase voltage controller.	13
7. A three-phase bridge inverter.	14
8. The investigated configuration of the experiment.	15
9. The connections of the PSBTPVC.	15
10. A view of the PSBTPVC experiment.	16
11. A view inside the thyristor box.	17
12. A view inside the power supply & time delay box.	17
13. Measured output waveforms of the driver with the thyristor gate and cathod as a load.	18
14. A view inside the PSBTPVC box.	19
15. Measured three-phase output waveforms generated by PSBTPVC.	20
16. Measured waveforms across the load with a balanced load of 25Ω at $\alpha = 90^\circ$ using the PSBTPVC.	21
17. Measured waveforms across the thyristor with a balanced load of 25Ω at $\alpha = 90^\circ$ using the PSBTPVC.	21

LIST OF FIGURES -- Continued

Figure	Page
18. Measured maximum adjustable range of the PSBTPVC.	22
19. Measured waveforms across the resistor with a balanced load of a 25Ω at $\alpha = 180^\circ$ using the PSBTPVC.	22
20. Measured waveforms across the capacitor with a balanced load of a 25Ω resistor and a $30\mu\text{F}$ capacitor connected in series at $\alpha = 90^\circ$ using the PSBTPVC.	23
21. Measured waveforms across the resistor with a balanced load of a 25Ω resistor and a $30\mu\text{F}$ capacitor connected in series at $\alpha = 90^\circ$ using the PSBTPVC.	23
22. Measured waveforms across the resistor with a balanced load of a 25Ω resistor and a $30\mu\text{F}$ capacitor connected in series at $\alpha = 0^\circ$ using the PSBTPVC.	24
23. Measured waveforms across the capacitor with a balanced load of a 25Ω resistor and a $30\mu\text{F}$ capacitor connected in series at $\alpha = 0^\circ$ using the PSBTPVC.	24
24. Measured waveforms across the thyristor with a balanced load of a 25Ω resistor and a $30\mu\text{F}$ capacitor connected in series at $\alpha = 0^\circ$ using the PSBTPVC.	25
25. Measured waveforms across the inductor with a balanced load of a 100Ω resistor and a 98.25mH inductor connected in series at $\alpha = 90^\circ$ using the SBTPVC.	25
26. Measured waveforms across the resistor with a balanced load of a 100Ω resistor and a 98.25mH inductor connected in series at $\alpha = 90^\circ$ using the PSBTPVC.	26
27. A ramp generator.	28
28. A basic ramp-comparator circuit.	29
29. The pulse response of a ramp generator.	30

LIST OF FIGURES -- Continued

Figure	Page
30. A basic error blocking circuit.	31
31. The pulse response of an error blocking circuit.	32
32. The response of a ramp generator with $R = 47K\Omega$. ..	34
33. The response of a ramp generator with $R = 27K\Omega$. ..	35
34. The response of a ramp generator with $R = 1K\Omega$	35
35. The response of a ramp generator with $R = 500\Omega$. ..	36
36. An actual output waveform of the ramp generator.	37
37. A zero crossing detector circuit.	39
38. A block diagram of a three-phase ramp-comparator-based firing controller.	42
39. A three-phase ramp-comparator-based firing circuit.	43
40. The connections of the RCBTPVC.	45
41. Measured three-phase output waveforms generated by the RCBTPVC.	45
42. Measured waveforms across the load with a balanced load of 25Ω at $\alpha = 90^\circ$ using the RCBTPVC.	46
43. Measured waveforms across the thyristor with a balanced load of 25Ω at $\alpha = 90^\circ$ using the RCBTPVC.	46
44. Measured maximum adjustable range of the RCBTPVC.	47
45. Measured waveforms across the capacitor with a balanced load of a 25Ω resistor and a $30\mu F$ capacitor connected in series at $\alpha = 90^\circ$ using the RCBTPVC.	47

LIST OF FIGURES -- Continued

Figure	Page
46. Measured waveforms across the resistor with a balanced load of 25Ω resistor and a $30\mu\text{F}$ capacitor connected in series at $\alpha = 90^\circ$ using the RCBTPVC.	48
47. Measured waveforms across the resistor with a balanced load of a 25Ω resistor and a $30\mu\text{F}$ capacitor connected in series at $\alpha = 0^\circ$ using the RCBTPVC.	48
48. Measured waveforms across the capacitor with a balanced load of a 25Ω resistor and a $30\mu\text{F}$ capacitor connected in series at $\alpha = 0^\circ$ using the RCBTPVC.	49
49. Measured waveforms across the thyristor with a balanced load of a 25Ω resistor and a $30\mu\text{F}$ capacitor connected in series at $\alpha = 0^\circ$ using the RCBTPVC.	49
50. Measured waveforms across the inductor with a balanced load of a 100Ω resistor and a 98.25mH inductor connected in series at $\alpha = 90^\circ$ using the RCBTPVC.	50
51. Measured waveforms across the resistor with a balanced load of a 100Ω resistor and a 98.25mH inductor connected in series at $\alpha = 90^\circ$ using the RCBTPVC.	50
52. A block diagram of equidistant pulse scheme.	53
53. A divide-by-six module.	54
54. The timing diagram of the divide-by-six module.	54
55. Phase shift versus frequency plot of a LM565.	56
56. A block diagram of a three-phase phase-locked-loop-based firing controller.	57
57. A three-phase phase-locked-loop-based firing circuit.	58
58. Measured three-phase output waveforms generated by the PLLBTPIIC.	60

LIST OF FIGURES -- Continued

Figure	Page
59. Measured the driver input signals of the PLLBTIC : G1, G2 and G3.	61
60. Measured the driver input signals of the PLLBTIC : G4, G5 and G6.	61
61. Measured the operation of the error blocking circuit.	62
62. Measured waveforms across phase AB with a balanced load of 130 Ω using the PLLBTIC.	63
63. Measured waveforms across AN with a balanced load of 130 Ω using the PLLBTIC.	63
64. Measured waveforms across the load with a balanced load of 25 Ω at $\alpha = 180^\circ$ using the PLLBTIC.	65
65. A phase shifter circuit.	77
66. SPICE program listing of ramp generator simulation.	79
67. A LM565 phase-locked-loop circuit.	80

LIST OF TABLES

Table	Page
1. Experimental data of ramp comparators.	41
2. The comparison of three different controllers. ...	67

ABSTRACT

This thesis reports upon the design of three different firing angle controller circuits for controlling three-phase voltages and compares them. These circuits will be used by the students to do controlled experiments in the Power Electronics Laboratory of the Electrical Engineering Department at Montana State University. The three circuits are a phase-shifter-based three-phase voltage controller; a ramp-comparator-based three-phase voltage controller and a phase-locked-loop based three-phase voltage controller. The phase-shifter-based controller is a nonlinear firing angle controller, and the other two controller circuits are linear firing angle controllers. All operate at 60Hz controllers. With the aid of a SPICE simulation, the error of the ramp-comparator circuit has been minimized by means of an error blocking circuit added to block the discharging error of the ramp-comparator circuit. The ramp-comparator-based controller may have different errors for each channel. The phase-locked-loop controller consists of a ramp-comparator circuit and a phase-locked-loop circuit. It has the advantage of equal error per channel, and the error may be reduced by changing the free running frequency of the phase-locked-loop. The firing angle can be controlled linearly by changing the reference voltage of the ramp-comparators. For the phase-locked-loop based voltage controller, the possible range of the firing angle may be from 0° to 180° with much less than 1° error. The theoretical error formulas are derived, and the experimental results of the designed controllers are presented. The application of phase-locked-loop in three-phase inverter design is also discussed in this thesis.

CHAPTER 1

INTRODUCTION

What does research mean ?
When one cannot invent, one must at
least improve.

- Fortune Cookie -

What does design mean ?
Design has no fixed form like water.
It depends on the practical situation
and the economical constraint.

- Timmious Lee -

Most of the fundamental ideas of science
are essentially simple, and may, as a
rule, be expressed in a language
comprehensible to everyone.

- Albert Einstein -

If you cannot—in the long run—tell
everyone what you have been doing, your
doing has been worthless.

- Erwin Schrödinger -

This thesis presents a discussion of the design and development of the firing circuits for the Power Electronics Laboratory of the Electrical Engineering Department at Montana State University. The Power Electronics Laboratory will provide the facilities for power electronics classes and for those who work on power electronics related research. The power electronics related research and classes at Montana State University involve mainly thyristorized systems such as three-phase AC to DC converters, AC voltage controllers (single phase and three-

phase), DC to AC inverters, as well as simulations of those systems. Therefore, it is necessary to have a highly accurate and reliable firing controller for the thyristorized systems so that the students can conduct experiments in the Power Electronics Laboratory. Those who work on the simulations of the power electronic system can compare the exact experimental data with the simulated results. The firing circuits are designed mainly for educational purposes. Therefore, low cost, easy maintainability and linear firing angle control are the basic criteria of the designs. None of the designs in the current published papers to the author's knowledge have the capability to display and generate precise firing angles.

Several different approaches have been implemented [1-9]. However, all of them may not meet the above criteria. The main disadvantages of the circuit proposed by Le and Berg [1] are the non-linear response caused by the phase shifter and the complexity of the circuit. The phase shifter circuits suggested by Le and Berg [1] can be simplified to reduce the number of components. Even though the circuit uses non-linear control of the firing angle, it is worthwhile to have this circuit in the Power Electronics Laboratory in order to acquaint students with the operation of the phase shifter circuit and its advantages and disadvantages. The discussion of designing a phase-shifter-based three-phase firing angle controller is presented in

Chapter 2. The circuits proposed by Ilango, Krishnan, Subramanian and Sadasivan [2] and Simard and Rajagopalan [6] may cause nonlinearity in controlling the firing angle. The major disadvantages of the circuit proposed by Arockiasamy and Doraipandy [3] are :

- 1) A separate discharge circuit is needed.
- 2) Stabilized power supplies with $+V_{cc}$ and $-V_{cc}$ are required.
- 3) Because of the inherent finite rise time, the maximum frequency of operation is restricted.
- 4) It is difficult to control a three-phase rectifier bridge because of the tolerances of the components.
- 5) The circuit is very sensitive to the temperature.

The problems of the proposed circuit by Tang, Lu and Wu [4] are the cost and difficulty of maintenance. In addition to the disadvantages of [4], the circuit proposed by Mirbod and El-amawy [5] is very slow to respond, and it takes 200ms to track and lock on the input frequency. It is slower than one cycle. The fastest response of a phase-locked loop is to lock on the input frequency during the next cycle. A low order of linearity is the shortcoming of the circuit in Krishnan and Ramaswami [7]. The scheme proposed by Westinghouse [8] may be suitable only for a single phase firing circuit, and it is also not linear. In Sugandhi and Sugandhi [9] two different approaches, namely the ramp-comparator method and the relaxation oscillator

method employing a UJT (unijunction transistor), are discussed. The main problem of the ramp-comparator method is that it has error terms due to the discharge of the charged capacitor. The major shortcoming of the relaxation oscillator method is that the total range of the control is only around 150° .

The error terms of the ramp-comparator method may be corrected by adding an error term blocking circuit. Therefore, the ramp-comparator method should be one of the best ways to control the firing angle linearly. The temperature dependence problem can be minimized by using a constant current source integrated circuit chip. The firing angle can be indicated directly on the digital voltmeter (DVM) by adding a subtractor to subtract the saturation voltage of the transistor. The discussion of designing a ramp-comparator-based three-phase firing angle controller is presented in Chapter 3. This circuit is designed for controlling single phase or three-phase output voltages. It can be used for controlling a DC to three-phase inverter. The phase-shifter-based three-phase firing circuit also has the same functions. By employing the combination of the ramp-comparartor circuit and the phase-locked loop (PLL) circuit, the circuit in Chapter 3 can be simplified. A PLL based firing circuit has the advantage of equidistant pulse firing. It can be used to control an AC to DC converter and a DC to three-phase inverter or a three-phase voltage

controller by changing the conduction angle of the thyristors. The discussion of designing a PLL-based firing angle controller is presented in Chapter 4. The discussion and the conclusion of this thesis are presented in Chapter 5 and Chapter 6 respectively.

CHAPTER 2

PHASE-SHIFTER-BASED FIRING ANGLE CONTROLLER DESIGN

Introduction

This chapter is devoted to the study of the phase-shifter-based firing circuit for naturally commutated power electronic circuits, e.g. an AC voltage controller, a rectifier bridge and an inverter. The concept to develop the firing scheme has been reported in Le and Berg [1]. However, the circuit reported in Le and Berg [1] has component redundancy which makes the circuit cost ineffective. An attempt has been made to reduce the number of components needed to realize the circuit. It is shown that the same characteristics can be obtained for the circuit with a reduced number of components. Further, the complete design procedure of the phase-shifter firing circuit is reported. The experimental results are also reported to verify the validity of the circuit.

Basic Phase Shifter Circuit

A phase shifter is one of the most economical ways to control the firing angle of a three-phase thyristor bridge. In the paper by Le and Berg [1], the phase shifter is implemented by using three operational amplifiers. The original phase shifter of the paper is shown in Figure 1.

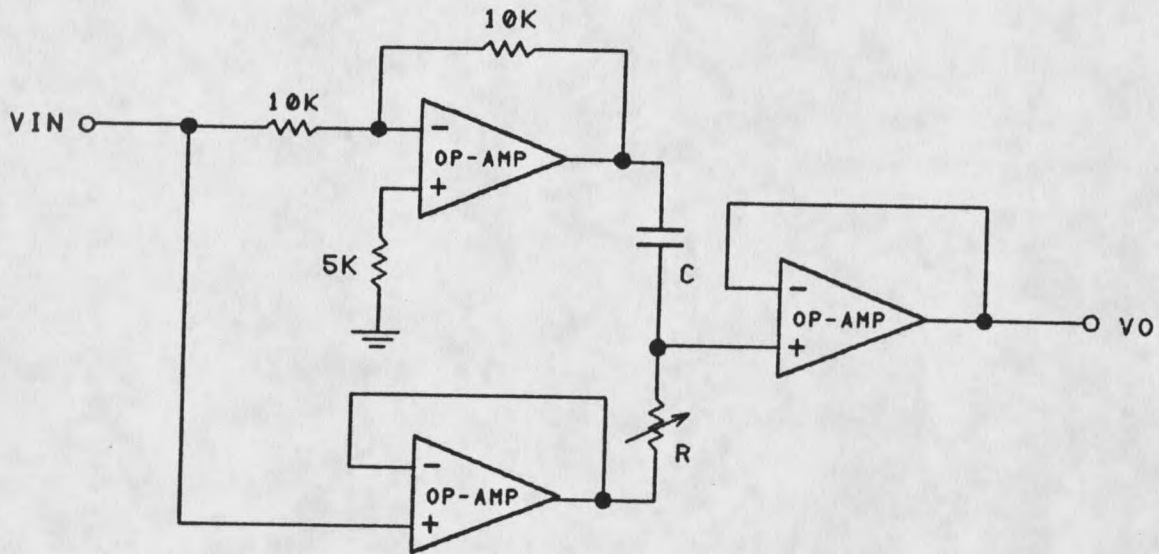


Figure 1. Phase shifter circuit from [1].

The phase shifter circuit has a gain of 1 and the phase angle θ of circuit can be written

$$\theta = -2 \arctan (\omega CR) \quad (2.1)$$

where ω is the input frequency in radians per second. The three operational amplifiers may be replaced by a single operational amplifier with exactly the same gain as well as the same phase shift function. The derivations of the gain and the phase shift function are shown in Appendix A. The phase shifter using one operational amplifier is shown in Figure 2. In equation (2.1), the phase angle θ will be zero if ωCR is equal to zero and the phase angle θ will approach -180° if ωCR approaches infinity. With a variable resistor of $1M\Omega$ and a capacitor of $1\mu F$, the phase angle θ can be

adjusted from 0° to -179.7° at 60Hz (377radians/sec).

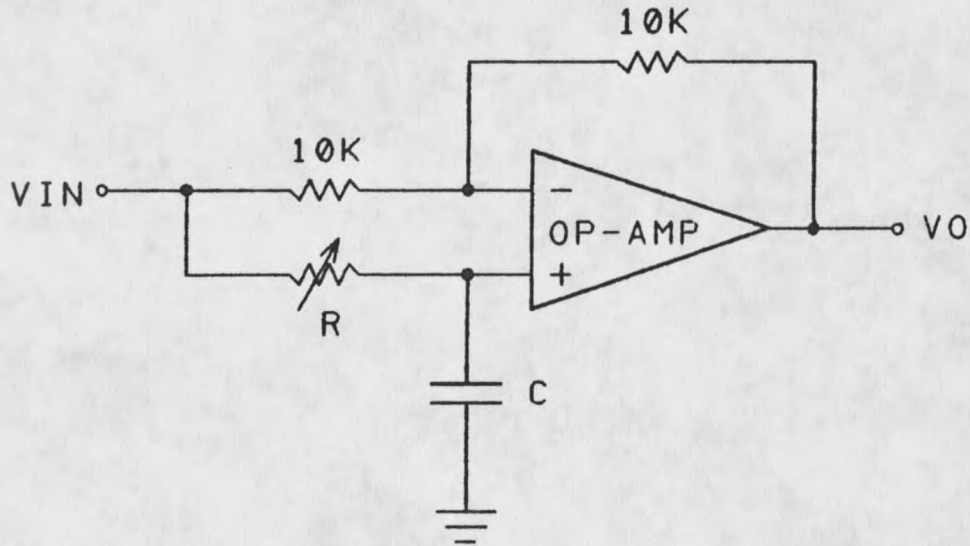


Figure 2. Single operational amplifier phase shifter

Application of Phase Shifter in Firing Circuit Design

Figure 3 shows a block diagram of a single phase control scheme which employs a phase shifter. In Figure 3 after the phase shifter circuit receives the input signal, it generates an output signal with a lagging phase angle as discussed in the previous section. This signal passes through a zero crossing detector stage where the sine wave is converted into a square wave. The square wave output signal is modulated by a 20kHz pulse signal using a two-input AND gate. After receiving the signal from the AND gate, the pulse driver drives a pulse transformer. The output signal of the pulse transformer is rectified and the rectified signal is used to trigger the thyristor with the

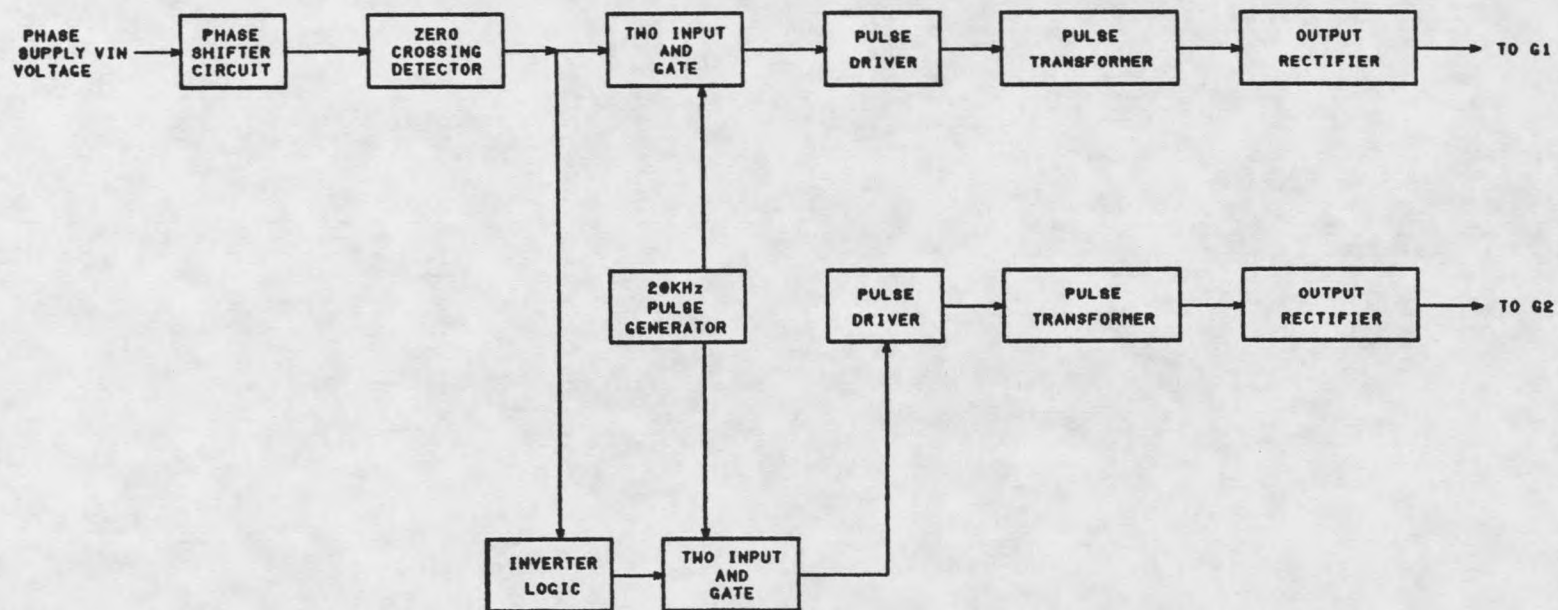
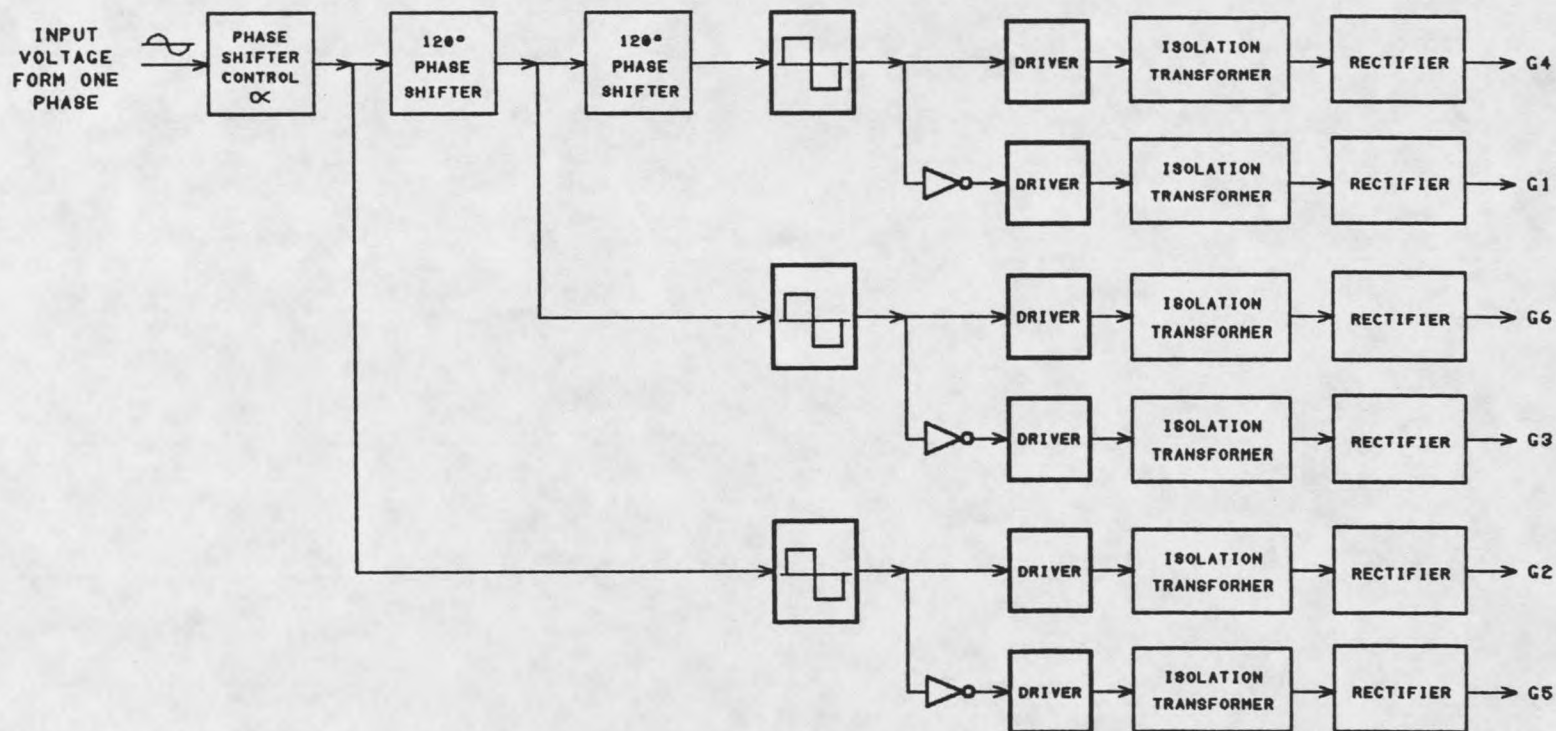


Figure 3. A block diagram of a single phase phase-shifter-based firing circuit.

firing angle range from 0° to 180° . In order to obtain the firing angle from 180° to 360° , an inverter is added to the output of the zero crossing detector; then the signal processing circuit is just like the one mentioned previously. The purpose of the pulse transformer is to isolate the pulse signals of the firing circuit because the pulse triggering signals of the firing circuit cannot have a common ground. Otherwise, the thyristorized control system may be damaged. The function of the pulse output signal, modulated by 20kHz, is to reduce the losses of the pulse transformer. The pulse transformer cannot be used in a low frequency application. How low the frequency can be is determined by the magnetic material of the pulse transformer. The lowest operating frequency of the commercial types of pulse transformers is typically 4kHz. The rectifier circuit is used to prevent the gate of the thyristor from mis-firing and to protect the pulse driver circuit in case the thyristor is damaged.

Phase-Shifter-Based Three-Phase Firing Circuit

Figure 4 shows a block diagram of a phase-shifter-based three-phase firing circuit. Three phase-shifters are employed in the circuit. One of them is used to control the firing angle, and each of the others generates a 120° phase shift. In other words, the circuit acts as a three-phase generator. If the firing angle is adjusted, the output of each pulse circuit will trigger the thyristor



11

Figure 4. A block diagram of a three-phase phase-shifter-based firing circuit.

R39 : ADJUST TO THE DESIRED α .
 R40 : ADJUST TO 120° PHASE SHIFT.
 R41 : ADJUST TO 120° PHASE SHIFT.
 R42,R43 : ADJUST TO DESIRED FREQUENCY AND DUTY CYCLE.

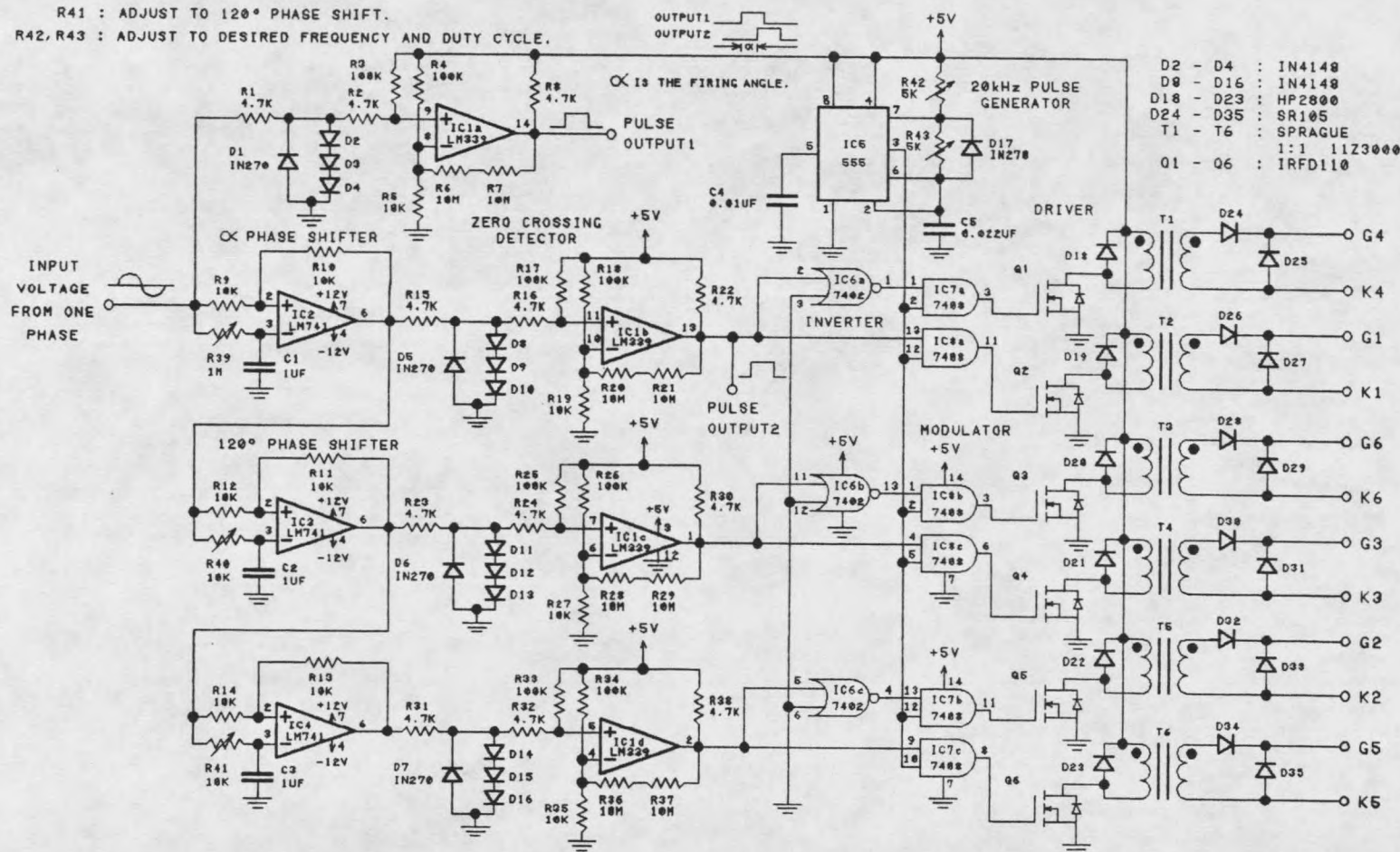


Figure 5. A three-phase phase-shifter-based firing circuit.

with the same adjusted firing angle. Figure 5 is the implementation of the block diagram given in Figure 4.

Application of Phase-Shifter-Based
Three-Phase Firing Circuit

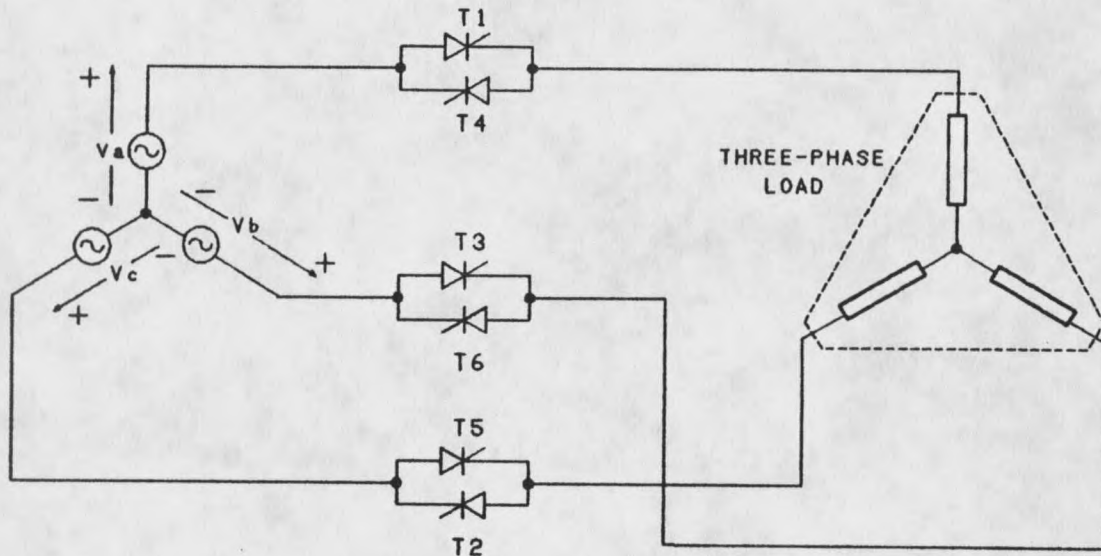


Figure 6. Three-phase voltage controller.

Figure 6 shows the schematic of a three-phase voltage controller. The controller can be used to control a three-phase load such as a three-phase resistive load and a three-phase induction motor. The controller can work as an electronic starter to control the inrush current of an induction machine. If the firing angle is reduced gradually from 180° to 0° , the conduction angle of the thyristors will be increased gradually from 0° to 180° . As a result, the induction motor can be speeded up gradually. By the same token, the speed of the induction motor can be

controlled by adjusting the firing angle of the thyristors.

The phase-shifter-based three-phase firing circuit can also be used to control a three-phase bridge inverter [10] as shown in Figure 7.

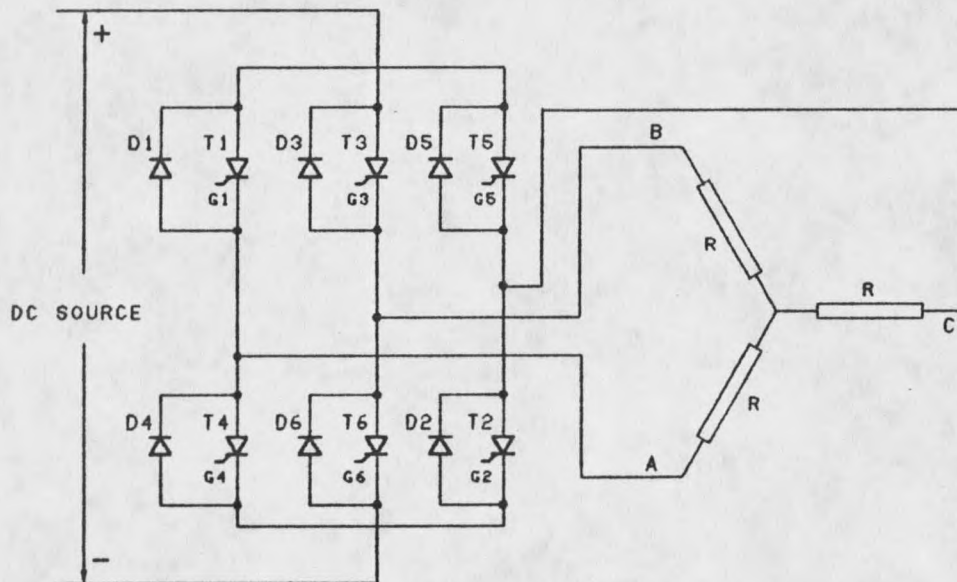


Figure 7. Three-phase bridge inverter.

An Experiment of a Phase-Shifter-Based Three-Phase Voltage Controller (PSBTPVC)

The configuration of the experiment is shown in Figure 8, and the connections of the controller are shown in Figure 9. Figure 10 is a photograph of the experiment in the Power Electronics Laboratory. Six of the 219DLV's are housed in the thyristor box as shown in Figure 11. The 219DLV is a high power, high current and high voltage thyristor. The author could not determine the specifications of the 219DLV thyristor because there is no test equipment available

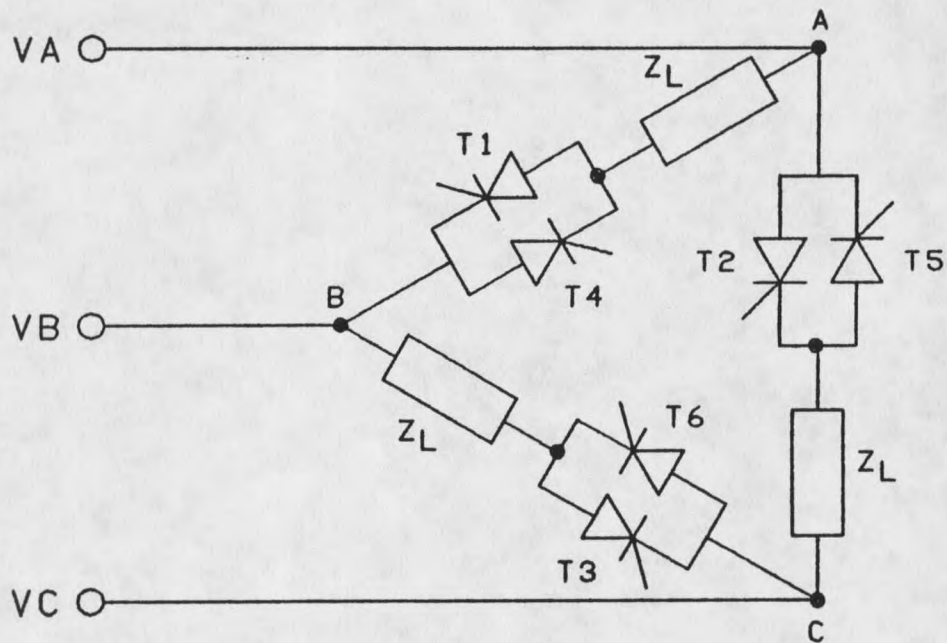


Figure 8. The investigated configuration of the experiment.

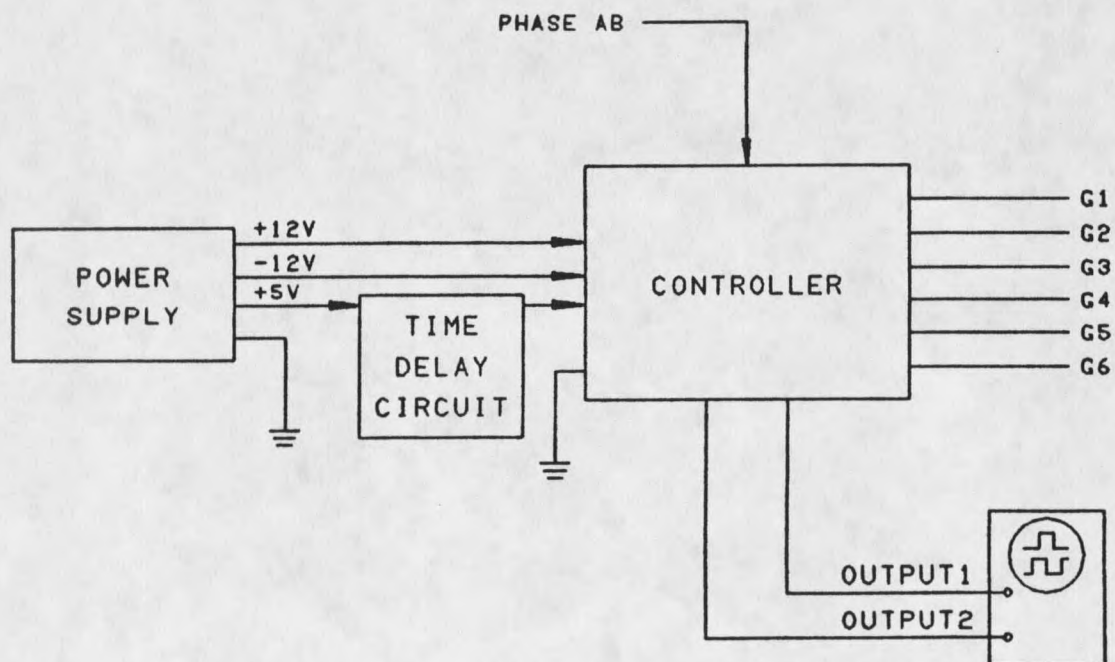


Figure 9. The connections of the PSBIPVC.

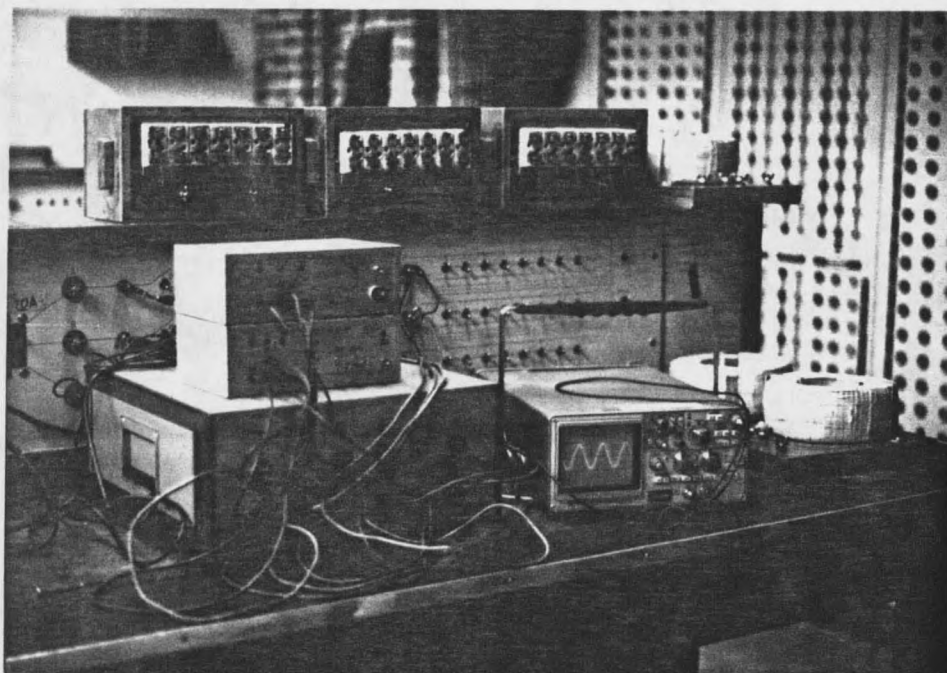


Figure 10. A view of the PSBTIPVC experiment.

which can be used to test the thyristors in the author's laboratory. Based on its size, we estimate that it should handle 100A or more. There are two fans in the box. One is used to inject the air into the box, and the other is used to draw the air out of the box. Six LEDs indicate the status of the six thyristor separately. If a fuse (20A) is blown, the corresponding thyristor's LED will light and the user will know which fuse has blown. Therefore, it saves time to check the fuses. Figure 30 shows the power supply & time delay box. The purpose of the time delay circuit is to avoid misfiring due to the transient response in turning on the power. The power supply has three supply

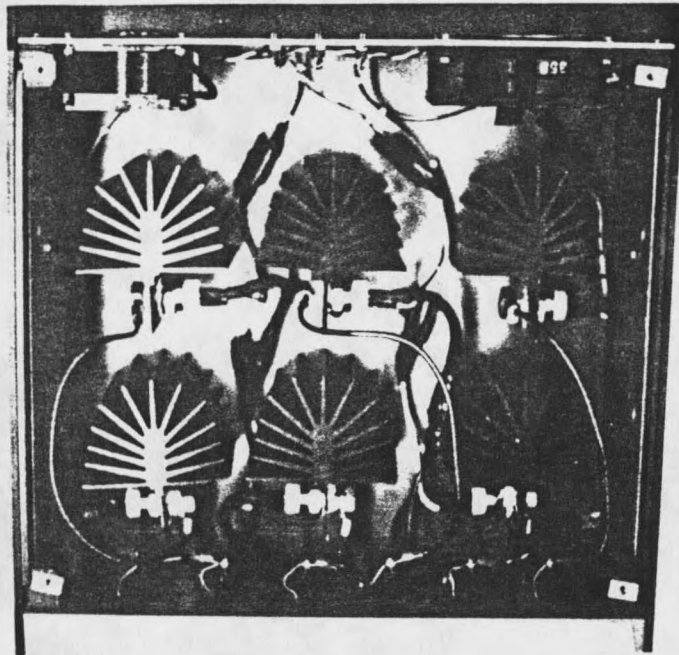


Figure 11. A view inside the thyristor box.

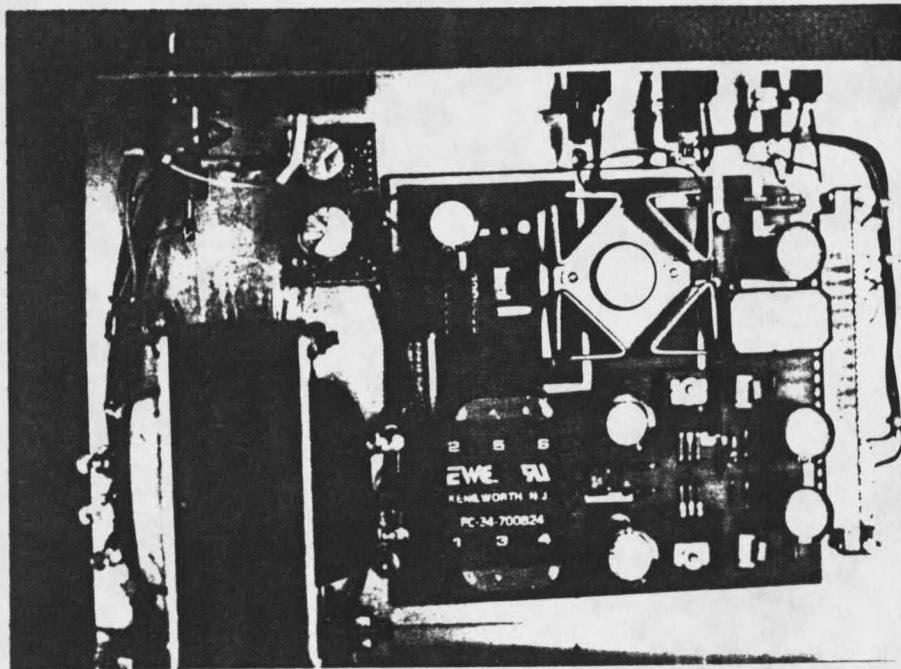


Figure 12. A view inside the power supply & time delay box.

voltages, 5V at 3A, $\pm 12\text{V}$ at 150mA. The time delay circuitry which is used to control the +5V supply can be adjusted from about 0.1 second to 5 second. The +5V supply can be adjusted to 7.2V and the $\pm 12\text{V}$ supply can be adjusted to about $\pm 22\text{V}$. The 5V supply was adjusted to 5.25V and the controller worked well with different power thyristors during the experiment. The typical output voltages of the pulse driver are 3.5V at 0.1A and 1.7V at 0.3A. The modulated frequency of the driver circuit is controlled by a 555 timer chip. The percentage of the duty cycle and the frequency of the modulated frequency can be adjusted by means of two 5k Ω trimmers. The waveforms of the modulated

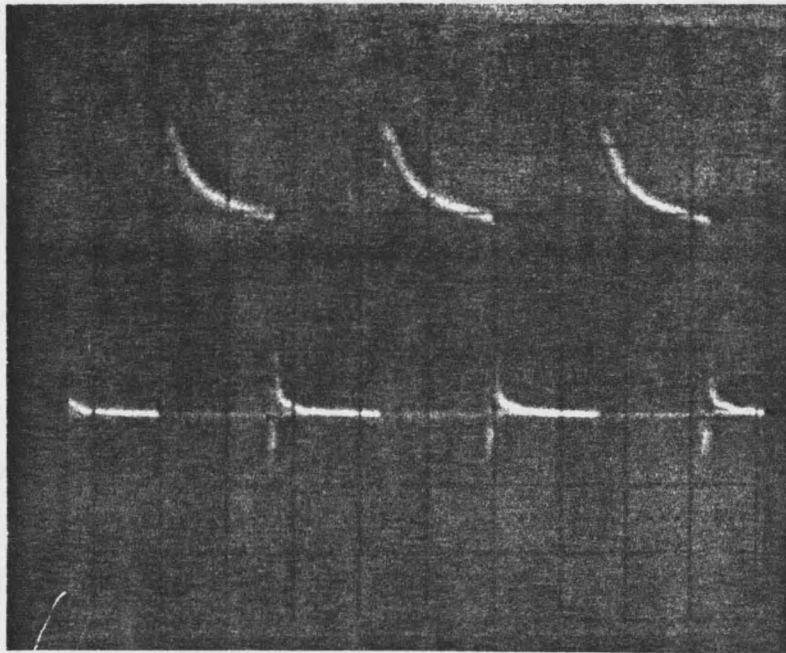


Figure 13. Measured output waveforms of the driver with the thyristor gate and cathode as a load.
Vertical : 0.5V/div. Horizontal : 10 μs /div.

frequency at 30kHz is shown in Figure 13. A picture of the assembled PSBTIPVC is shown in Figure 14. The calibration of the PSBTIPVC is performed by using a dual channel oscilloscope with a ground-isolated connector connected to the plug of the power cord of the oscilloscope. A standard experimental breadboard is used for the power supply of the PSBTIPVC because the plug of the power cord of the breadboard has two terminals, and the power supply and time delay box has a polarized plug. The phase-shifter can be adjusted to 120° and 240° by comparing the phase of the three-phase voltage lines. The PSBTIPVC was fully calibrated. The generated three-phase waveforms are shown in Figure 15.

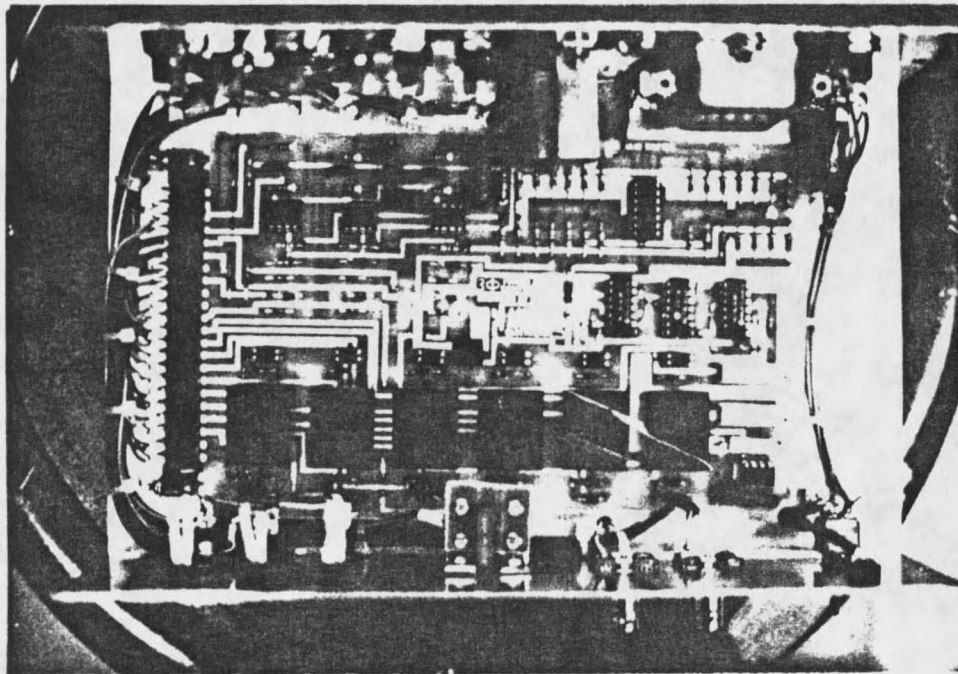


Figure 14. A view inside the PSBTIPVC box.

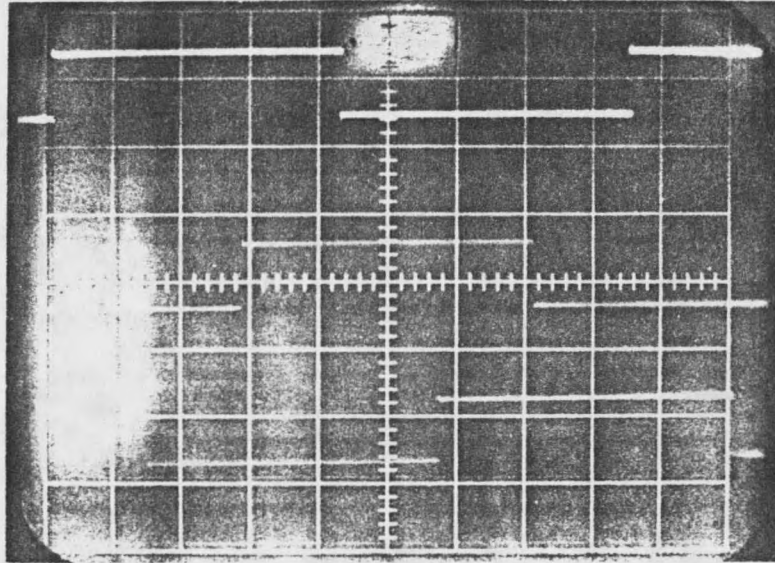


Figure 15. Measured three-phase output waveforms generated by PSBTPVC. Upper : 0° . Middle : 120° . Bottom : 240° .
Vertical : 5V/div. Horizontal : 2ms/div.

Experimental Results of the PSBTPVC

Figures 16 to 26 show the responses of the load and the thyristor with different loads and different firing angles. Figure 19 shows the maximum adjustable firing angle of the controller. The measured range of the firing angle was from 0° to 174.88° . The author used the SPICE model of the LM741 and ran the SPICE program. The SPICE result at 60Hz was exactly the same as the calculated value but the experimental result was not. The experimental phase-shifting circuit designed by Le and Berg [1] permitted a maximum phase shift of 171.22° at 60Hz. According to the experimental results, each of LM13741C, LF356C AND TL071C had a maximum phase shift of 1° or 2° higher than LM741C.

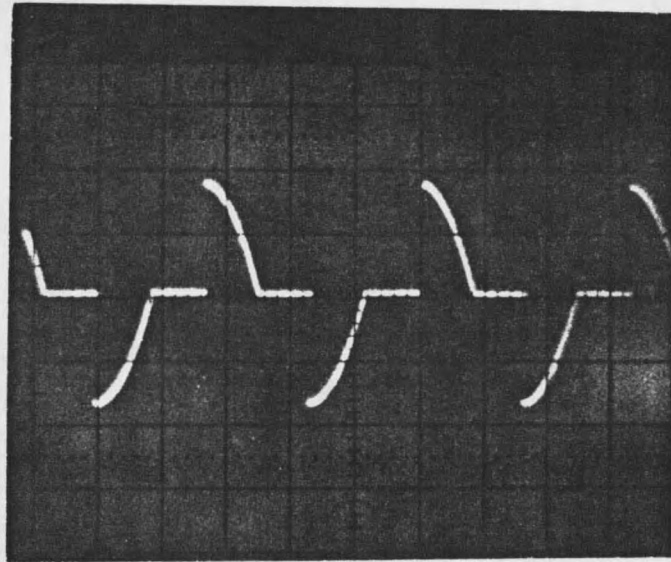


Figure 16. Measured waveforms across the load with a balanced load of 25Ω at $\alpha = 90^\circ$ using the PSBTPVC. Vertical : 100V/div. Horizontal : 5ms/div.

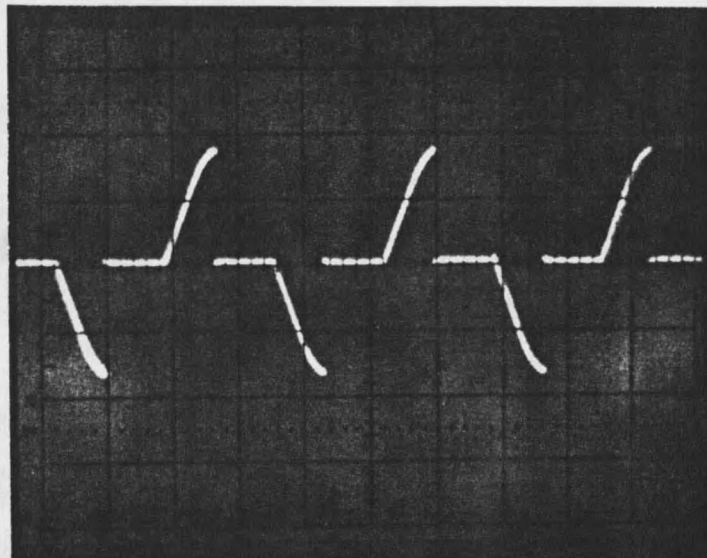


Figure 17. Measured waveforms across the thyristor with a balanced load 25Ω at $\alpha = 90^\circ$ using the PSBTPVC. Vertical : 100V/div. Horizontal : 5ms/div.

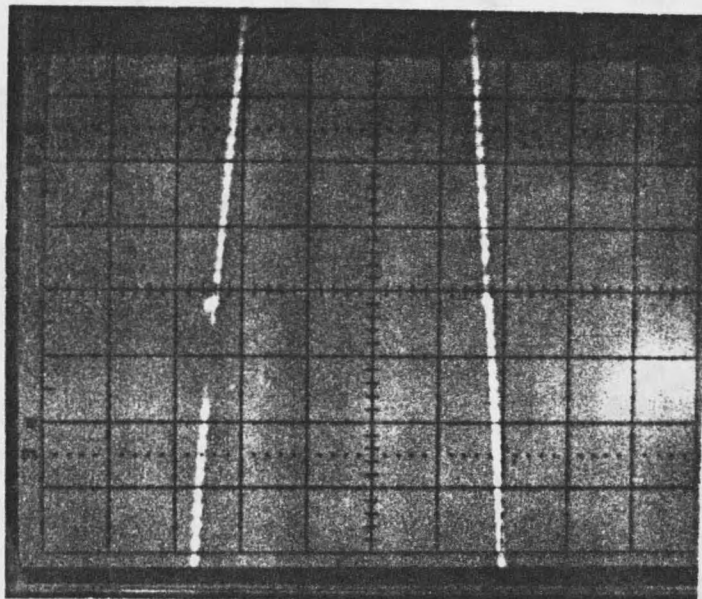


Figure 18. Measured maximum adjustable range of the PSBTPVC. The voltage across the thyristor with a balanced load of 25Ω at $\alpha = 180^\circ$.
Vertical : 10v/div. Horizontal : 2ms/div.

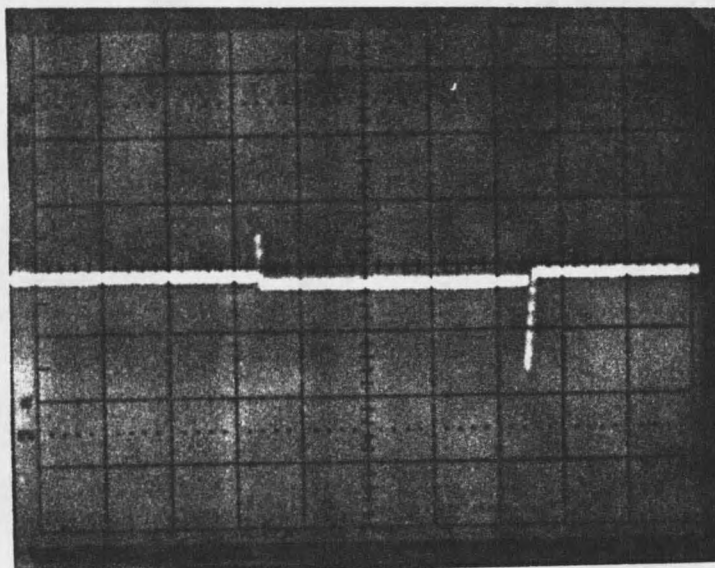


Figure 19. Measured waveforms across the resistor with a balanced load of 25Ω at $\alpha = 180^\circ$ using the PSBTPVC.
Vertical : 10V/div. Horizontal : 2ms/div.

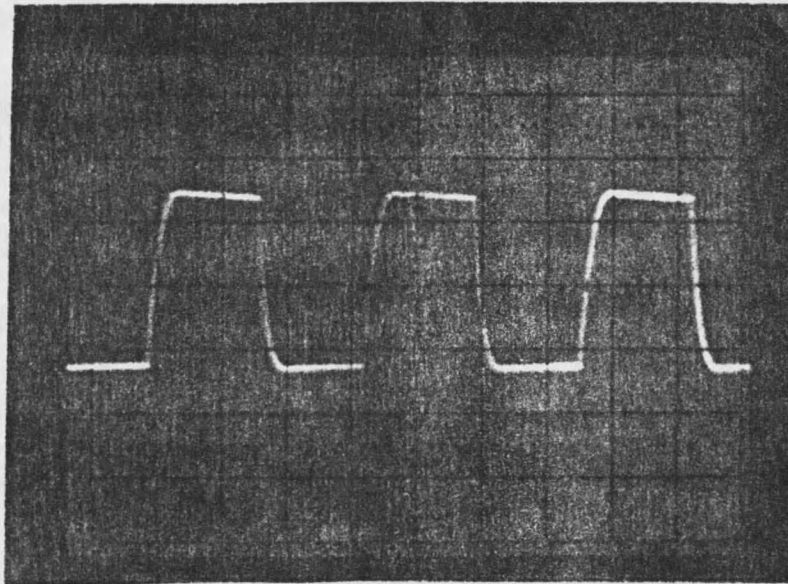


Figure 20. Measured waveforms across the capacitor with a balanced load of a 25Ω resistor and a $30\mu\text{F}$ capacitor connected in series at $\alpha = 90^\circ$ using the PSBTPVC.
Vertical : 100V/div. Horizontal : 5ms/div.

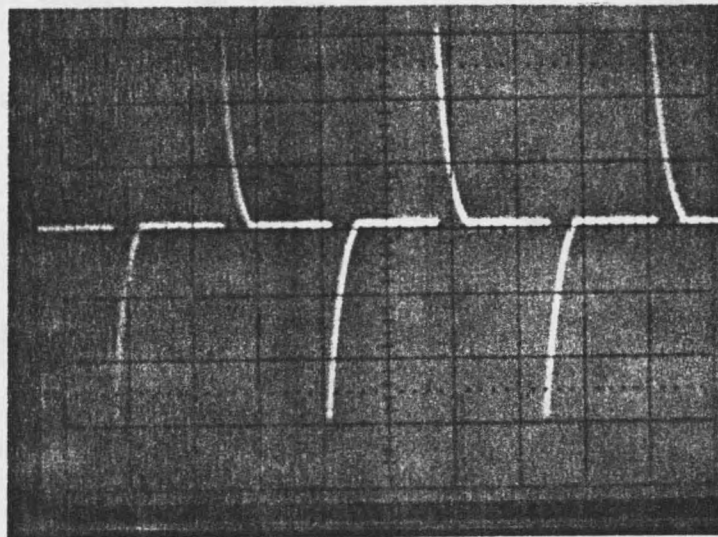


Figure 21. Measured waveforms across the resistor with a balanced load of a 25Ω resistor and a $30\mu\text{F}$ capacitor connected in series at $\alpha = 90^\circ$ using the PSBTPVC.
Vertical : 50V/div. Horizontal : 5ms/div.

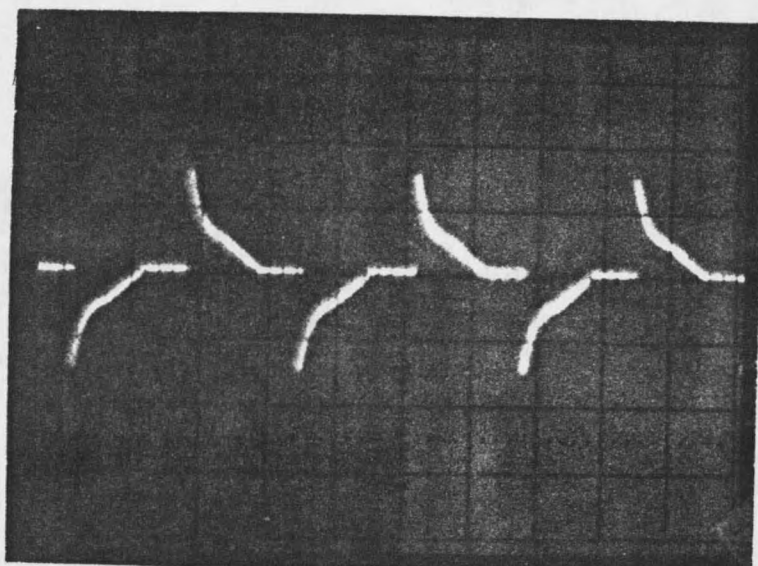


Figure 22. Measured waveforms across the resistor with a balanced load of a 25Ω resistor and a $30\mu\text{F}$ capacitor connected in series at $\alpha = 0^\circ$ using the PSBTPUC.
Vertical : 100V/div. Horizontal : 5ms/div.

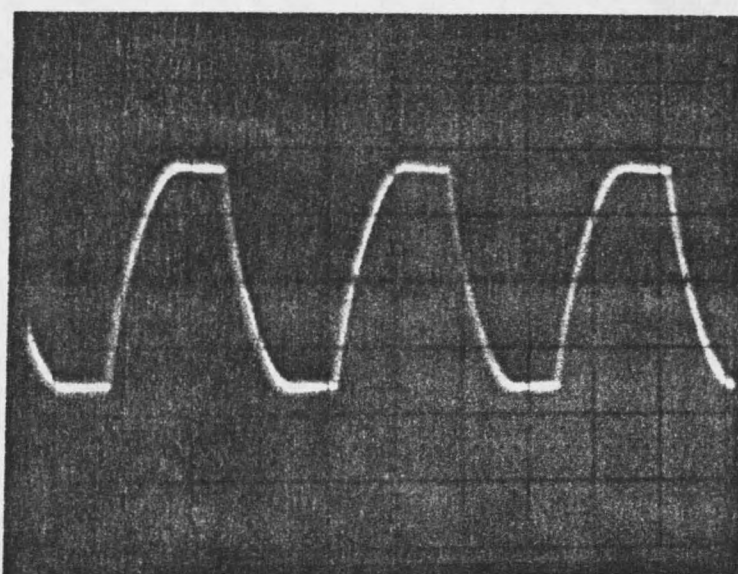


Figure 23. Measured waveforms across the capacitor with a balanced load of a 25Ω resistor and a $30\mu\text{F}$ capacitor connected in series at $\alpha = 0^\circ$ using the PSBTPUC.
Vertical : 100V/div. Horizontal : 5ms/div.

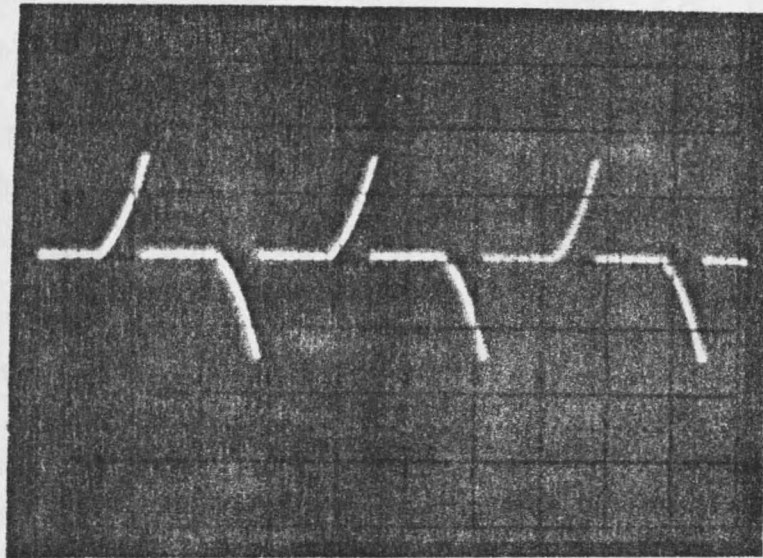


Figure 24. Measured waveforms across the thyristor with a balanced load of a 25Ω resistor and a $30\mu\text{F}$ capacitor connected in series at $\alpha = 0^\circ$ using the PSBTPVC.
Vertical : 100V/div . Horizontal : 5ms/div .

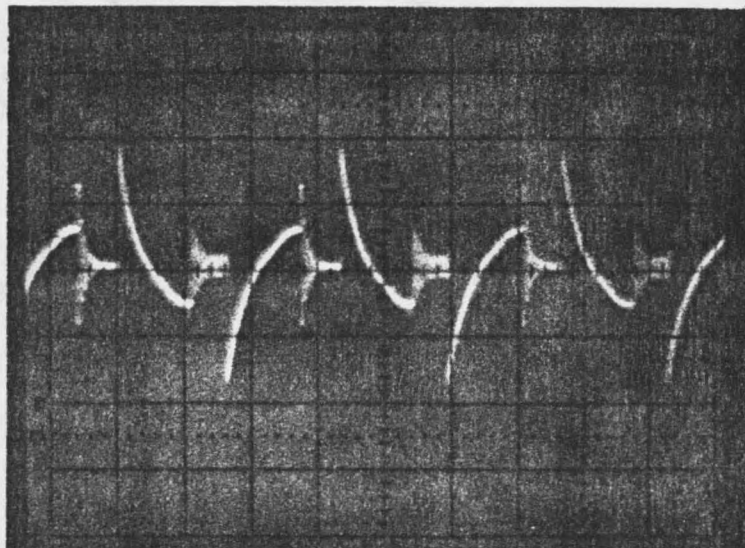


Figure 25. Measured waveforms across the inductor with a balanced load of a 100Ω resistor and a 98.25mH inductor connected in series at $\alpha = 90^\circ$ using PSBTPVC.
Vertical : 100V/div . Horizontal : 5ms/div .

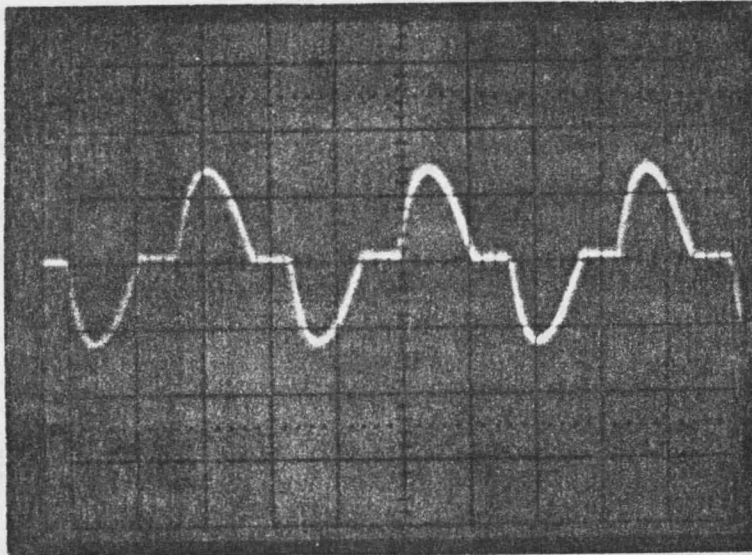


Figure 26. Measured waveforms across the resistor with a balanced load of a 100Ω resistor and a 98.25mH inductor connected in series at $\alpha = 90^\circ$ using the PSBTIPVC.

Vertical : 100V/div . Horizontal : 5ms/div .

Conclusions

With regard to the simplification of the circuit proposed by Le and Berg [1], the following conclusions are drawn from the study and the experimental results reported in this chapter.

1. Simplicity and low cost are the advantages of PSBTIPVC.
2. PSBTIPVC needs only one transformer to sense the line signal and it has no misfiring problem.
3. Nonlinearity and higher error compared to a linear-ramp-based circuit are the disadvantages of PSBTIPVC. It is difficult to adjust the firing angle to the desired values.

CHAPTER 3

RAMP-COMPARATOR-BASED FIRING CIRCUIT DESIGN

Introduction

This chapter focuses on studying the three-phase ramp-comparator based linear firing circuit for naturally commutated power electronic circuits like an AC voltage controller, rectifier bridge and inverter. One of the disadvantages of the control scheme presented in the previous chapter is the nonlinearity of the circuit. The concept of developing a linear firing circuit has been presented in Arockiasamy and Doraipandy [3], and Westinghouse [8]. However, the circuits presented in the references [3] and [8] are linear ramp-comparator-based single phase circuits. In Dubey, Doradla, Joshi and Sinha [10], the concept of a linear ramp-comparator approach has been applied in designing line commutated three-phase AC to DC converters. Unfortunately, the circuits in [3], [8] and [10] have error terms because of the discharge of the charged capacitor. An error term blocking circuit has been developed to avoid the effects due to the discharging errors. In addition, the complete design procedure of the three-phase ramp-comparator-based linear firing circuit is presented and the experimental results to prove the

validity of the circuit are presented as well.

Basic Ramp-Comparator Circuit

A ramp generator shown in Figure 27. A ramp-comparator circuit is composed of two elements, a ramp generator [14] and a comparator as shown in Figure 28.

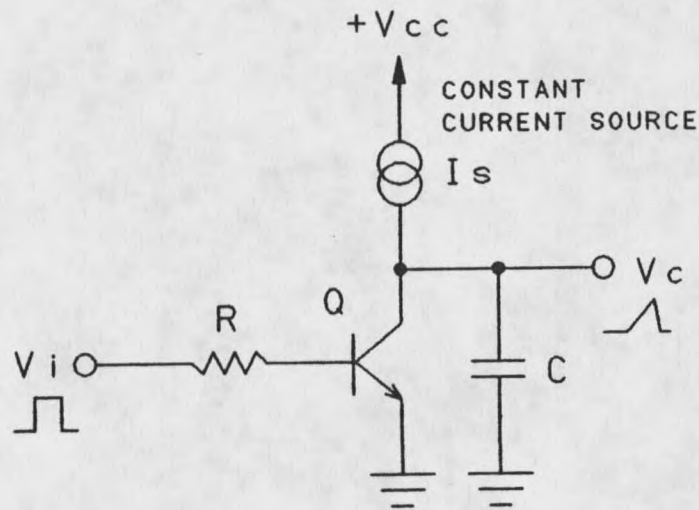


Figure 27. A ramp generator.

In Figure 27, the input pulse voltage, V_i , is used to switch the bipolar junction transistor. While the transistor is off, the capacitor C charges according to the following relationship,

$$dV_c = \frac{I_s dt}{C} \quad (3.1)$$

where V_c is the voltage across the capacitor C . If the current source, I_s , is a constant current generator, V_c

will increase linearly with time. If the non-inverting input of a comparator is connected to the V_c of a ramp generator as shown in Figure 28, the output of the comparator can be controlled by changing the reference voltage, V_{ref} , which is applied to the inverting input of the comparator. As a result, linear control of V_o can be obtained.

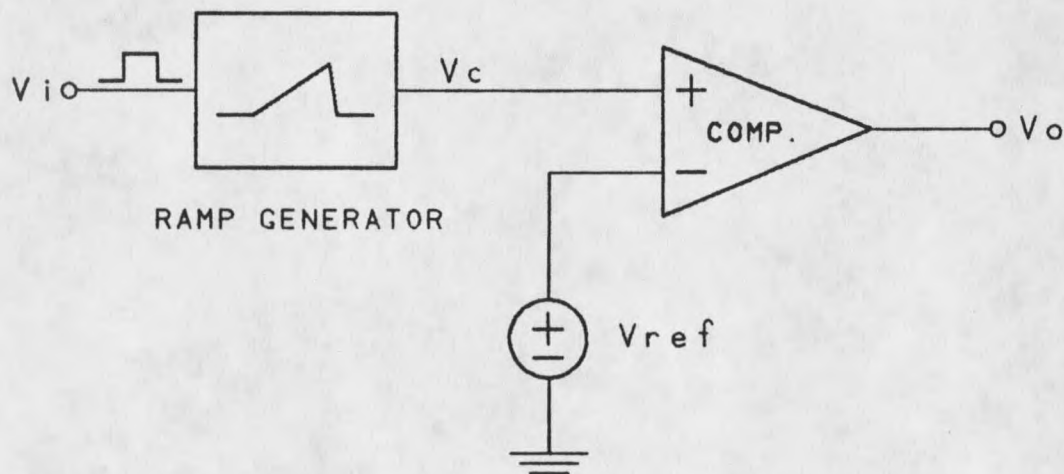


Figure 28. A basic ramp-comparator circuit.

An Error Blocking Circuit

One major problem in the circuit of Figure 27 is caused by discharging the capacitor of the ramp generator and is shown in Figure 29. In Figure 29, t_d is the error term caused by the discharging capacitor of the ramp generator. As a result, V_o in Figure 28 contains an error. The error is mainly dependent upon how long it takes to discharge the capacitor. The error term is the percentage of the ratio of the discharging time to the charging time. If this error

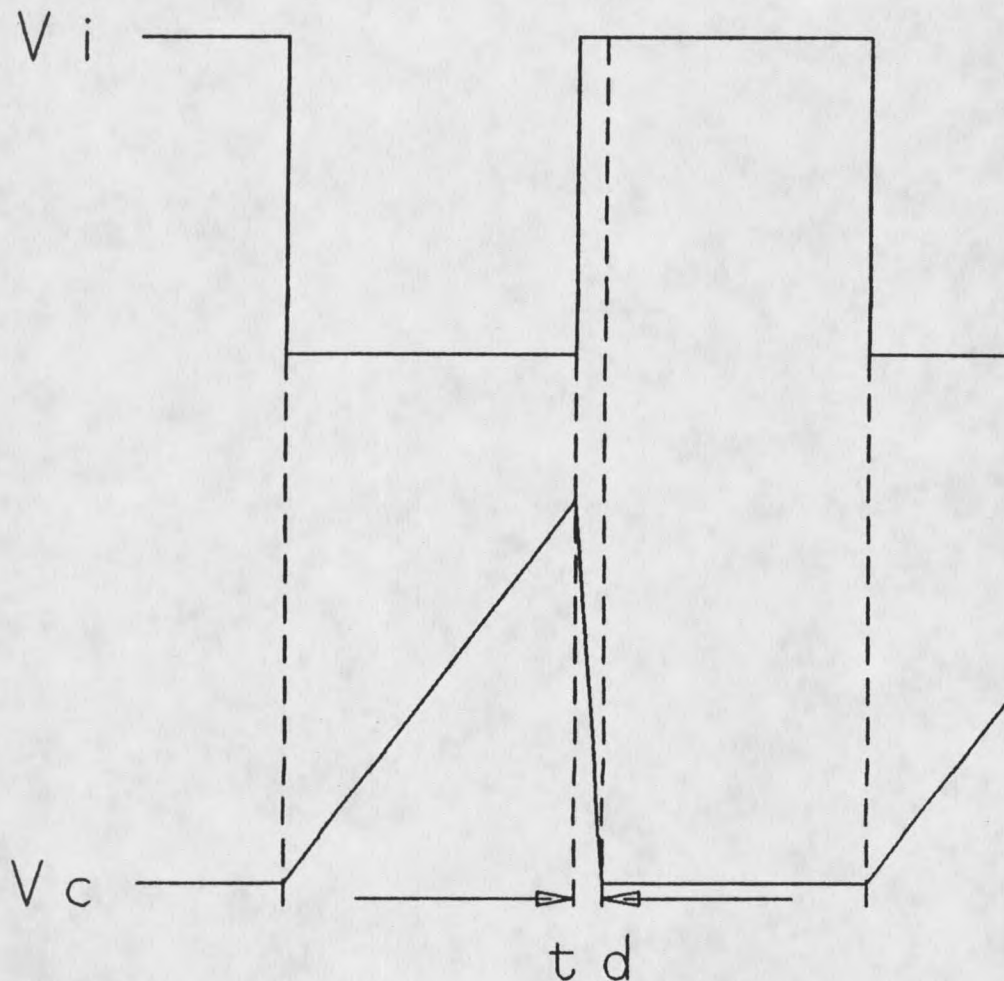


Figure 29. The pulse response of a ramp generator.

cannot be eliminated, the controller circuit will misfire. One thing which can be done to avoid the discharging error is to add an additional discharging circuit to the output of the ramp generator. This addition can minimize t_d . However, it is impossible to reduce t_d to zero. A new technique called error blocking, which is developed by the author, and can be used to block the discharging error, is shown in Figure 30.

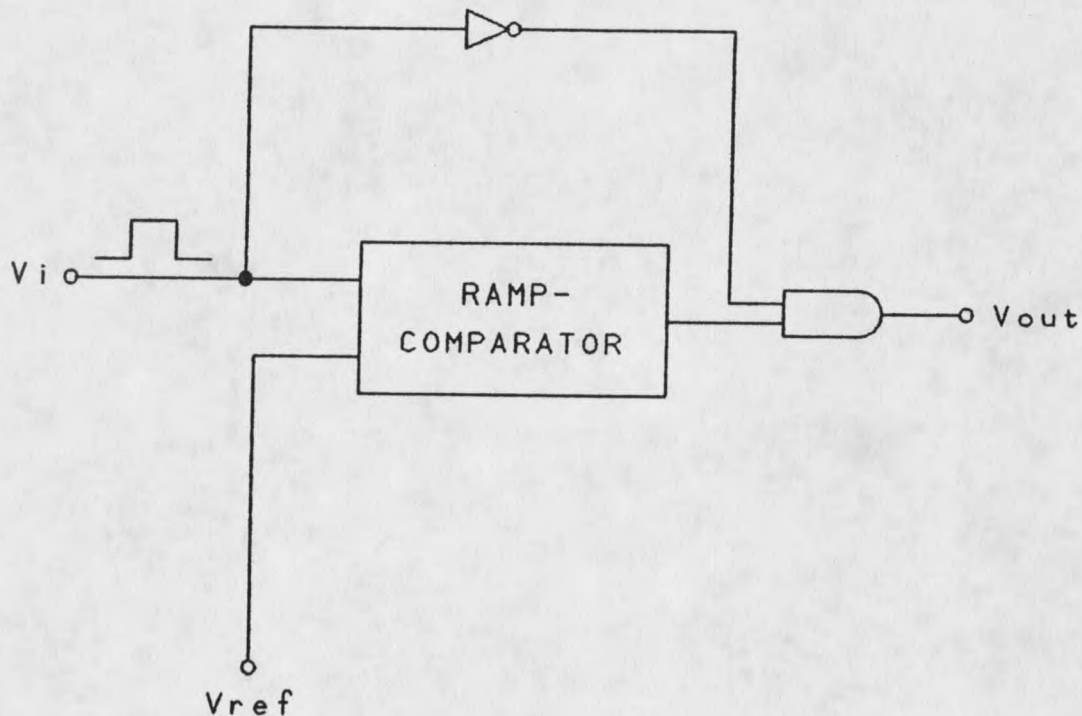


Figure 30. A basic error blocking circuit.

From the previous section when the input signal of the ramp generator is low, the linear ramp waveform is generated. An inverter and an AND gate are added to the circuit. If the input signal, V_i , goes low, the output of the inverter will go high. If V_c is greater than V_{ref} in Figure 28, V_{out} will go high. No matter whether the ramp-comparator output is high or low, if V_i goes high, V_{out} will go low. In other words, the addition of an inverter and an AND gate blocks the discharging error. The response of a basic error blocking circuit is shown in Figure 31.

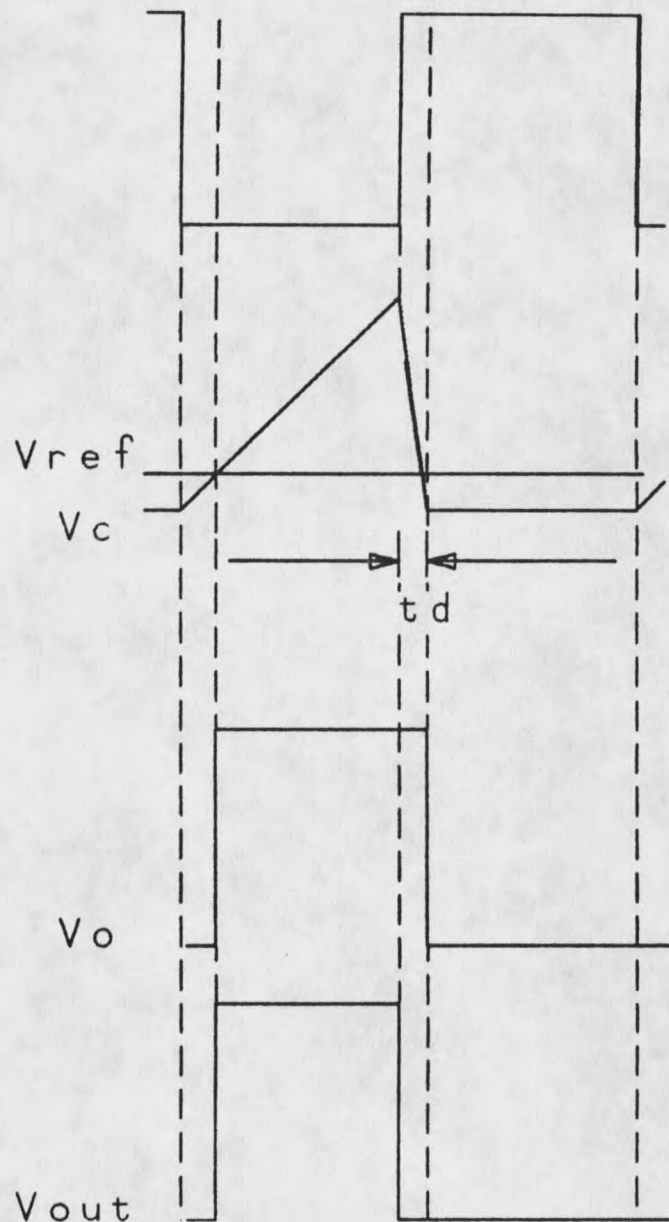


Figure 31. The pulse response of an error blocking circuit.

Correction of the Error Due to
Saturation of the Transistor

Referring to Figure 27, if the transistor is overdriven the saturation voltage will drop to a small value. Although

the value is very small, it does affect the performance of the circuit. It is necessary to correct this error term. The author's preliminary design mainly dealt with the reduction of the error term by adjusting the current of the current source. As a result, at 180° the output voltage of the ramp generator was equal to 1.80 volts plus the error term (the saturation voltage of the transistor). At a phase angle of 0° , the output voltage of the ramp generator was equal to the error term. If a ramp-generator-based three-phase voltage controller is considered, the controller requires six ramp generators. Because of the tolerances of the components of the ramp generators, the currents of the constant current sources must be adjusted to generate the same output voltages for each of the ramp generators. According to the experimental results, the variation in the saturation voltages of six Motorola 2N2222A transistor ramp used in generators was 5mV. The error is 0.25° for 5mV variation. It is an acceptable error compared to an 8.78° error in [1].

Improve Performance of the Ramp Generator by Using a SPICE Simulation

Using SPICE and the model of a 2N2222 in SPICE, the author simulated the circuit as shown in Figure 27 and the results of the SPICE simulation for various values of base resistor R are shown in Figures 32, 33, 34 and 35. The SPICE program is listed in Appendix B. According to the

SPICE results, the more the transistor is overdriven the lower the transistor saturation voltage will be. That is confirmed by the transistor data book. If the value of R is 500Ω and the saturation voltages of the six transistors vary 30%, the error will be about 0.17° , a very small error. However, the error term induced by the offset voltage of the comparator is quite large so that it is necessary to take this error term into account. The author used an LM339 for the comparator in the ramp-comparator circuit. The LM339 chip has a typical offset voltage value of $\pm 2\text{mv}$ and the maximum offset voltage of $\pm 5\text{mv}$ at a room temperature of 25°C . Usually, if the worst case error is considered, the maximum offset voltage has to be used to

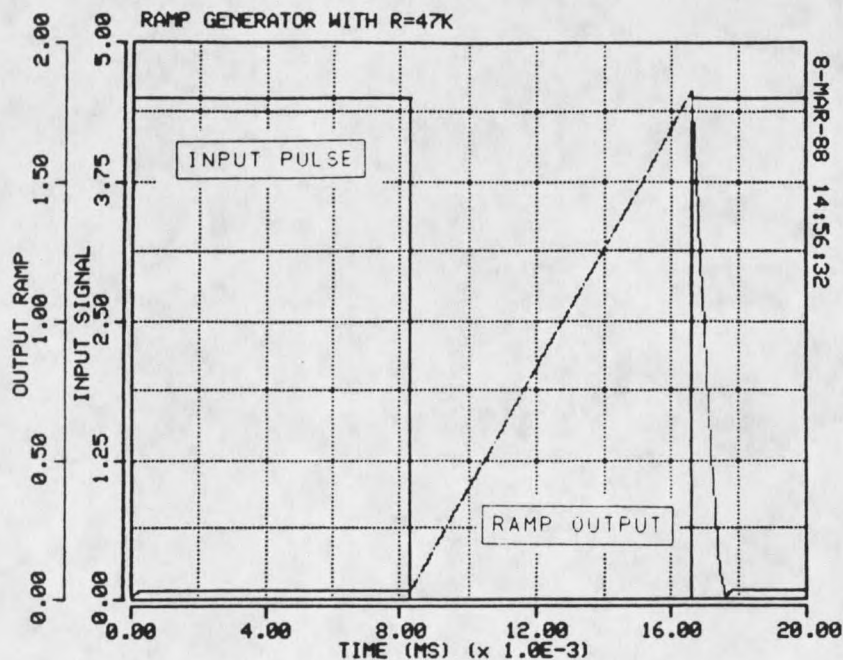


Figure 32. The response of a ramp generator with $R = 47\text{K}\Omega$.

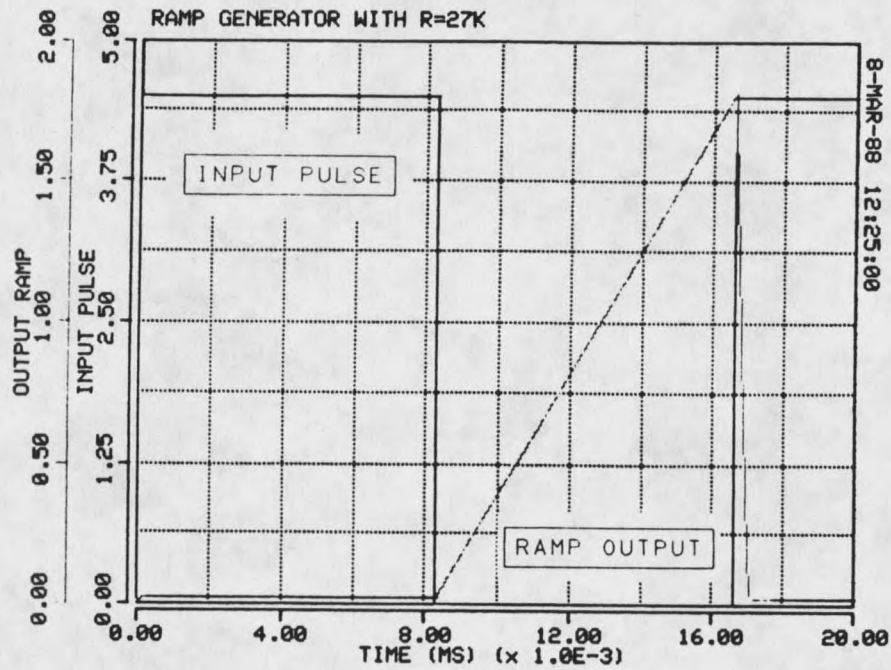


Figure 33. The response of a ramp generator with $R = 27K\Omega$.

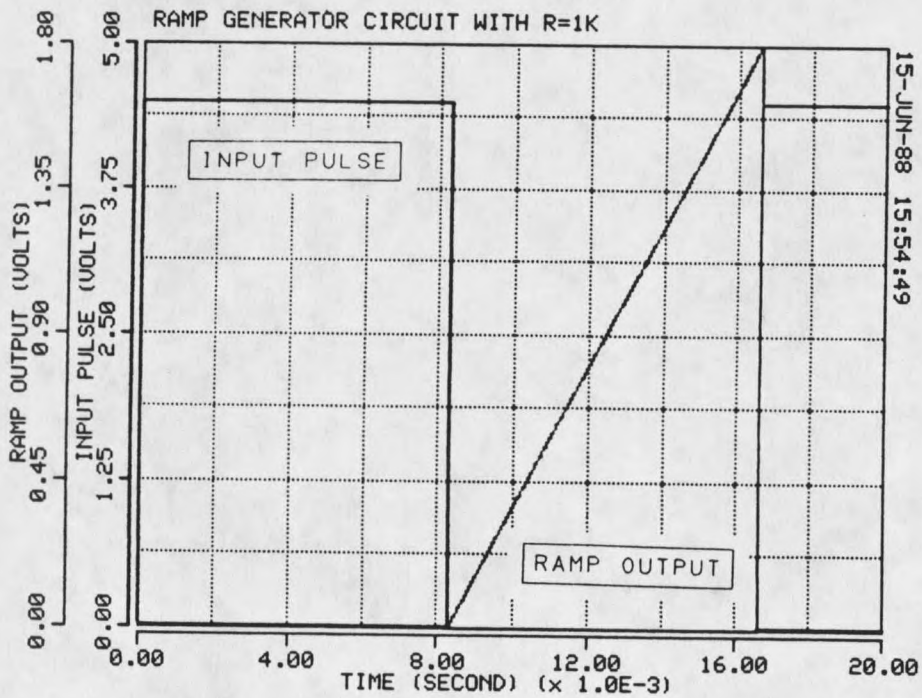


Figure 34. The response of a ramp generator with $R = 1k\Omega$.

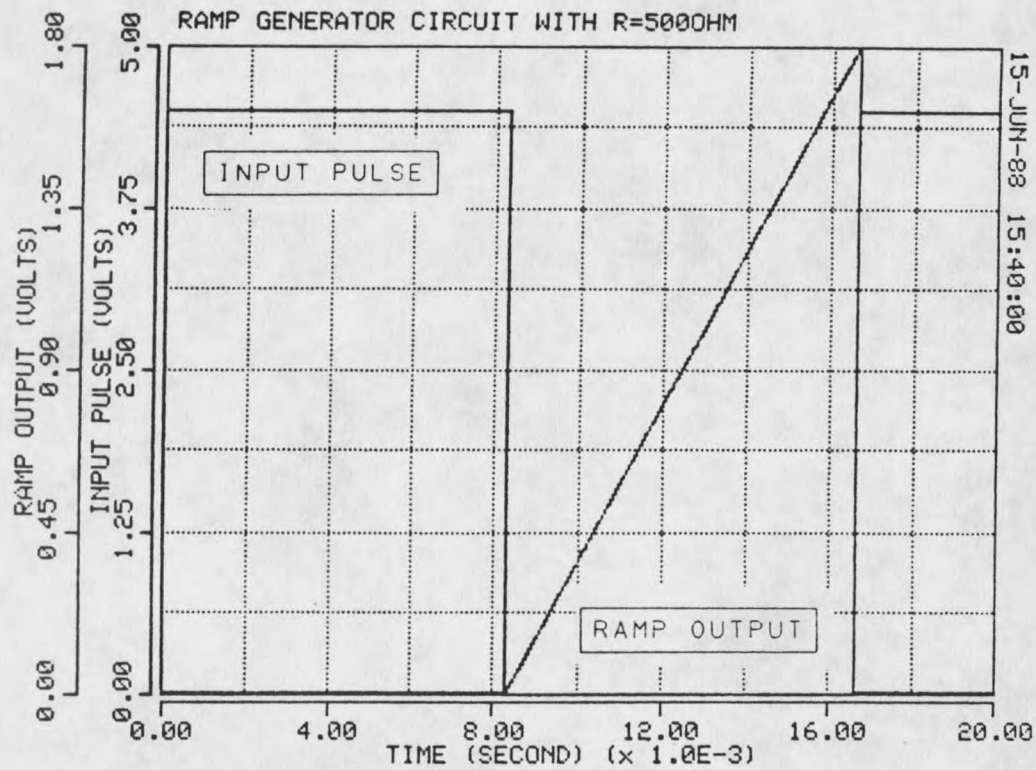


Figure 35. The response of a ramp generator with $R = 500\Omega$.

calculate the total error of the ramp-comparator circuit.

Error Analysis of the Ramp-Comparator Circuit

The maximum error of the ramp generators $Err1(max)$ may be defined as follows:

$$V_{err} = \frac{V_{ce(on)max} - V_{ce(on)min}}{2} \quad (3.2)$$

$$V_{ave} = \frac{V_{ce(on)max} + V_{ce(on)min}}{2} \quad (3.3)$$

$$\text{Err1(max)} = \pm \frac{V_{\text{err}} \times 180^\circ}{1.8} \quad (\text{in degrees}) \quad (3.4)$$

where

$V_{\text{ce(on)max}}$ = the highest $V_{\text{ce(on)}}$ value among the transistors

$V_{\text{ce(on)min}}$ = the lowest $V_{\text{ce(on)}}$ value among the transistors

V_{err} = the mean error voltage of the ramp generators

V_{ave} = the mean collector-emitter saturation voltage of the ramp generators.

An actual output waveform of the ramp generator is shown in Figure 36.

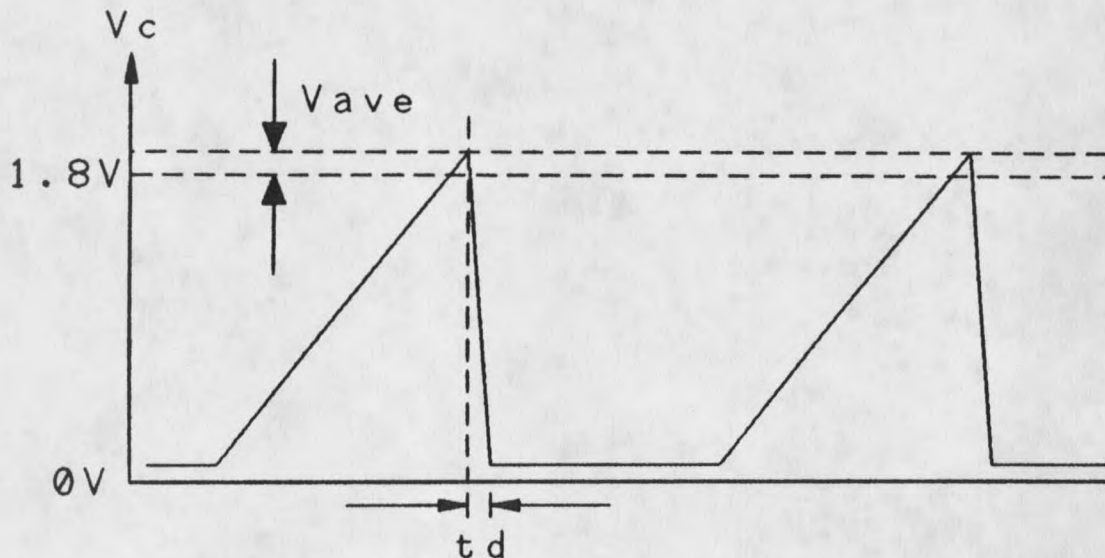


Figure 36. An actual output waveform of the ramp generator.

The output voltages of the ramp generators are adjusted to 1.80 volts plus the error term, V_{err} .

The maximum error of the comparators Err2(max) is obtained from

$$\text{Err2(max)} = \pm \frac{V_{os} \times 180^\circ}{1.8} \text{ (in degrees)} \quad (3.5)$$

where V_{os} is the maximum offset voltage of the comparators. The total error of the ramp-comparator circuits is equal to the sum of Err1(max) and Err2(max) .

If $R = 500\Omega$, and a 2N2222 and a LM339 are used for R, Q and the comparator respectively, the total calculated error of the ramp-comparator circuits is $\pm 0.67^\circ$. This value is the sum of Err1(max) , which is obtained from the last section, and Err2 which is obtained by applying equation (3.5) and the data given from last section. The author tested two LM339s. Each LM339 has four comparators. The offset voltages of eight comparators varied from -2mV to $+1.5\text{mV}$. The experimental sum of errors is approximately 0.43° . The calculated error is higher than the experimental error because the calculated error is the worst-case maximum error.

Error Analysis of the Pulse Driver Circuit

Consider the duty cycle of the modulated frequency of a driver circuit 50%.

For the ideal case,

$$\text{Error} = \frac{f_1 \times 180}{f_m} \quad (\text{in degrees}) \quad (3.6)$$

where f_1 is the line frequency and f_m is the modulated frequency of the pulse driver circuit.

Error Analysis of a Zero Crossing Detector Circuit

Figure 37 shows a zero crossing detector circuit.

In Figure 37,

$$V_2 = V_{cc} \left(\frac{R_1 + R_2}{R_1 + R_2 + R_3} \right) + V_{in} \left(\frac{R_3}{R_1 + R_2 + R_3} \right) \quad (3.7)$$

$$V_1 = V_{cc} \left(\frac{R_5 \cdot R_6}{R_5 \cdot R_6 + R_4 \cdot R_5 + R_4 \cdot R_6} \right) + \frac{V_o \cdot R_4 \cdot R_5}{R_5 \cdot R_6 + R_4 \cdot R_5 + R_4 \cdot R_6} \quad (3.8)$$

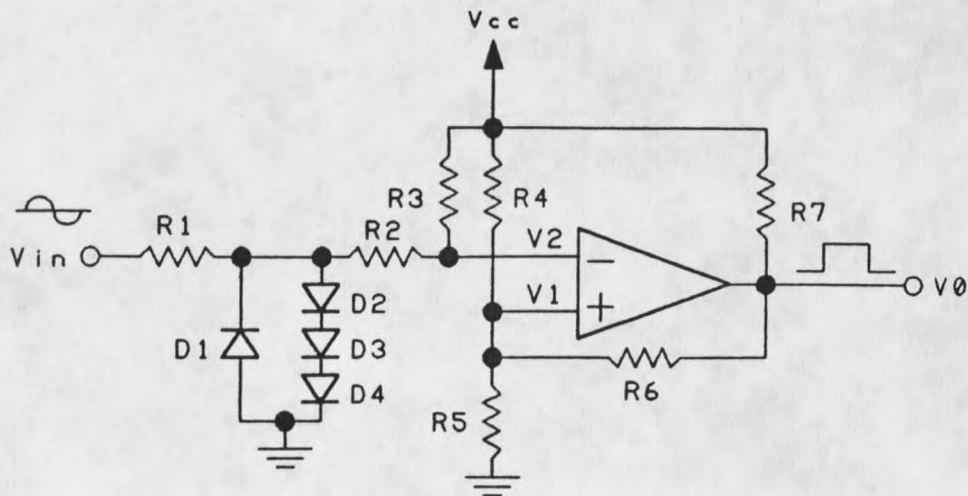


Figure 37. A zero crossing detector circuit.

If $R_6 \gg R_5$ and $R_6 \gg R_4$, equation (3.7) may be simplified.

$$V_1 = V_{cc} \left(\frac{R_5}{R_4 + R_5} \right) \quad (3.9)$$

If $R_1 + R_2 = R_5$ and $R_3 = R_4$ then equation (3.7) may be rewritten as

$$V_2 = V_{cc} \left(\frac{R_5}{R_4 + R_5} \right) + V_{in} \left(\frac{R_4}{R_4 + R_5} \right) \quad (3.10)$$

To change the state of the comparator,

$$V_1 - V_2 = \pm V_{os} .$$

In other words,

$$V_{in} \left(\frac{R_4}{R_4 + R_5} \right) = \pm \text{offset voltage} . \quad (3.11)$$

Offset voltage is an error of the circuit. The time delay of the comparator is also an error of the circuit. From equation (3.11), the higher input voltage has the smaller error.

Experimental Results of a Ramp Generator

Table 1 shows the experimental data (V_{ce} voltage) of the ramp generator circuit with different values of R and the same operating conditions as the previous section. Six ITT 2N2222A transistors were used in the experiment.

TRANSISTOR	R = 500 Ω V _{ce(sat)} in mV	R = 1K Ω V _{ce(sat)} in mV	R = 27K Ω V _{ce(sat)} in mV
1	15	17.75	96
2	16.25	19.25	103
3	15.25	18	97.5
4	16	19	100
5	15	17.8	108

Table 1. Experimental data of ramp comparators.

Application of Ramp-Comparator
Circuit in Firing Controller

The block diagram of a three-phase ramp-comparator-based firing controller is illustrated in Figure 38. For each phase, two ramp-comparator circuits are employed to keep the firing angles of the two thyristors 180° apart. Figure 39 shows the implementation of the block diagram in Figure 38 for one phase. Each phase has the same control circuit. For the three-phase firing circuit, there are three single phase control circuits which share the same reference voltage and the same modulated frequency signal. Twenty-seven kilohm resistors are used for the R of the ramp generators. The author calculated the value of R to be 27K Ω using the typical data of 2N2222 and an overdrive factor of 10 from the Motorola data book. The 27K Ω resistor may be too high, and it may cause larger variation of the V_{ce(sat)} of the transistors according to the experimental data.

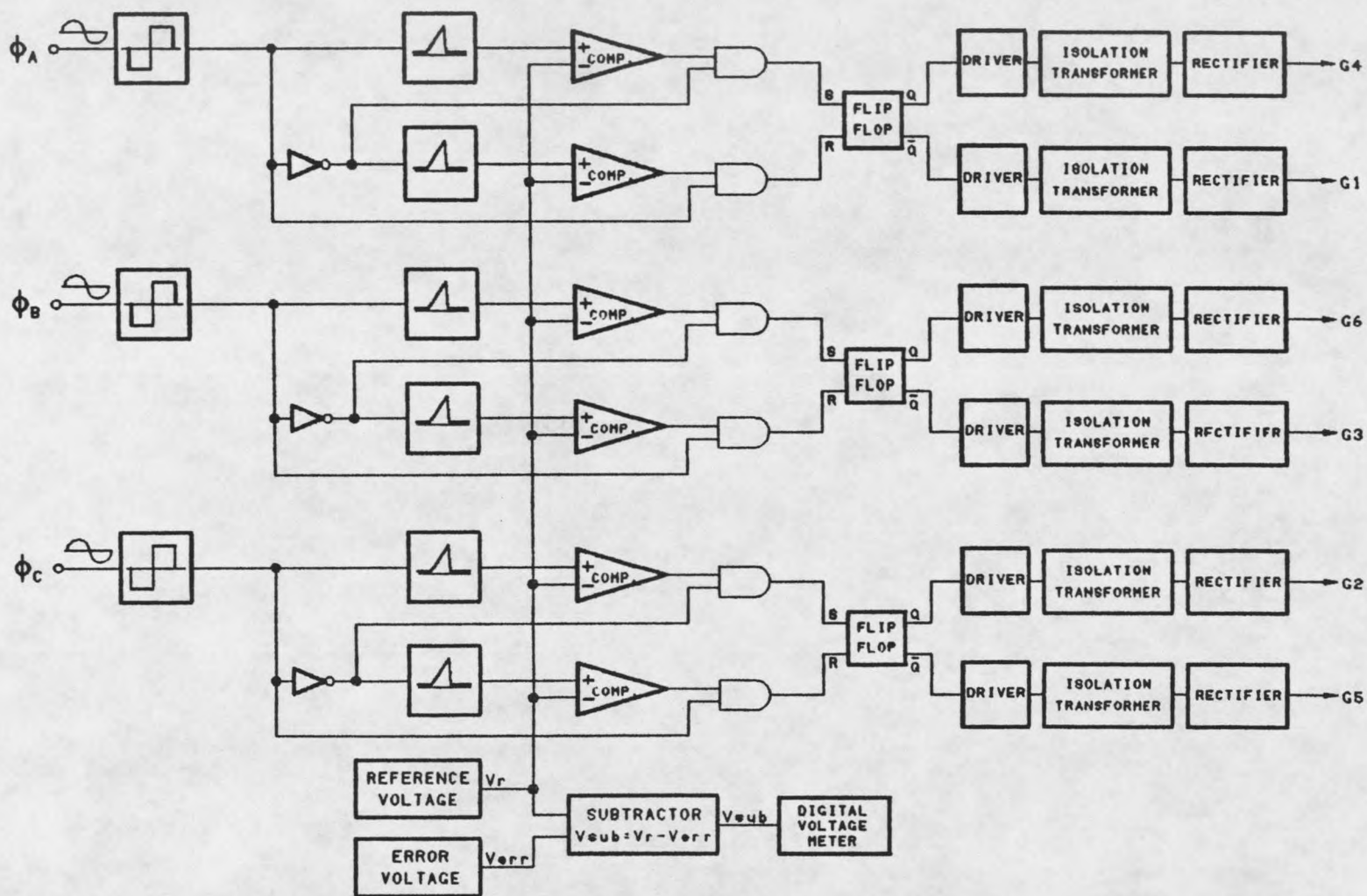


Figure 38. A block diagram of a three-phase ramp-comparator-based firing controller.

An Experiment of Ramp-Comparator-Based Three-Phase
Voltage Controller (RCBTPVC)

The configuration of the experiment is the same as in the last section and the connections of the controller are shown in Figure 40. The calibration procedures of RCBTPVC which are shown in Figure 39 are listed as follows:

1. Adjust the offset voltage of the subtractor by adjusting the 20K Ω trimmer.
2. Use an oscilloscope to find out the $V_{ce(on)}$ of each transistor and calculate V_{ave} .
3. Adjust the error voltage to V_{ave} .
4. Adjust the reference voltage until the output voltage is 1.800.
5. Connect the three-phase voltage source, the thyristors and a resistive load for one phase.
6. Use the oscilloscope to monitor the voltage across the load and adjust the constant current sources for the corresponding phase until the lowest error is obtained at $\alpha = 180^\circ$.
7. Repeat procedures 5 and 6 until all three phases have been completely calibrated.

Because of manufacturing constraints it may be desirable to use all six transistors from the same manufacturer and of the same manufacturing date in order to minimize the mean error voltage of the ramp generators. The RCBTPVC was fully calibrated. The three-phase output waveforms of the RCBTPVC are shown in Figure 41.

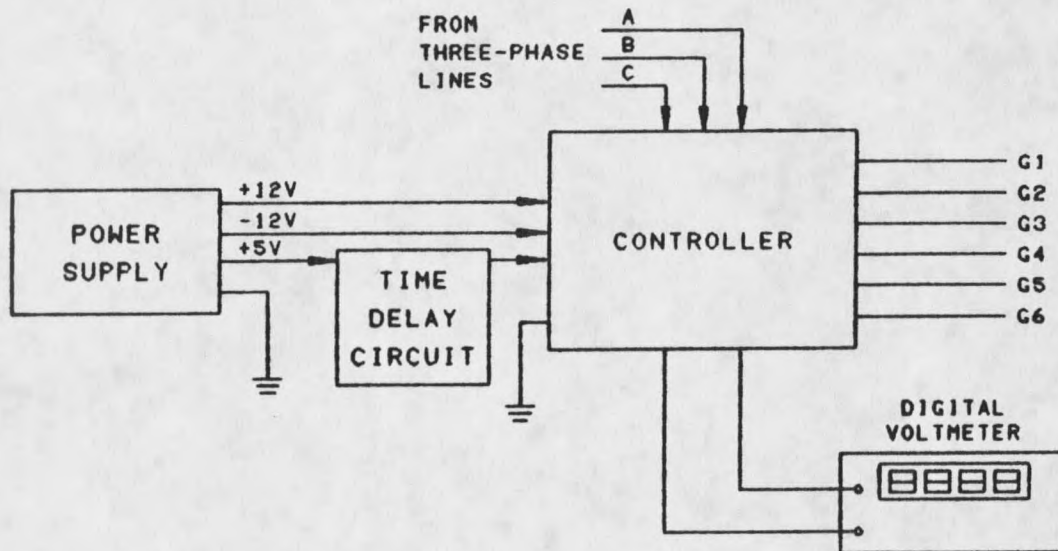


Figure 40. The connections of the RCBIPVC.

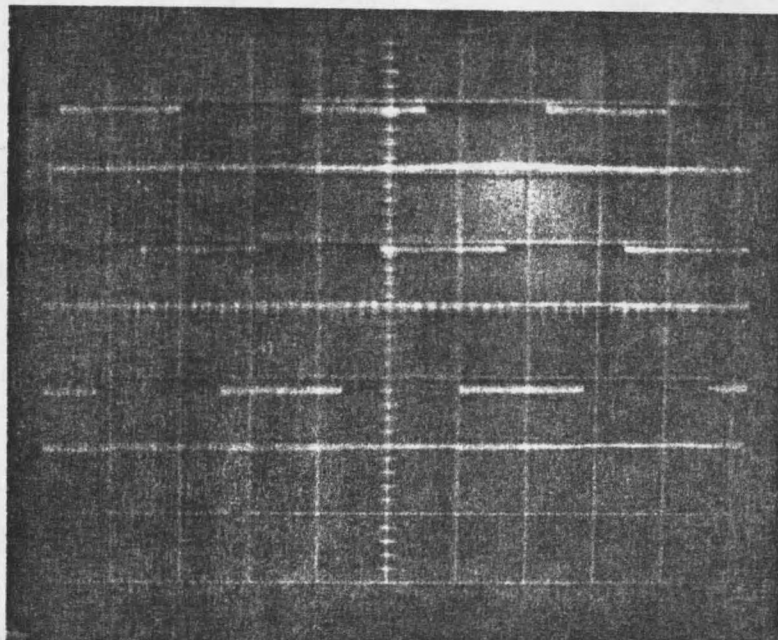


Figure 41. Measured three-phase output waveforms generated by RCBIPVC. Upper : 0°. Middle : 120°. Bottom : 240°. Vertical : 5V/div. Horizontal : 5ms/div.

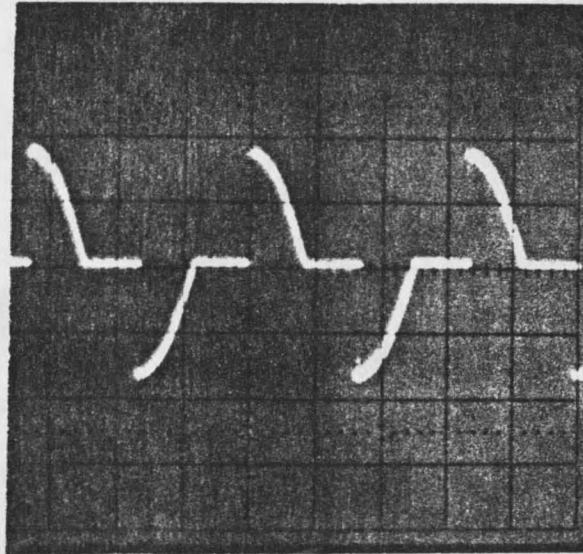
Experimental Results of the RCBTPVC

Figure 42. Measured waveforms across the load with a balanced load of 25Ω at $\alpha = 90^\circ$ using the RCBTPVC.
Vertical : 100V/div. Horizontal : 5ms/div.

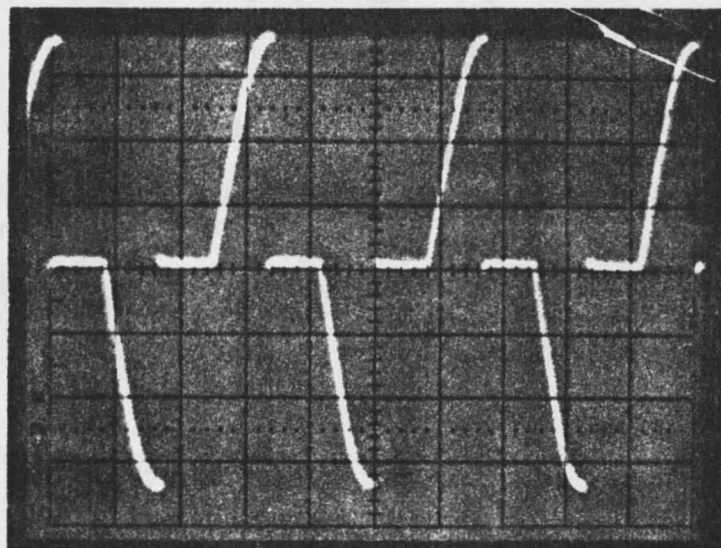


Figure 43. Measured waveforms across the thyristor with a balanced load of 25Ω at $\alpha = 90^\circ$ using the RCBTPVC.
Vertical : 50V/div. Horizontal : 5ms/div.

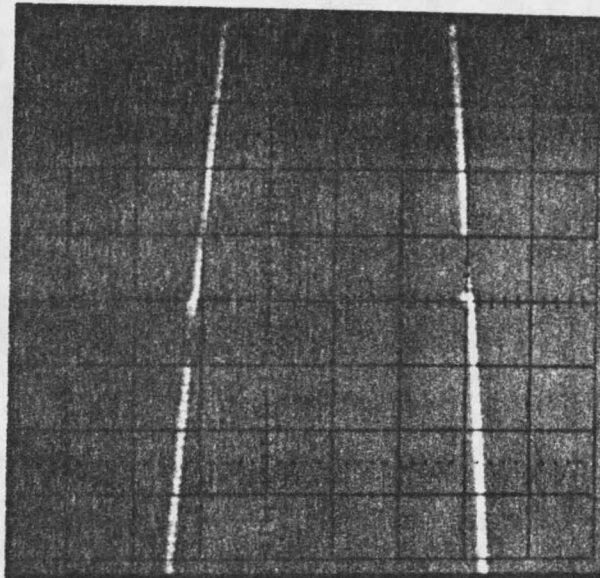


Figure 44. Measured maximum adjustable range of the RCBIPVC. The voltage across the thyristor with a balanced load of 25Ω at $\alpha = 180^\circ$.
Vertical : 10V/div. Horizontal : 2ms/div.

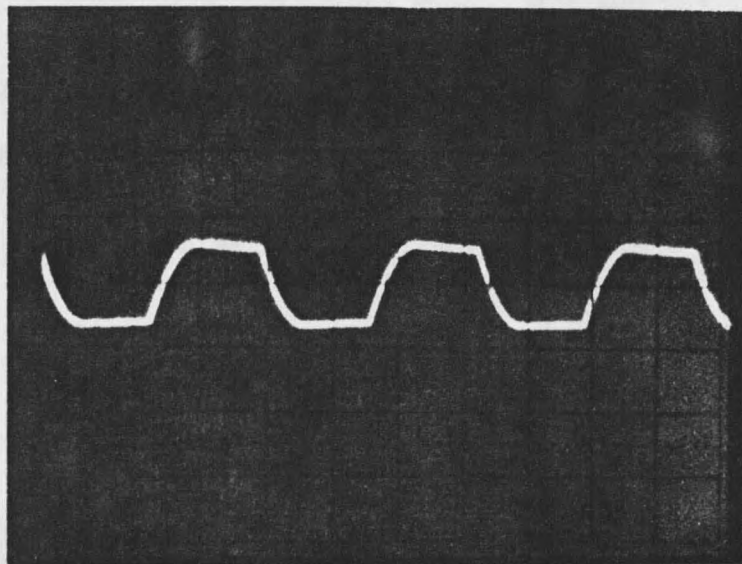


Figure 45. Measured waveforms across the capacitor with a balanced load of a 25Ω resistor and a $30\mu\text{F}$ capacitor connected in series at $\alpha = 90^\circ$ using the RCBIPVC.
Vertical : 50V/div. Horizontal : 5ms/div.

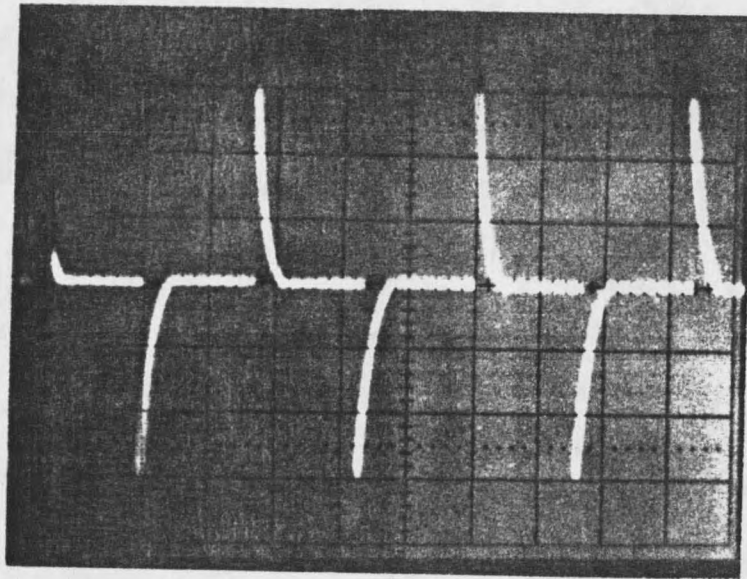


Figure 46. Measured waveforms across the resistor with a balanced load of a 25Ω resistor and a $30\mu\text{F}$ capacitor connected in series at $\alpha = 90^\circ$ using the RCBTPVC.

Vertical : 50V/div . Horizontal : 5ms/div .

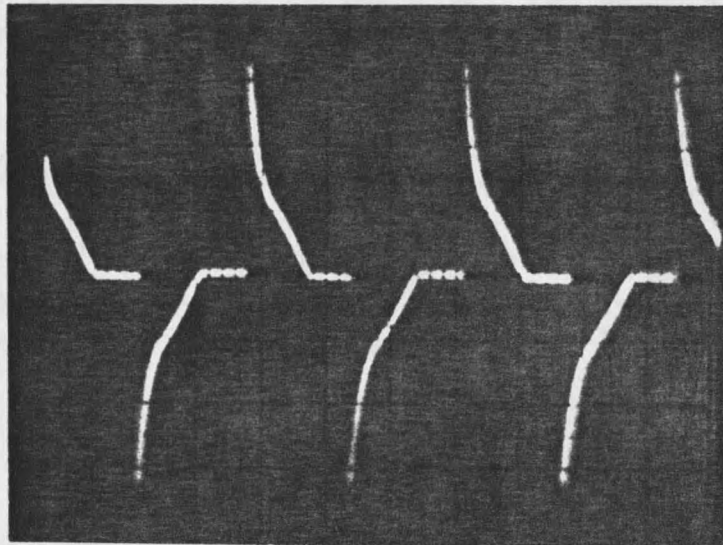


Figure 47. Measured waveforms across the resistor with a balanced load of a 25Ω resistor and a $30\mu\text{F}$ capacitor connected in series at $\alpha = 0^\circ$ using the RCBTPVC.

Vertical : 50V/div . Horizontal : 5ms/div .

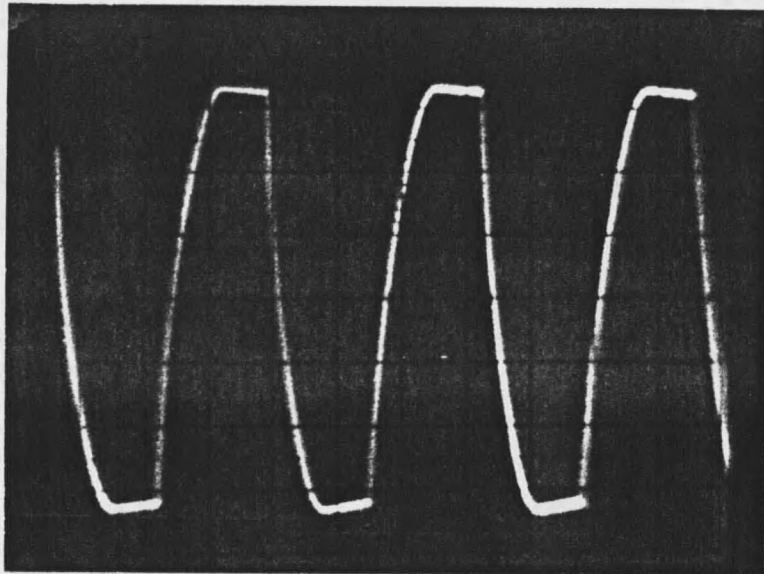


Figure 48. Measured waveforms across the capacitor with a balanced load of a 25Ω resistor and a $30\mu\text{F}$ capacitor connected in series at $\alpha = 0^\circ$ using the RCBTPVC.
Vertical : 50V/div. Horizontal : 5ms/div.

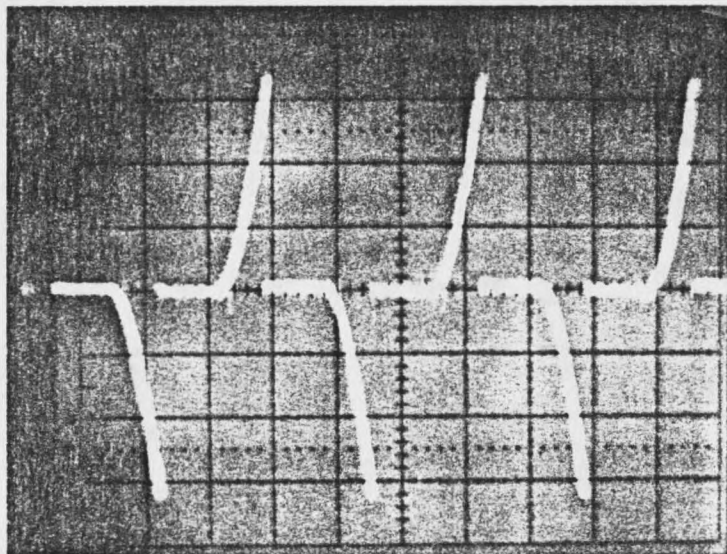


Figure 49. Measured waveforms across the thyristor with a balanced load of a 25Ω resistor and a $30\mu\text{F}$ capacitor connected in series at $\alpha = 0^\circ$ using the RCBTPVC.
Vertical : 50V/div. Horizontal : 5ms/div.

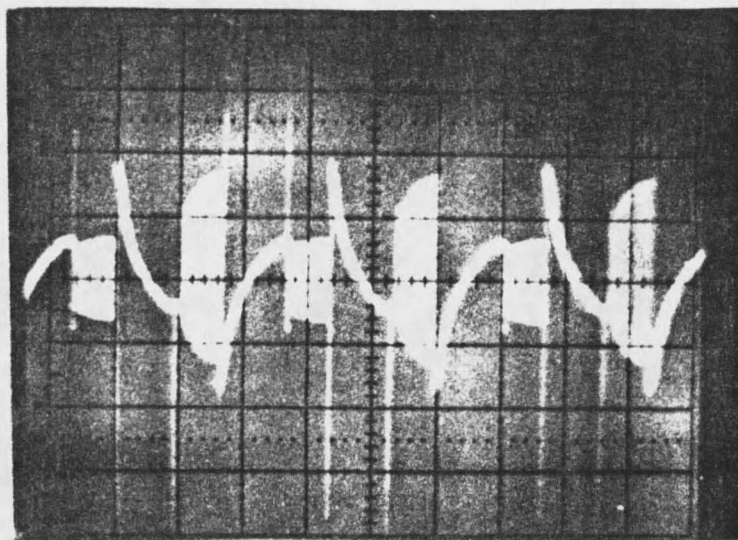


Figure 50. Measured waveforms across the inductor with a balanced load of a 100Ω resistor and a 98.25mH inductor connected in series at $\alpha = 90^\circ$ using RCBTPVC.
Vertical : 50V/div . Horizontal : 5ms/div .

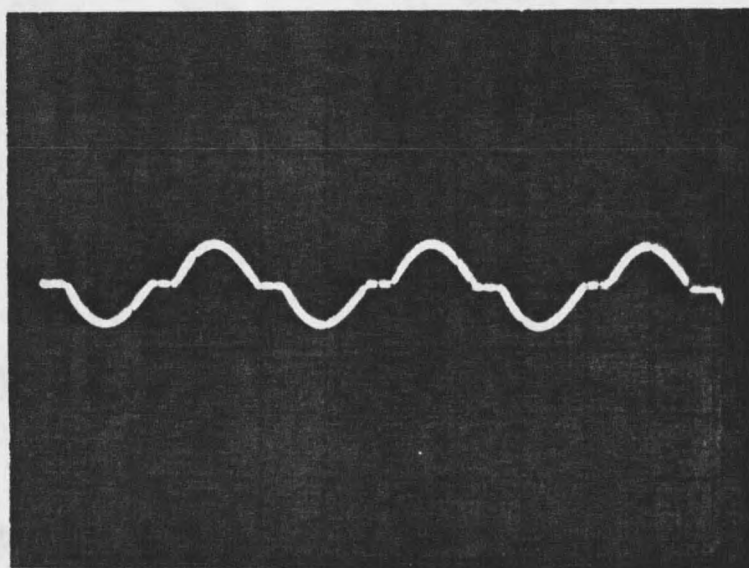


Figure 51. Measured waveforms across the resistor with a balanced load of a 100Ω resistor and a 98.25mH inductor connected in series at $\alpha = 90^\circ$ using the RCBTPVC.
Vertical : 100V/div . Horizontal : 5ms/div .

Figures 41 to 51 show the responses of the load and the thyristor with different loads and different firing angles. The measured range of the firing angle was from 0° to 176.78° .

Conclusions

The following conclusions are drawn from the study and the experimental results reported in this chapter.

1. Linear control of firing angle and greater accuracy than PSBTPVC are the advantages of RCBTPVC.
2. The RCBTPVC has the following disadvantages:
 - a. Poor transient response.
 - b. Misfiring if the noise level is high enough to trigger the set-reset flip-flop.
 - c. More expensive than PSBTPVC.
 - d. Poor thermal stability. The current of the constant current source chip changes with temperature.
 - e. The need for three input transformers to sense three-phase signals.
 - f. All the outputs of the controller may have different errors.

CHAPTER 4

PHASE-LOCKED-LOOP-BASED FIRING CONTROLLER DESIGN

Introduction

This chapter is devoted to the study of the phase-locked-loop-based linear firing circuit. The phase-locked-loop-based firing circuit has the advantage of firing the controlled thyristors at a constant, equidistant spacing. The control scheme presented in the last chapter has the problem of complex calibrating procedures. In Simard and Rajagopalan [6], an equidistant pulse firing scheme is proposed to give a more simple firing circuit to control a three-phase inverter. However, the scheme proposed by Simard and Rajagopalan [6] is nonlinear and it introduces an unnecessary error term. The maximum error that may be introduced in the equidistant spacings of the consecutive pulses can be shown to be $360^\circ/N$ where N is a frequency multiplying factor [10]. An improved scheme which keeps all the advantages of the phase-locked-loop and eliminates all the disadvantages in [6] has been implemented. Further, the complete design procedure of the phase-locked-loop-based linear firing circuit is reported. The experimental results are also presented to verify the validity of the circuit.

Basic Phase-Locked Loop

A phase-locked loop is commonly used in motor control, frequency synthesizers and radio receivers. In designing a thyristorized three-phase AC to DC converter, a phase-locked technique is usually employed to generate equidistant spacings of six consecutive pulses for triggering six thyristors. The basic principle of the equidistant pulses scheme by Simard and Rajagopalan [6] is simplified into a scheme as shown in Figure 52.

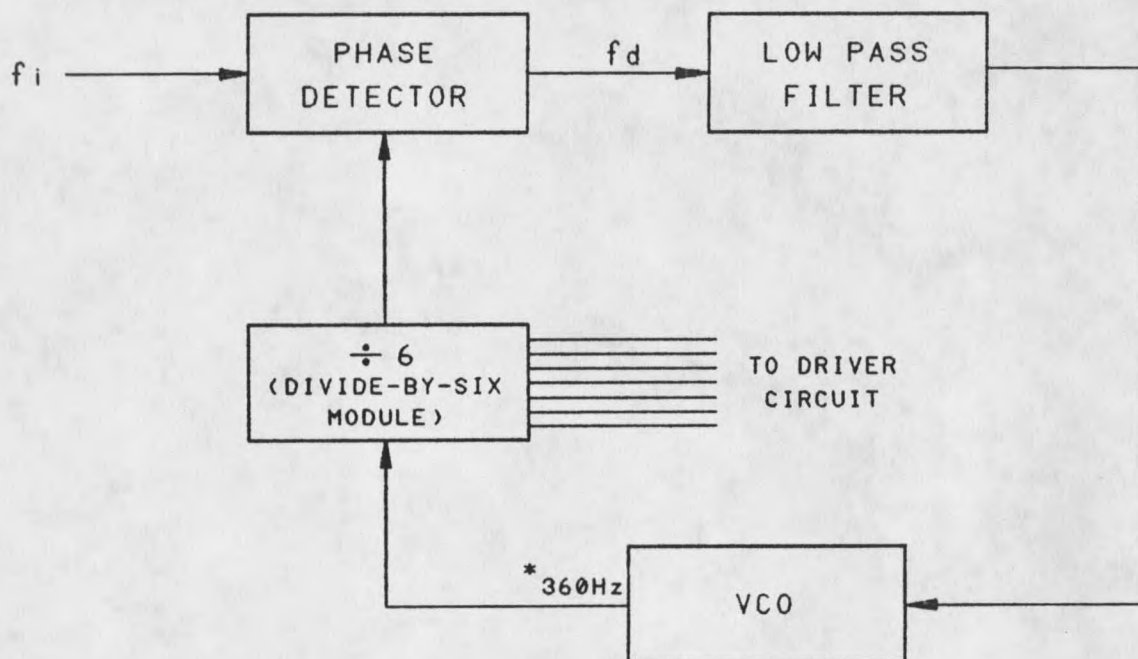


Figure 52. A block diagram of equidistant pulses scheme.

In Figure 52, when the phase detector receives the input frequency, f_i , the phase detector outputs a phase difference signal, f_d , by comparing the signals of f_i and f_c . After the low pass filter receives the output signals

from the phase detector, the low pass filter integrates the phase difference signal and outputs a DC signal. This DC signal can control the output frequency of the voltage controlled oscillator, VCO. Then the output signal of the VCO is divided by 6 and the resulting signal is the f_c . The

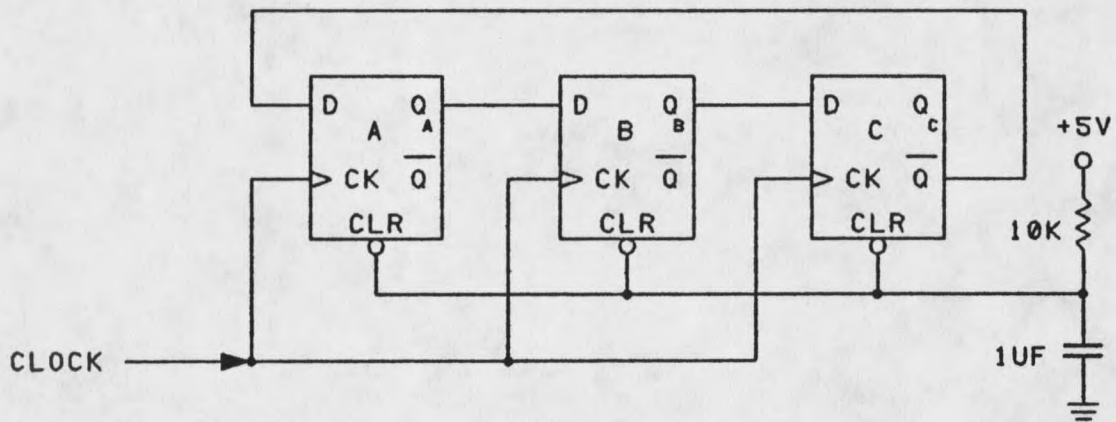


Figure 53. A divide-by-six module.

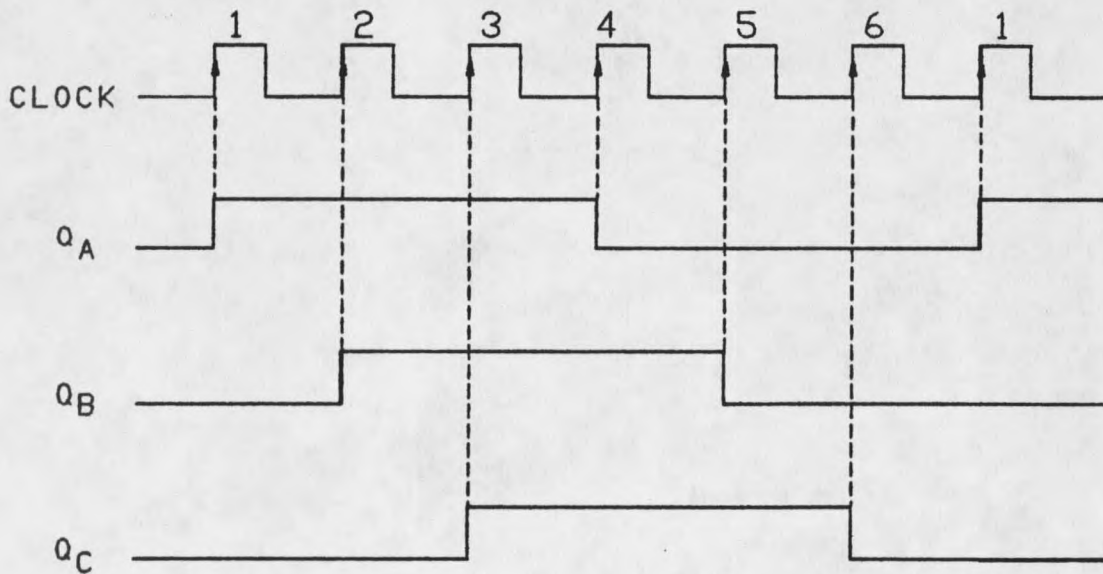


Figure 54. The timing diagram of the divide-by-six module.

output logic signals of the divide-by-six module can be used to drive the driver circuit. In other words, the circuit in Figure 52 works like a frequency multiplier. A divide-by-six module can be implemented by using three flip-flops. Figure 53 shows the schematic of the divide-by-six module, and Figure 54 shows its timing diagram [12].

Phase-Locked-Loop-Based Firing Controller

A phase-locked-loop (PLL) can be used to control the firing angle linearly by adding two ramp-comparator circuits. It has all the advantages of the ramp-comparator circuits and the phase-locked-loop circuits. The range of most of the existing firing circuits may not cover from 0° to 180° . The firing circuit can be adjusted from 0° to 175° so that the error of the firing circuit is 5° . By adjusting the free running frequency to shift the phase angle of the PLL output, the firing circuit can be adjusted from 2.5° to 177.5° so that the error of the firing circuit is 2.5° . Therefore, the error of the linear firing circuit may be reduced by half by changing the free running frequency of the PLL chip. Figure 55 shows the relationship of the free running frequency and the phase shift of the output frequency of an LM565 PLL chip. Actually, the PLL-based firing circuit may be adjusted from 0° to 180° with less than a 1° error. This error is caused mainly by the modulated frequency of the pulse driver and the turn-on time delay of the thyristor. All the error terms of the

input stages can be corrected by changing the free running frequency of the PLL chip to shift the phase of the output frequency. The designed PLL-based firing circuit does not have the error term [6] of $360^\circ/N$. The block diagram of a three-phase phase-locked-loop-based firing controller is illustrated in Figure 56. By changing

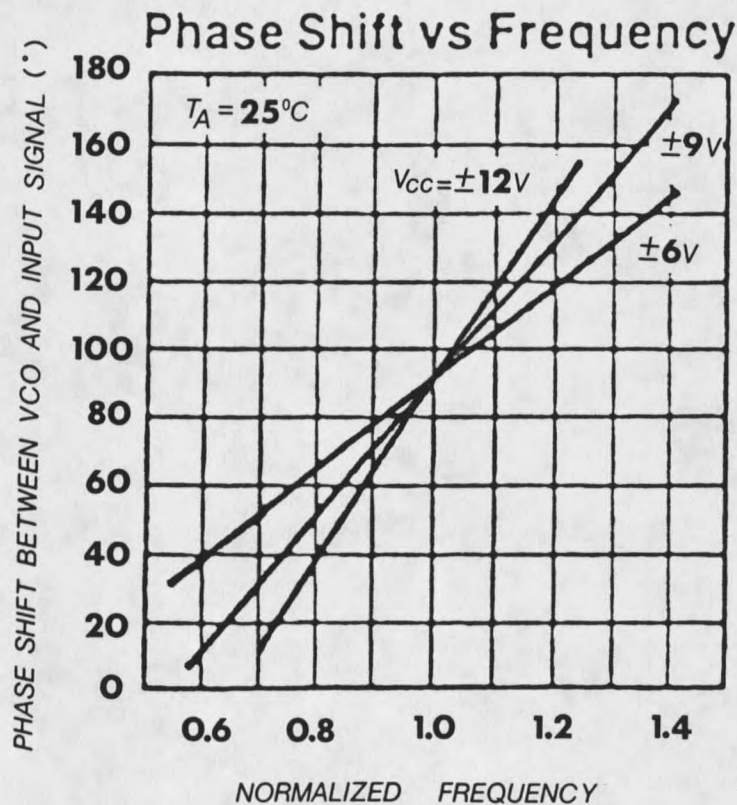


Figure 55. Phase shift versus frequency plot of LM565.[14]

the combinational logic circuit in Figure 56, the phase-locked-loop-based scheme can be used to control a three-phase AC voltage controller, an AC to DC three-phase converter and a DC to AC three-phase inverter. An AC to DC

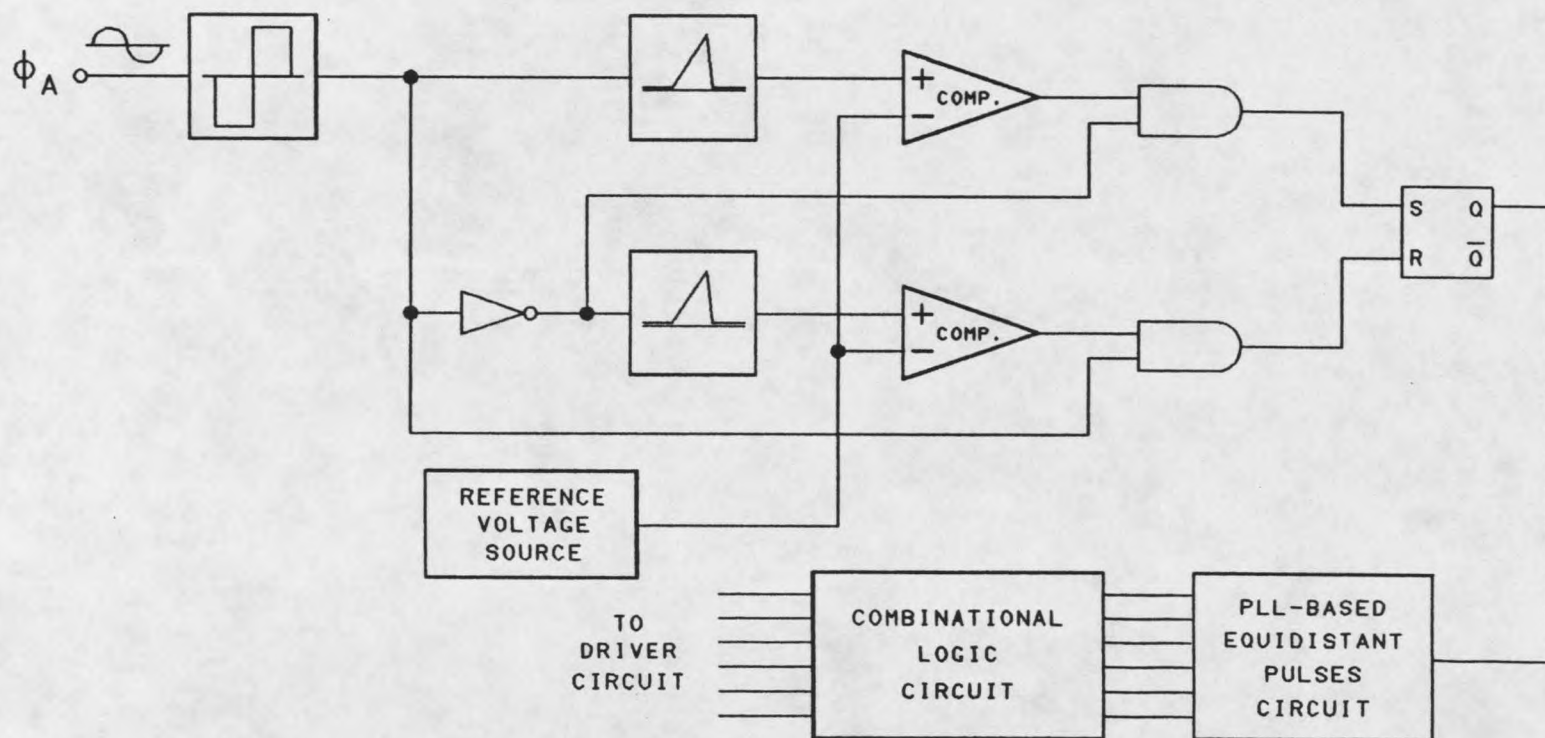


Figure 56. A block diagram of a three-phase phase-locked-loop-based firing controller.

converter has a 120° conduction angle with the range of the firing angle from 0° to 60° . A complete DC to three-phase inverter controller is shown in Figure 57. By changing the connections between the counter outputs and the set-reset Flip-flops in Figure 57, only three set-reset Flip-flops are needed for a three-phase voltage controller and each Flip-flop has 50% duty cycle. The design techniques of the PLL circuit [14] are discussed in Appendix C.

An Experiment of a PLL-Based DC to Three-Phase Inverter (PLLBTPIC)

The configuration of the experiment is the same as the one in Figure 7 in Chapter 2. A 26V power supply was used in the experiment. The complete PLLBTPIC circuit is wired on the breadboard. The outputs of the divide-by-six module were connected to the driver circuit of the RCBTPVC. The modulated frequency of the driver circuit was adjusted to 10kHz. The power supply voltages were the same as in the previous experiments. Two additional power supplies were connected to the circuit to supply $\pm 6V$. Referring to Sugandhi and Sugandhi [9], it is possible to trigger three thyristors at the same time and shortcircuit the power supply when the configuration of Figure 7 is used.

According to the experimental results, this configuration can handle only 0.3A when a balanced three-phase 130Ω load is used. When the supply voltage is higher than 40V, the thyristors have commutation problems and short circuit the

power supply. According to the thyristor data book, if the applied anode-to-cathode voltage increases the current rise time will decrease. If the maximum forward pulse current of the thyristor increases, the pulse turn-off time will increase. In other words, it takes a longer time to turn off the thyristor. As a result, more than three thyristors may turn on at the same time. The easiest way to solve this problem is to use the McMurray method and to force the thyristors to commute by using an LC network [9], [10], [11], [13], [15]. In chapter 2, the author mentions that the PSBTIPUC can be used to control a DC to three-phase inverter. However, Sugandhi and Sugandhi [9] suggest that a 120° conduction angle of the thyristors is better than 180° .

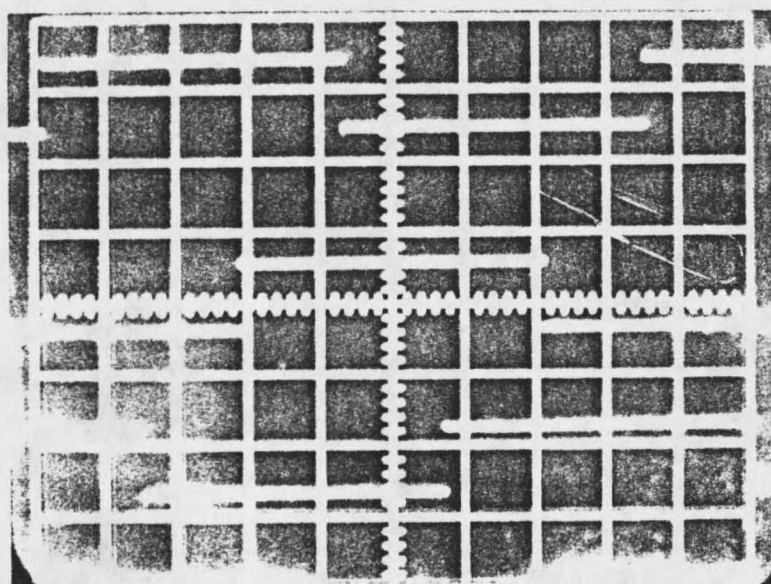


Figure 58. Measured three-phase output waveforms generated by PLLBTIPIC. Upper : 0° . Middle : 120° . Bottom : 240° .
Vertical : 50V/div. Horizontal : 2ms/div.

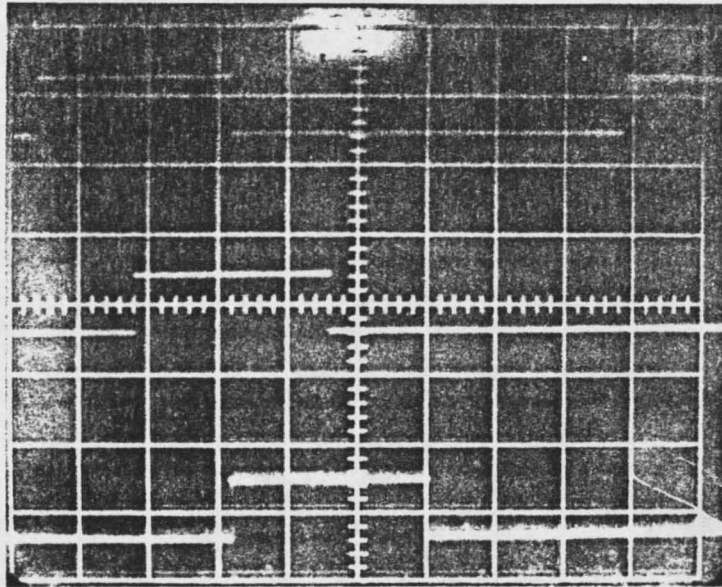


Figure 59. Measured the driver input signals.
Top : G1. Middle : G2. Bottom : G3.
Vertical : 5V/div. Horizontal : 2ms/div.

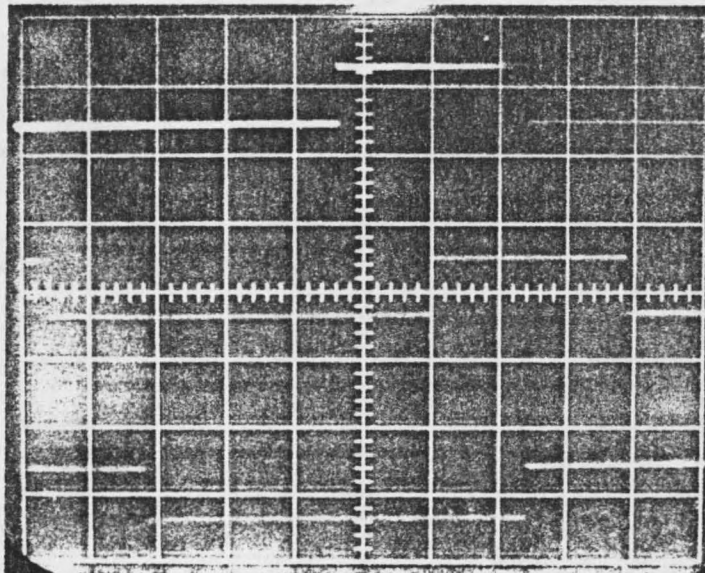


Figure 60. Measured the driver input signals.
Top : G3. Middle : G4. Bottom: G5.
Vertical : 5V/div. Horizontal : 2ms/div.

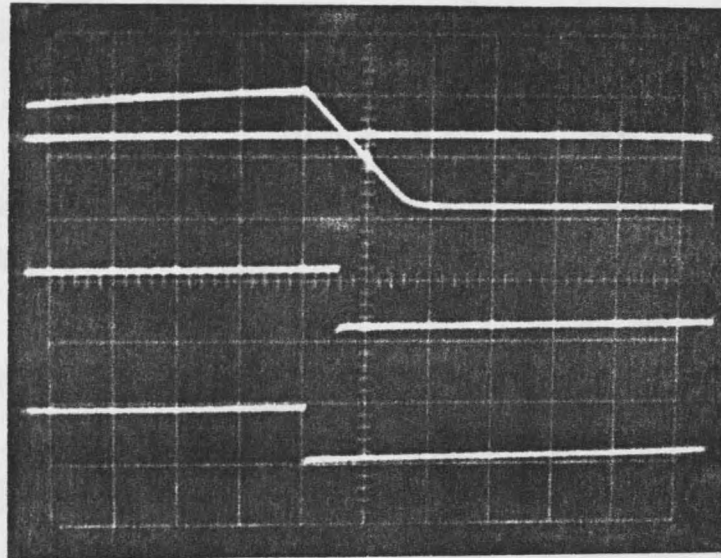


Figure 61. Measured the operation of the error blocking circuit. Top : ramp generator output. Vertical : 10V/div. The straight line : the reference voltage. Vertical : 10V/div. Top pulse : the error blocking output. Vertical : 5V/div. Bottom pulse : the comparator output. Vertical : 5V/div. Horizontal : 0.2ms/div.

conduction angle because it reduces the chance of commutation failure of the three-phase inverter. Actually, a PLL-based controller can be used to generate a three-phase output waveforms. Figures 59 and 60 show the driver signals at the outputs of the set-reset flip-flops of PLLBTPIIC. In chapter 3, the author uses an error blocking circuit. Figure 61 shows the operation of the error blocking circuit.

Experimental Results of the PLLBTPIIC

Figures 62 and 63 show the waveforms of the PLLBTPIIC with a balanced load of 130 Ω . Figure 64 shows the error of the

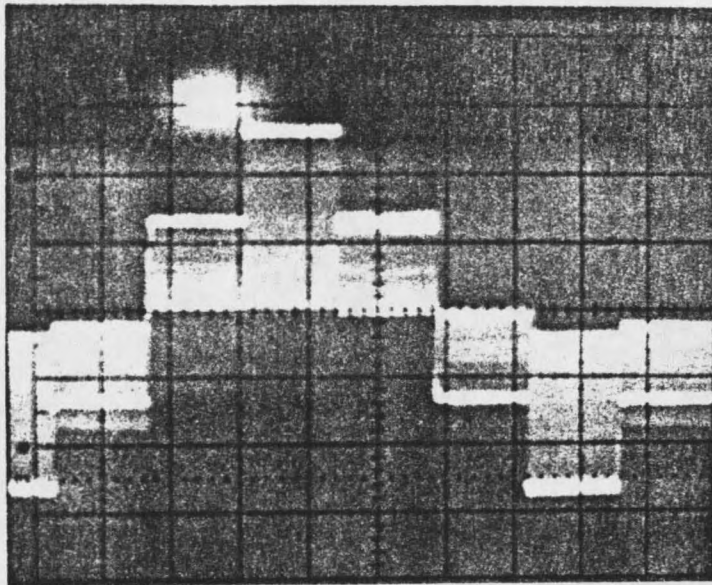


Figure 62. Measured waveforms across phase AB with a balanced load of 130Ω using the PLLBTIC.
Vertical : 10V/div. Horizontal : 2ms/div.

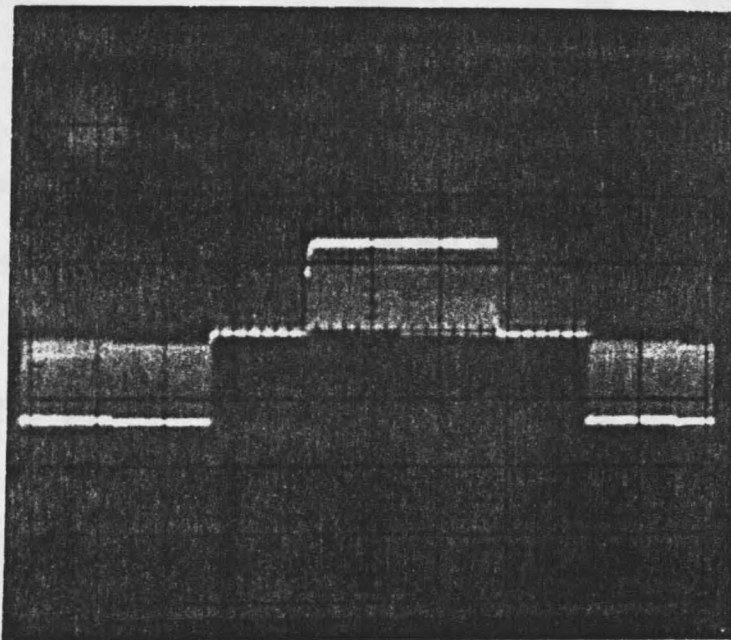


Figure 63. Measured waveforms across AN with a balanced load of 130Ω using the PLLBTIC.
Vertical : 10V/div. Horizontal : 2ms/div.

PLLBTPIC which is about 1° . By adjusting the free running frequency of the PLL, the error can be reduced by half because a 1° error is split to both ends. Therefore, the new range of the linear firing is from 0.5° to 179.5° . By adding the error of the modulated frequency, the range of the worst case linear firing should be from 0.86° to 179.14° for a 10kHz modulating frequency. However, the error of the modulated frequency is fixed and the thyristor has a turn-on time delay. In other words, the modulated frequency cannot keep increasing. The lowest obtainable error of the firing angle should be only the error caused by the modulated frequency and the time delay of the thyristor.

An Experiment of a PLL-Based Three-Phase Voltage Controller (PLLBTPVC)

The configuration of the experiment is the same as in Figure 8. The modulated frequency was 30kHz with a balanced load of 25Ω . In the last two chapters, the measured waveforms with the same loads are exactly the same because all the controllers designed by the author have the same driver circuits. Therefore, the author did not test the controller with different loads. In Figure 64, the error of the PLLBTPVC is about $1.13^\circ \pm 3\%$ error due to the tolerance of the oscilloscope at 180° .

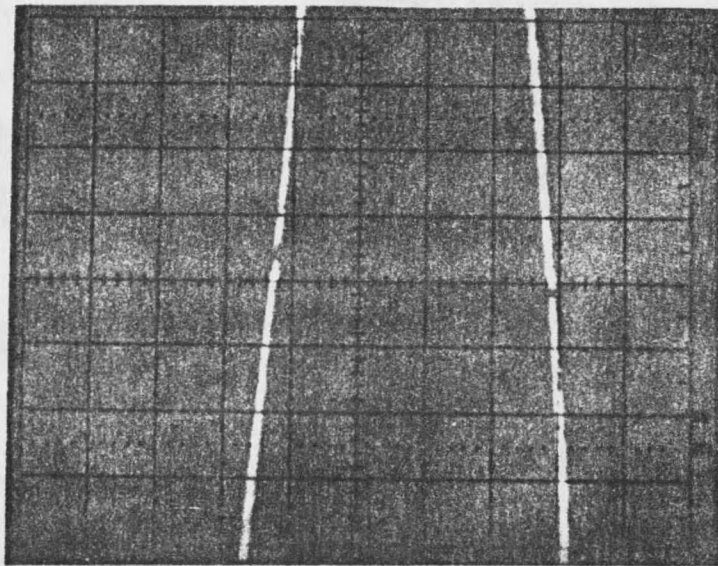


Figure 64. Measured waveforms across the load with a balanced load of 25Ω at $\alpha = 180^\circ$ using PLLBTPUC.
Vertical : 10V/div. Horizontal : 5ms/div.

Conclusions

With regard to the improvement of the scheme proposed by Simard and Rajagopalan [6], the following conclusions are drawn from the study and the experimental results reported in this chapter.

1. The advantages of phase-locked-loop-based three-phase controller (PLLBTPC):
 - a. Linear.
 - b. Less than 1° error can be achieved.
 - c. Very accurate.
 - d. All the outputs of the controller have the same error because of equidistant firing.
 - e. Needs only one input transformer to sense the line signal.

2. The disadvantages of PLLBTPC:

- a. Poor transient response.
- b. Misfiring, if the noise level is high enough to trigger the set-reset flip-flops and the D-type flip-flops of the PLL circuit the system will become extremely unstable.
- c. More expensive than PSBTPVC.
- d. Poor thermal stability. The currents of the constant current source chips change with temperature.

CHAPTER 5

DISCUSSION

Comparison of Three Different Controllers

Table 2 shows the comparison of three different controllers.

	PSBTIVC	RCBTIVC	PLBTIVC
Accuracy	Low	High	Very high
Circuit complexity	Simple	Very complex	Complex
Complexity of calibration	Simple	Very complex	Complex
Cost	Cheap	Most expensive	More expensive
Error (per channel)	$\leq 5.12^\circ$	$\leq 3.22^\circ$	$\leq 1.13^\circ$
Firing angle display	Oscilloscope	DVM	DVM
Linearity	Nonlinear	Very linear	Very linear
Misfiring problem	No	Yes (solvable)	Yes (solvable)
Number of input transformers	1	3	1
Size	Small	Large	Medium
Thermal instability	Low	Very high	Very high

Table 2. Comparison of three different controllers.

Comments

All the controllers designed by the author have been for 60Hz machines. If the line frequency is changed the accuracy of the controllers will no longer hold. A thermal compensation circuit is needed for all the ramp generators since the current source is sensitive to the temperature. The variation of the line frequency has been a difficult problem for engineers. For a non-60Hz based controller, like the one proposed by Simard and Rajagopalan [6], the PLL is used to lock on the input frequency. However, it is impossible to predict the frequency of the next cycle. Therefore, for the long run, it is very difficult to tell whether non-60Hz based controllers are better than 60Hz based controllers.

CHAPTER 6

CONCLUSION

The design of three different firing angle controller circuits, including a phase-shifter-based firing angle controller, a ramp-comparator-based firing angle controller and a phase-locked-loop-based firing angle controller, is presented in this thesis. The following basic conclusions are drawn from this research.

1. The experimental phase-shifter circuit proposed by Le and Berg [1] has a maximum phase shift of 171.22° at 60KHz and the experimental simplified version of phase-shift circuit designed by the author has a maximum phase shift of 174.88° at 60KHz. It shows the improvements of the new version compared to the old version.
2. Overdriving the ramp generator will result in a low $V_{ce(sat)}$. It helps to reduce the error of the ramp generator circuit.
3. The error blocking circuit helps to block the discharging error of the ramp generator.
4. The error analysis techniques used in this thesis have the advantages of revealing which part of the circuit may introduce the largest error terms so that the

- designer can implement changes to reduce the error.
5. Computer simulation can show the user only a rough response of the circuit. Moreover, the parameters of a transistor vary with transistors. Therefore, the worst-case parameters have to be used by the designer. The simulated SPICE results of $V_{ce(sat)}$ of 2N2222 are lower than that of the experimental results because the parameters of the simulated model of 2N2222 are based on the typical values from the specification sheets. Usually, the typical values from the specification sheets are only the nominal values of the transistors. Hence, the experimental results will not, in general, be the same as the SPICE simulated results.
 6. The ramp generators used in both RCBTPVC and PLLBTHVC have no built-in thermal compensation, and they are sensitive to temperature. It is necessary to add an additional thermal compensation circuit to each ramp generator if the controller is not operated at room temperature.
 7. The PLLBTPVC has only two ramp generators. Therefore, the procedures of calibration are less complex than that of RCBTPVC. The free running frequency of the PLL chip can be adjusted to reduce the error of the PLLBTPVC.
 8. The experimental results show that the PLLBTPIC has no

problem to control a low power three-phase inverter but it is a problem to control a high power three-phase inverter. This is because the three-phase inverter has commutation problems. If the maximum forward pulse current of the thyristor increases the pulse turn-off time of the thyristor will increase. Therefore, it takes a longer time to turn off the thyristor and natural commutation can no longer commutate the thyristors of the higher power inverter. Hence, a forced commutation circuit, like the McMurray inverter circuit, must be used in order to commutate the thyristors of the inverter.

Suggested Future Work

The work presented in this thesis can be further extended in the following directions.

1. The reference voltage of the ramp-comparator can be replaced by a selectable voltage source and the firing angle shown directly. Therefore, the user can select the desired firing angles to control the thyristors without using an oscilloscope or the DVM and trimming the potentiometer of the controller.
2. To use the circuit suggested by National Semiconductor [14] or by Gray and Meyer [16], a temperature-independent current source can be designed to overcome the problem of changing the environmental temperature.

3. The use of low offset comparators may improve the accuracy of the controller.

REFERENCES CITED

REFERENCES CITED

- [1] L. X. Le and G. J. Berg, 'Firing Circuit for a Three-Phase SCR Voltage Controller', IEEE Trans. Ind. Electron., vol. IE-31, no.4, pp.389-390, Nov. 1984.
- [2] B. Ilango, R. Krishnan, R. Subramanian, and S. Sadasivan, 'Firing Circuit for Three-Phase Thyristor-Bridge Rectifier', IEEE Trans. IECI, vol. IECI-25, no.1, pp.45-49, Feb. 1978.
- [3] R. Arockiasamy and S. Doraipandy, 'A Novel Scheme to Obtain Voltage Controlled Time Delay Suitable for Thyristor Control', IEEE Trans. IECI, vol. IECI-23, no.1, pp.27-31, Feb. 1976.
- [4] Pei-chong Tang, Shui-shong Lu and Yung-chun Wu, 'Microprocessor-Based Full-Wave Thyristor Dual Converter', IEEE Trans. IE, vol. IE-29, no.1, pp.67-73, Feb. 1982.
- [5] Ali Mirbod and Ahmed El-amawy, 'A General-Purpose Microprocessor-Based Control Circuit for a Three-Phase Controlled Rectifier Bridge', IEEE trans. IE, vol. IE-33, no.3, pp.310-317, Aug. 1986.
- [6] Remy Simard and U. Rajagopalan, 'Economical Equidistant Pulse Firing Scheme for Thyristorized DC Drives', IEEE Trans. IECI, vol. IECI-22, no.3, pp.425-429, Aug. 1975.
- [7] Thadiappan Krishnan and Bellamkonda Ramaswami, 'A Fast-Response DC Motor Speed Control System', IEEE Trans. IA, vol. IA-10, no.5, pp.643-651, Sept./Oct. 1974.
- [8] Silicon Controlled Rectifier Designers Handbook, Westinghouse Electric Corporation, Semiconductor Division, Sept. 1970.
- [9] R. K. Sugandhi and K. K. Sugandhi, Thyristors: Theory and Applications, Wiley Eastern Limited, New Delhi, India, 1984.

- [10] G. K. Dubey, S. R. Doradla, A. Joshi and R. M. K. Sinha, Thyristorised Power Controllers, New Delhi, India, 1986.
- [11] S. B. Dewan and Straughen, Power Semiconductor Circuits, John Wiley & Sons, Inc., 1975.
- [12] Tsui Wai, Digital Circuit : Implementation and Application, Wah Mei Science & Technology Press, Hong Kong, 1987.
- [13] SCR Technology, edited by Sheung Tam School of Electric Factory, Chungking, The People's Republic of China, 1984.
- [14] Linear Databook, National Semiconductor Corporation, 1982.
- [15] Paresh C. Sen and G. Premchandran, 'Improved PWM Control Strategy for Inverters and Induction Motor Drives', IEEE Trans. on Ind. Electron., vol. IE-31, no.1, Feb. 1984.
- [16] Paul R. Gray and Robert G. Meyer, Analysis and Design of Analog Integrated Circuit, 2nd edition, John Wiley & Sons, Inc., pp.284-289, 1984.

APPENDICES

APPENDIX A

Derivation of the Phase Shifter Circuit
Transfer Function

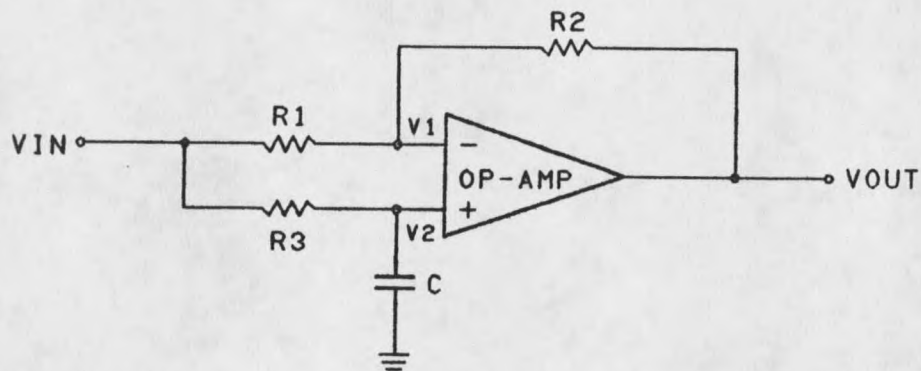


Figure 65. A phase shifter circuit.

Consider the circuit in Figure 65. By applying Kirchhoff's current law to nodes V1 and V2, we have

$$\frac{V_{IN} - V_1}{R_1} = \frac{V_1 - V_{OUT}}{R_2} \quad (1)$$

$$V_2 = V_{IN} \left(\frac{1 / j\omega C}{R_3 + 1 / j\omega C} \right) \quad (2)$$

The basic output voltage of the operational amplifier is

$$A(V_2 - V_1) = V_{OUT} \quad (3)$$

where A is the open-loop gain of the operational amplifier and ω is the angular frequency of the input signal in

radians per second. By rearranging (1) and (2) and substituting into (3), we have

$$A \left(\frac{V_{IN}}{1 + j\omega \cdot R_3 \cdot C} - \frac{V_{IN} \cdot R_2}{R_1 + R_2} - \frac{V_{OUT} \cdot R_1}{R_1 + R_2} \right) = V_{OUT}$$

Assuming $A \rightarrow \infty$ and setting $R_1 = R_2$, we have

$$H(j\omega) = \frac{V_{OUT}}{V_{IN}} = \frac{1 - j\omega \cdot R_3 \cdot C}{1 + j\omega \cdot R_3 \cdot C}$$

The gain $H(\omega)$ and phase angle θ of the phase shifter circuit, therefore, may be written

$$H(\omega) = \frac{\sqrt{1 + (\omega R_3 C)^2}}{\sqrt{1 + (\omega R_3 C)^2}} = 1$$

$$\theta = -2 \arctan(\omega R_3 C)$$

APPENDIX B

SPICE Program Listing of Ramp Generator Simulation

```

RAMP CIRCUIT SIMULATION
VCC 1 0 DC 5V
VIN 4 0 PULSE(0.5 4.5 0 0 0 8.3MS 16.6MS)
R1 4 3 27K
Q1 2 3 0 MOD1
C1 2 0 4.7UF
ICOM 1 2 DC 0.00101524
.PRINT TRAN V(4) V(3) V(2)
.MODEL MOD1 NPN IS=3.108E-15 XTI=3 EG=1.11
+UAF=131.5 BF=217.5 NE=1.541 ISE=190.7E-15
+IKF=1.296 XTB=1.5 BR=6.18 NC=2 ISC=0 IKR=0
+RC=1 CJC=14.57E-12 VJC=.75 MJC=.3333 FC=.5
+CJE=26.08E-12 VJE=.75 MJE=.3333 TR=51.35E-9
+TF=451E-12 ITF=.1 VTF=10 XTF=2
.TRAN 0.01MS 25.9MS UIC
.OPTIONS LIMPTS=3000
.END
[EOB]

```

Figure 66. SPICE program listing of ramp generator simulation.

Note: The transistor model parameters are obtained from the
 PSPICE transistor library for 2N2222.

APPENDIX C

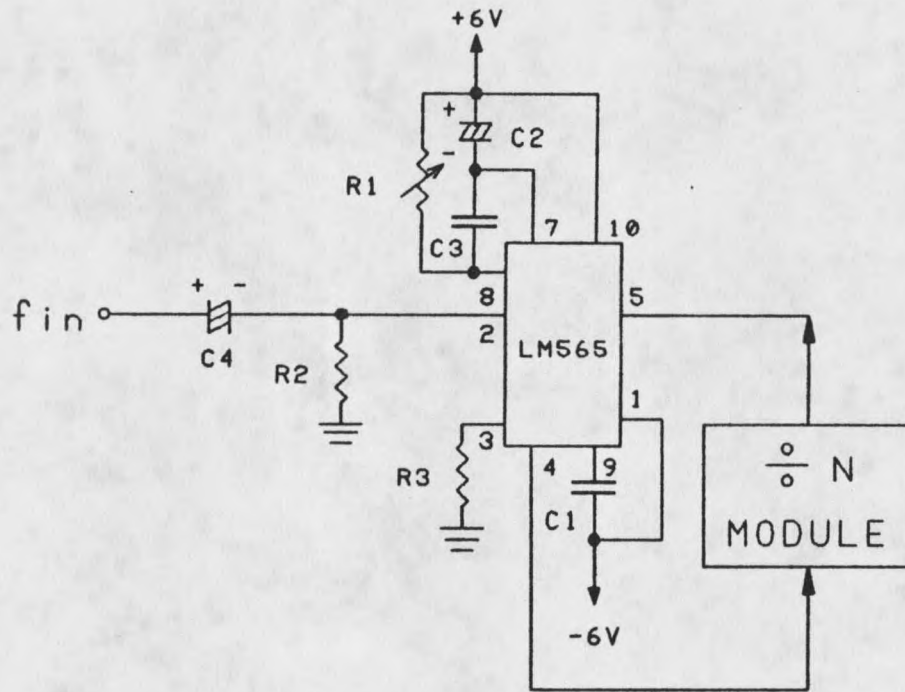
Phase-Locked-Loop Circuit Design Using LM565 Chip

Figure 67. A LM565 phase-locked-loop circuit.

From National Semiconductor [14] the free running frequency of the PLL as shown in Figure 67 is given by

$$f_o \approx \frac{0.3}{R1 \cdot C1} \quad (4)$$

The loop gain of the PLL is given by

$$A1 = K_o K_d (1/\text{sec}) \quad (5)$$

where

$$K_o = \text{sensitivity} \left(\frac{\text{radians/sec}}{\text{volts}} \right) ,$$

$$K_d = \text{phase detector sensitivity} \left(\frac{\text{volts}}{\text{radian}} \right)$$

and

$$K_o \cdot K_d = \frac{33.6 f_o}{V_c} \quad (6)$$

where f_o is the VCO frequency in Hz and V_c is the total supply voltage to the PLL circuit.

The hold in range of the loop of the PLL chip is given by

$$f_h = \pm \frac{8 f_o}{V_c} . \quad (7)$$

For circuit stability,

$$1 / R_{int} \cdot C_2 > K_o \cdot K_d \quad (8)$$

where R_{int} is the internal resistance between pin 10 and pin 7 of the LM565 chip.

MONTANA STATE UNIVERSITY LIBRARIES



3 1762 10144995 5

