DESIGN, FABRICATION, AND TESTING OF THE VAN DER PAW PIEZORESISTIVE STRUCTURE FOR PRESSURE SENSING

by

Robert Douglas Cassel

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APPROVAL

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Robert Douglas Cassel

This thesis has been read by each member of the thesis committee and has been found to be satisfactory regarding content, English usage, format, citations, bibliographic style, and consistency, and is ready for submission to the Division of Graduate Education.

Dr. Ahsan Mian

Approved for the Department of Mechanical and Industrial Engineering

Dr. Christopher Jenkins

Approved for the Division of Graduate Education

Dr. Carl A. Fox, Vice Provost

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ABSTRACT

The project characterizes a piezoresistive sensor under variations of both size and orientation with respect to the silicon crystal lattice for its application to MEMS pressure sensing. The sensor to be studied is a four-terminal piezoresistive sensor commonly referred to as a van der Pauw (VDP) structure. The VDP sensor is used primarily in sheet resistance measurements, but has also been determined to be useful in determining the stress components at a point on (100) and (111) silicon wafer surfaces. In a previous study, our team has determined the relation between the biaxial stress state at a point and the piezoresistive response of the VDP by combining the VDP resistance equations with the equations governing silicon piezoresistivity. It was found that the theoretical sensitivity of the VDP sensor is over three times higher than the conventional filament type resistor. With MEMS devices being used in applications which continually necessitate smaller size, understanding the effect of size on VDP performance is important.

In order to test the validity of the theoretical calculations which were done by our group, appropriate devices were manufactured on a (100) silicon test wafer. The wafer was designed to have numerous pressure sensitive diaphragms which can reliably sustain a pressure difference of approximately 50kPa. Each diaphragm was doped with a VDP or other sensor designed to test the sensitivity of the VDP vs. a certain parameter. These parameters include size, misalignment, and diaphragm position, in addition to the comparison of sensitivity to conventional sensor types. A test strip was also included in the design in order to determine an empirical relationship between stress and resistance.

In testing the VDP devices for comparison with conventional sensor types, it was found that the VDP devices had a linear response as expected, were the most sensitive, and provided a number of additional advantages. Specifically, the VDP device allows for significant miniaturization, because its resistance value is independent of size, and the measurement technique is independent of line resistance. The simple geometry of the VDP also simplifies fabrication.

INTRODUCTION

Stress Measurement

The measurement of strain is often desired in many engineering applications. To meet that need, a number of strain measurement techniques have been developed. The most direct techniques detect displacement changes. Displacement measurement can directly lead to the strain measurement given a total original length that can be used to normalize the displacement change, resulting in a strain calculation. Another method for strain determination utilizes a fundamental constitutive relationship between the stress and strain in a material, commonly referred to as Hooke's Law,

$$\sigma = \varepsilon \cdot E \tag{1}$$

Equation 1 is Hooke's Law for an isotropic material, where σ is stress in units of [MPa], ε is dimensionless strain and E is the material stiffness, or Young's Modulus, in units of [MPa], which remains unchanged with respect to direction. Using this fundamental relationship, with the knowledge of the material constant, E, strain measurements can be determined through stress measurement, and vice versa.

Strain Gages

A simple method for strain measurement is done using an extensometer. An extensometer is a device which simply attaches to a material sample and measures the displacement, using a dial or electronic measurement, between two points on that sample

as it is strained. Extensometers are typically used in uniaxial tension tests where they are attached at two points on the sample being tested, and as the material elongates, the extensometer elongates equally. This simple strain measurement method has a number of limitations, however. To be an accurate measure of strain, it is necessary that the strain be uniform throughout the length between the points being measured, which is typically not the case in tensile testing. Extensometers also tend to slip, and can create stress concentrations if not used properly, causing premature failure.

Another more reliable method of strain sensing is the conventional strain gage. Strain gages are thin metallic films that are mounted on a material sample, and that elongate with the sample when mounted properly. The resistance of these strain gages can be measured. When the material is elongated, the gage is simultaneously and equally strained, causing an elongation of the gage along with a slight reduction in cross-sectional area due to the Poisson effect. The effect on the gage is illustrated in Figure 1

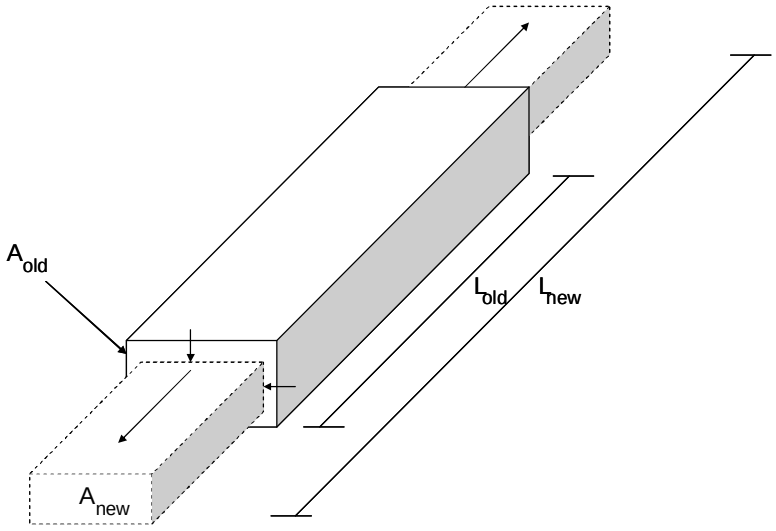


Figure 1: Illustration of area reduction and length increase in strained gage wire.

The resistance of a foil is given by

$$R = \rho \frac{L}{A} \tag{2}$$

Where L is the length in [cm] of the resistive element, A is the cross-sectional area in [cm^2], and ρ is the resistivity in [Ω-cm]. As the material elongates, L increases and A decreases, causing a cumulative increase in resistance, R. In order to maximize the sensitivity of a strain gage, a conventional method of using small wires which double back on themselves as shown in Figure 2 is used.

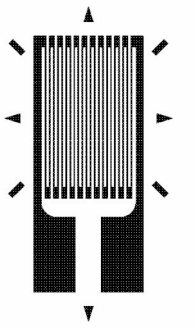


Figure 2: Typical metal foil strain gage illustrating small wires doubling back on themselves.

Because the change in A is small under strain, while L is relatively larger, doubling back as shown increases the resistance change by emphasizing the change in length over the change in cross-sectional area. Even with this modification, the resistance change is typically very small under small strains. To enhance the performance of the strain gage, four gages are often arranged in a wheatstone bridge circuit which can more accurately measure resistance differences between two gages. A wheatstone bridge circuit can be seen in Figure 3.

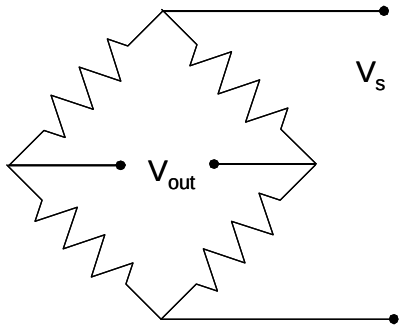


Figure 3: Typical wheatstone bridge circuit used to enhance strain gage sensitivity.

Piezoresistive Strain Gage

The conventional strain gage suffers from both sensitivity issues, and scalability issues. Because the conventional strain gage uses an indirect relationship to stress through geometry to produce resistance change, it is relatively insensitive. Piezoresistive strain gages improve on sensitivity by operating directly proportional to the stress in the material [1].

Metals and other crystalline materials typically occur in polycrystalline form. However, when these materials are found or produced in crystalline form, a lattice structure exists which can result in anisotropic properties. The polycrystalline form of these materials is isotropic in the macroscopic sense. While an individual crystal in a polycrystalline material may exhibit anisotropic properties, these properties are counteracted by other crystals in the macroscopic sense, eliminating any net anisotropy. In crystalline semiconductor materials, when the crystal lattice is strained, the interatomic spacings change, enhancing or reducing the ability of electrons to move through the conduction band. When a stress produces a strain on the crystal lattice in a semiconductor material, such as silicon or germanium, the resistivity of that material changes [2].

Specifically, when stress is applied, strain energy is input, which reduces the band gap between the conduction and valence band in the semiconductor, enhancing conductivity. This phenomenon is called piezoresistivity, and it can produce a much larger resistance change for a given strain compared to that of a conventional strain gage. It should be noted that it has been shown that polycrystalline silicon can also exhibit the effect to a lesser degree [3]. This increased sensitivity can be reflected in the gage factor of the strain gages. The gage factor is the normalized resistance change of the gage divided by the strain.

$$GF = \frac{\Delta R / R_G}{\varepsilon} \tag{3}$$

A conventional strain gage typically has a gage factor of approximately 2. Piezoresistive strain gages can have a gage factor of approximately 100 [4]. The disadvantages associated with this increase in sensitivity are an increased sensitivity to temperature effects, an increase in fragility due to the use of brittle silicon, and an increased cost due to manufacturing complexity.

A piezoresistive strain gage is created on a silicon substrate using microelectronic manufacturing processes. Dopants in the silicon are used to improve the conductivity and piezoresistivity of the doped regions, and also to achieve electrical isolation. These dopants can be either p or n-type, and because the silicon substrate is typically lightly doped either p or n, electrical isolation can be achieved by doping a region with an opposite type dopant. That is, an n-type silicon substrate doped in a small region with p-type dopants will form a reversed bias p-n junction, electrically isolating the region. In

this way, piezoresistive elements can be created on the silicon surface in any specified shape or reasonable size. Typical piezoresistive strain gages are shaped similar to that of the conventional strain gage in Figure 2.

Piezoresistivity for Silicon Sensors

Piezoresistivity is a change in resistivity resulting from a change in strain. For silicon, general Hooke's law accurately models the relationship between stress and strain.

$$\sigma_{ij} = E_{ijkl}\varepsilon_{kl} \tag{4}$$

where indicial notation has been used. Replacing i,j,k, and l with 1,2, or 3 corresponds to the x,y,z coordinate directions. σ is stress, E is Young's Modulus, and ε is strain.

For a general conductor, the relationship between current and electric field strength is given by

$$\overline{\mathrm{E}}_i = \rho_{ij} J_j \tag{5}$$

where E with overbar is electric field strength in [V/cm], and is distinguished from Young's Modulus by the overbar. J is current in [A/cm^2], and ρ is the isotropic resistivity of the conductor in [Ω-cm].

For an unstressed, isotropic conductor in silicon, resistivity is given by

$$\rho_{ij}^{'} = \rho\delta_{ij} \tag{6}$$

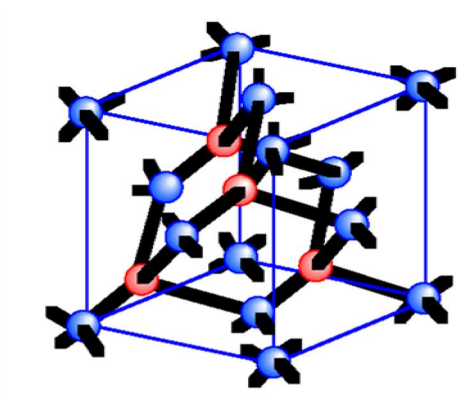
where ρ is the isotropic resistivity of the conductor, δ_{ij} is the Kronecker delta, and $\rho_{ij}^{'}$ is the second order resistivity tensor. The prime represents the coordinate system of the wafer, as will be discussed. If the conductor is piezoresistive, the second order resistivity

tensor will change given a change in stress state, which is also a second order resistivity tensor. The resulting equation is modified as follows,

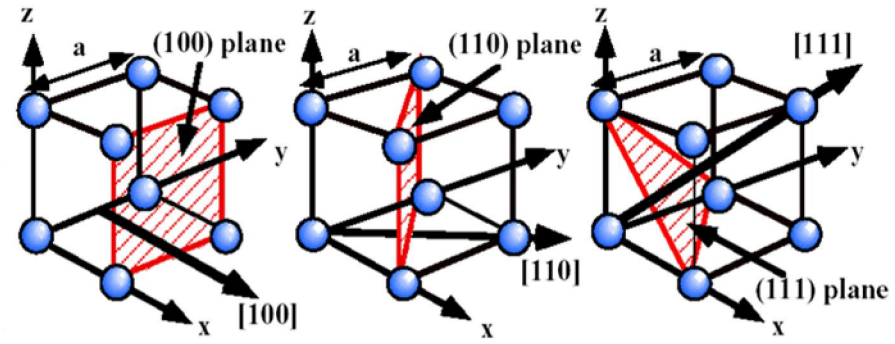
$$\rho_{ij}^{'} = \rho\delta_{ij} + \rho\pi_{ijkl}^{'}\sigma_{kl}^{'} \tag{7}$$

where $\pi^{'}_{ijkl}$ is the fourth order piezoresistivity tensor which characterizes the relationship between the stress tensor, $\sigma^{'}_{kl}$, and the resitivity tensor. Note that repeated indices indicate summation. Equation 7 is for a fully anisotropic piezoresistive, conductive material in an arbitrary coordinate system. [5]

Silicon substrates, commonly referred to as wafers, are single crystals with a distinct crystal lattice. The crystal lattice is a result of the tetrahedral bonding of silicon atoms, which leads to a cubic crystal lattice containing three distinct crystallographic planes, as shown in Figure 4. [6]



a)



b)

Figure 4: a) Diamond silicon crystal structure b) Three planes in the silicon crystal defined by Miller indices [4]

A silicon wafer is typically either (100) or (111) type, meaning a (100) or (111) plane is the wafer surface. It was later determined that (100) wafers would be used in device production, so the following discussion will be limited to (100) wafers only.

The macroscopic result of the distinct crystallographic planes is anisotropy in the material properties, including piezoresistivity. The piezoresistivity tensor for silicon, π'_{ijkl}, can be further simplified with the symmetry assumptions inherent in a cubic material. Many of the terms in the tensor can be eliminated, because the crystal lattice is highly symmetric.

The piezoresistivity tensor can be transformed from an unprimed coordinate system to a primed coordinate system by

$$[\pi'] = [T][\pi][T]^{-1} \tag{8}$$

where T is the transformation matrix defining coordinate rotation given by

$$[T]=\begin{bmatrix} a_{11}^2 & a_{12}^2 & a_{13}^2 & 2a_{11}a_{13} & 2a_{12}a_{13} & 2a_{11}a_{12} \\ a_{21}^2 & a_{22}^2 & a_{23}^2 & 2a_{21}a_{23} & 2a_{22}a_{23} & 2a_{21}a_{22} \\ a_{31}^2 & a_{32}^2 & a_{33}^2 & 2a_{31}a_{33} & 2a_{32}a_{33} & 2a_{31}a_{32} \\ a_{11}a_{31} & a_{12}a_{32} & a_{13}a_{33} & a_{11}a_{33}+a_{31}a_{13} & a_{12}a_{33}+a_{32}a_{13} & a_{11}a_{32}+a_{31}a_{12} \\ a_{21}a_{31} & a_{22}a_{32} & a_{23}a_{33} & a_{21}a_{33}+a_{31}a_{23} & a_{22}a_{33}+a_{32}a_{23} & a_{21}a_{32}+a_{31}a_{22} \\ a_{11}a_{21} & a_{12}a_{22} & a_{13}a_{23} & a_{11}a_{23}+a_{21}a_{13} & a_{12}a_{23}+a_{22}a_{13} & a_{11}a_{22}+a_{21}a_{12} \end{bmatrix} \quad (9)$$

and a_{ij} are direction cosines defined by

$$a_{ij} = \cos(x_i^{'}, x_j) \quad (10)$$

and $x_i^{'}$ and x_j are the primed and unprimed coordinate axes respectively. [7] It has been determined by Bittle et al. [8] that the unprimed piezoresistivity tensor, π, is given by,

$$[\pi]=\begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{bmatrix} \quad (11)$$

which has 3 independent terms. By operating on the unprimed piezoresistivity tensor given in Eq. 11 with the transformation tensor, T, given in Eq. 9, in the fashion of Eq. 8, the primed piezoresistivity tensor can be obtained. The crystallographic axes in a (100) wafer, and the relation between the unprimed and primed coordinate systems are shown in Figure 5. Also shown is the double primed coordinate system, which is that of the sensing device.

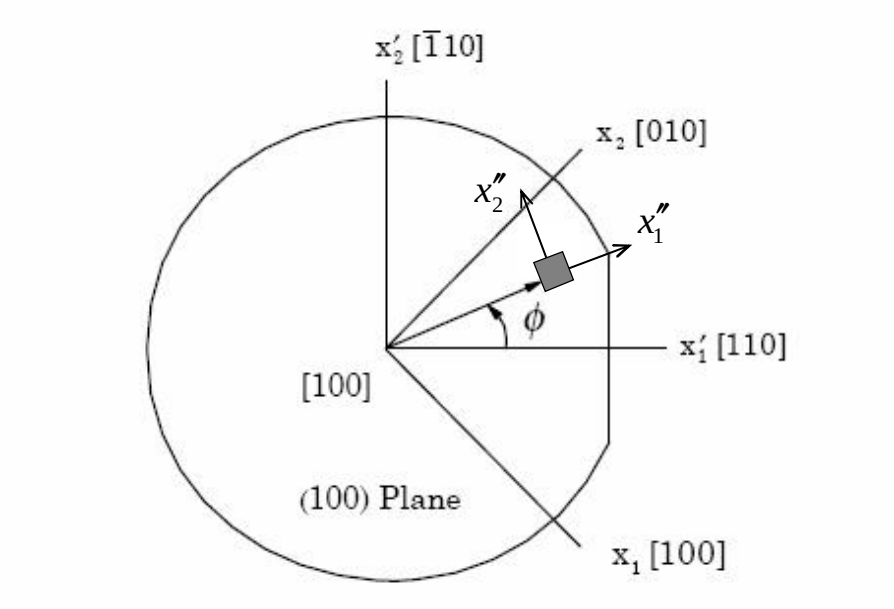


Figure 5: Crystallographic axes in relation to wafer axes and device axes for a (100) wafer [9]

It can be seen that a 45° rotation is required to obtain the appropriate piezoresistivity tensor for the wafer axes. Performing this rotation, the resultant equations for resistivity are

$$\rho_{11}^{'} = \rho\left[1 + \frac{\pi_{11} + \pi_{12} + \pi_{44}}{2}\sigma_{11}^{'} + \frac{\pi_{11} + \pi_{12} - \pi_{44}}{2}\sigma_{22}^{'} + \pi_{12}\sigma_{33}^{'} + \alpha T\right] \tag{12}$$

$$\rho_{22}^{'} = \rho\left[1 + \frac{\pi_{11} + \pi_{12} - \pi_{44}}{2}\sigma_{11}^{'} + \frac{\pi_{11} + \pi_{12} + \pi_{44}}{2}\sigma_{22}^{'} + \pi_{12}\sigma_{33}^{'} + \alpha T\right] \tag{13}$$

$$\rho_{12}^{'} = \rho\left[(\pi_{11} + \pi_{12})\sigma_{12}^{'}\right] \tag{14}$$

Note that a temperature term has been added due to the temperature dependence exhibited by silicon piezoresistive devices. Under testing this term will not vary, so it will be excluded in further use of Eqs. 12-14. The σ_{33} term will also be omitted, as out-of-

plane stresses will be neglected in theoretical development and testing of the devices. Eqs. 12-14 are used in the characterization of conventional piezoresistive strain gages.

Pressure Sensing

There are many current applications for pressure sensing devices. Automotive applications include seat pressure sensing to activate airbags, tire pressure sensing, pressure sensing in brake systems, and increasingly in ergonomic and safety systems [10, 11]. Pressure sensing is often used in other industries as well, with growing necessity for size reductions.

Numerous methods exist for pressure sensing in air. Capacitive pressure sensing utilizes the displacement of a fixed plate under pressure to modify the capacitance of a system. Many devices operate on the flexure of a plate diaphragm, as shown in Figure 6 and the associated displacement or strains to measure pressure. Optical sensors measure the displacement of the diaphragm, which corresponds to pressure. Conventional strain gages and piezoresistive strain gages measure the strain in the diaphragm, which can be correlated to pressure.

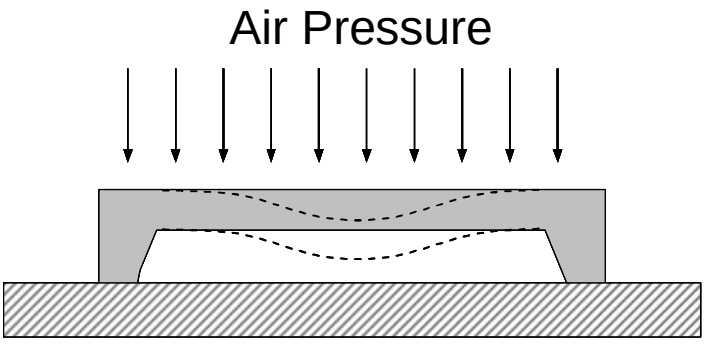


Figure 6: Plate diaphragm illustrating plate deflection under a vacuum condition within the diaphragm.

VAN DER PAUW PIEZORESISTIVE PRESSURE SENSING

In a typical piezoresistive pressure sensor, a diaphragm as shown in Figure 6 is used, along with a conventional piezoresistive strain gage which can be a serpentine structure, or a simple rectangular structure, typically forming a wheatstone bride configuration. There are a number of complications that arise from the use of these device types, however. The most notable is the ability to miniaturize the devices. It is typically desired to reduce the device size, as the piezoresistive equations are only valid for a uniform stress field. Because standard silicon etch techniques produce rectilinear features, pressure diaphragms are commonly square, and as such, have a significantly varying stress field over the diaphragm. The devices used on such diaphragms must be small enough such that the assumption of stress uniformity is valid. The resistor devices must also be large enough such that measurement errors are small. Furthermore, future MEMS applications necessitate smaller overall sensor size, which further requires piezoresistive device size reductions.

The van der Pauw (VDP) device structure as a pressure sensing device has been developed as an alternative to these conventional piezoresistive structures to provide a device that has a sensitivity which does not change with size variations, and has the added benefit of enhanced sensitivity over conventional piezoresistive structures. This enhanced sensitivity provides for miniaturization while maintaining small measurement errors.

The feasibility of the VDP device as a pressure sensor is easily verified. The van der Pauw theorem, developed by J.J. van der Pauw [12, 13] is commonly used to measure

isotropic conductivity. Typically this structure is a simple 2D square conductor device as shown in Figure 7, however, van der Pauw's theorem holds for any arbitrary conductive surface, and the theory has been extended for any square region of piezoresistive material [5, 14].

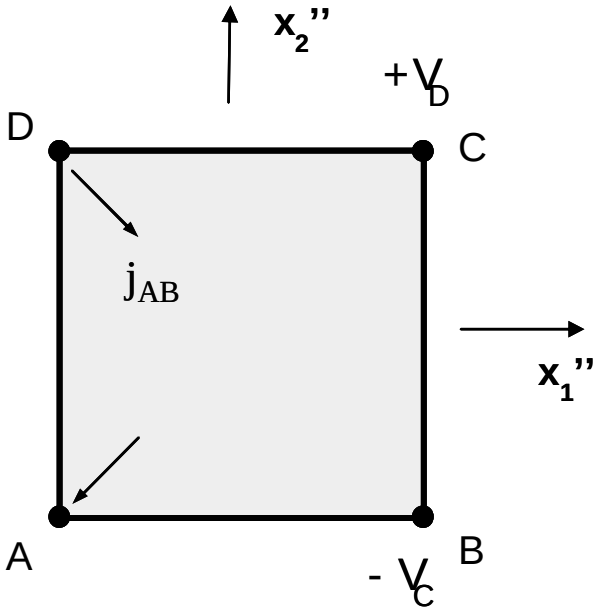


Figure 7: The van der Pauw (VDP) device structure

A current is passed through two terminals of the structure, A and B in Figure 7, while the voltage difference between the remaining two terminals, C and D in Figure 7, is measured. Dividing the voltage difference by current yields what is defined as a "resistance". This resistance will change based on the stress state in the device material, and in that way, can be used as a stress sensor. The device can also be mounted on a pressure diaphragm for pressure sensing, just as the conventional serpentine resistor structure is.

Passing current through terminals A and B, and measuring the voltage difference across D and C gives $R_{AB,CD}$. For the square VDP structure in Figure 7, $R_{BC,DA}$ can be defined also.

$$R_{AB,CD} = \frac{V_D - V_C}{j_{AB}}, R_{BC,DA} = \frac{V_A - V_D}{j_{BC}} \tag{15}$$

Van der Pauw's theorem for an isotropic conductor [12,13] states

$$\exp\left(-\frac{\pi t R_{AB,CD}}{\rho}\right) + \exp\left(-\frac{\pi t R_{BC,DA}}{\rho}\right) = 1 \tag{16}$$

where ρ is the isotropic resistivity of the conductor, and t is the conductor thickness. For the rotationally symmetric square pictured in Figure 7, $R_{AB,CD}$ and $R_{BC,DA}$ are the same. Eq. 16 can therefore be reduced to

$$R_{AB,CD} = R_{AD,BC} = \frac{\rho \ln 2}{\pi t} \equiv R^0 \tag{17}$$

which gives a nominal, unstressed resistance which can be used to normalize the stressed resistance values obtained.

For a general, rectangular resistor, it has been found [15] that the unstressed, isotropic resistance equations are

$$R_{AD,BC} = -\frac{8\rho}{\pi t} \ln \prod_{n=0}^{\infty} \left\{ \tanh\left[\frac{L_1}{L_2} (2n+1) \frac{\pi}{2} \right] \right\} \tag{18}$$

$$R_{CD,AB} = -\frac{8\rho}{\pi t} \ln \prod_{n=0}^{\infty} \left\{ \tanh\left[\frac{L_2}{L_1} (2n+1) \frac{\pi}{2} \right] \right\} \tag{19}$$

where ρ and t are once again resistivity and thickness of the conductor, respectively. L_1 and L_2 are the lengths of the sides of the retangular conductor. The governing tensor equations of conduction in a stressed anisotropic conductor are given by

$$\overline{\mathrm{E}}_i'' = -\frac{\partial V}{\partial x_i''} = \rho_{ij}'' J_j'' \qquad \text{and} \qquad J_i'' = -\left(\rho_{ij}''\right)^{-1} \frac{\partial V}{\partial x_j''} = -\kappa_{ij}'' \frac{\partial V}{\partial x_j''} \tag{20}$$

Where E with overbar is electric field, V is the field potential, ρ is the resistivity, in tensor form, J is the current density vector, and κ is the conductivity tensor, which is simply the inverse of the resistivity tensor. The double prime represents the conductor coordinate system, as opposed to the primed coordinate system, which is that of the wafer. The equation of continuity for current flow in a conductive medium is

$$\frac{\partial J_i''}{\partial x_i''} = -\frac{\partial q}{\partial t} \tag{21}$$

where q is electric charge density. We wish to examine the steady state case, so Eq. 21 reduces to

$$\frac{\partial J_i''}{\partial x_i''} = 0 \tag{22}$$

Combining Eqs. 20 and 22 yields

$$\kappa_{11}'' \frac{\partial^2 V}{\partial x_1''^2} + 2\kappa_{12}'' \frac{\partial^2 V}{\partial x_1'' \partial x_2''} + \kappa_{22}'' \frac{\partial^2 V}{\partial x_2''^2} = 0 \tag{23}$$

In an isotropic material, the conductivity components, κ, do not depend on direction, so κ_{12} is zero. This leaves only

$$\kappa_{11}'' \frac{\partial^2 V}{\partial x_1''^2} + \kappa_{22}'' \frac{\partial^2 V}{\partial x_2''^2} = 0 \tag{24}$$

Silicon is anisotropic, however, and κ_{12} is non-zero. In order to use Eq. 24, and therefore Eqs. 18 and 19, it is necessary to perform appropriate coordinate transformations to the geometry of the device to achieve a κ_{12} which is zero. It has been found by Mian et al. [5] that the rectangular device is transformed to a parallelogram during the transformation of the governing equation from anisotropic to isotropic, as shown in Figure 8.

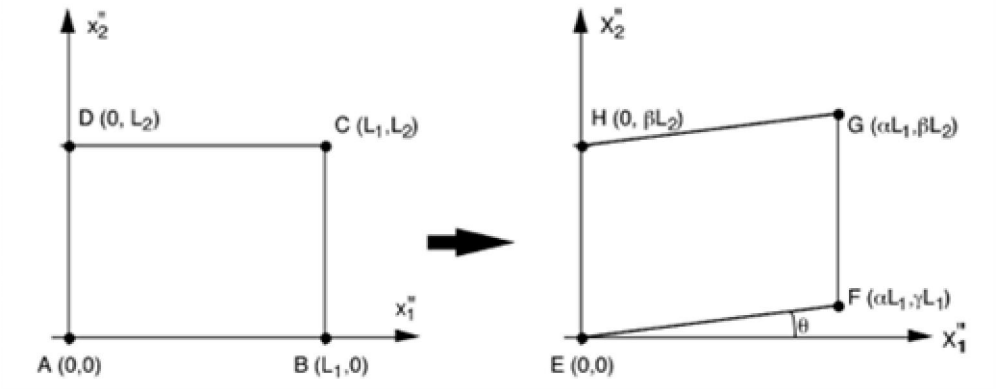


Figure 8: Anisotropic rectangular conductor transformed into an isotropic conductive parallelogram

It was also found that the angle at which the device geometry must be altered is less than 5° for the highest magnitudes of stress encountered in packaging applications. The resulting error is less than 0.1% if the parallelogram is approximated as a rectangle. Therefore, the quasi-isotropic parallelogram, which is equivalent to the anisotropic rectangle, will be approximated as an isotropic rectangle, and Eqs. 18 and 19 will be used, replacing L_1 and L_2 with the lengths of the sides of the parallelogram, which are given by

$$L_{FG} = \frac{\sqrt{\rho_{22}^{''}}}{\sqrt[4]{\rho_{11}^{''}\rho_{22}^{''} - \rho_{12}^{''2}}} L_2 \tag{25}$$

$$L_{EF} = \frac{\sqrt{\rho_{11}^{''}}}{\sqrt[4]{\rho_{11}^{''}\rho_{22}^{''} - \rho_{12}^{''2}}} L_1 \tag{26}$$

$$\frac{L_{EF}}{L_{FG}} = \frac{\sqrt{\rho_{11}^{''}}}{\sqrt{\rho_{22}^{''}}} \frac{L_1}{L_2} \tag{27}$$

The isotropic resistivity will be replaced with

$$\rho = \sqrt{\rho_{11}^{''}\rho_{22}^{''} - \rho_{12}^{''2}} \tag{28}$$

With these changes, and the assumption of a square VDP with $L_1 = L_2$, the resulting resistance equations are

$$R_{AD,BC} = R_{\varphi+90}^{\sigma} = -\frac{8\sqrt{\rho_{11}^{''}\rho_{22}^{''} - \rho_{12}^{''2}}}{\pi t} \ln \prod_{n=0}^{\infty} \left\{ \tanh\left[\sqrt{\frac{\rho_{11}''}{\rho_{22}''}} (2n+1) \frac{\pi}{2} \right] \right\} \tag{29}$$

$$R_{AB,CD} = R_{\varphi}^{\sigma} = -\frac{8\sqrt{\rho_{11}^{''}\rho_{22}^{''} - \rho_{12}^{''2}}}{\pi t} \ln \prod_{n=0}^{\infty} \left\{ \tanh\left[\sqrt{\frac{\rho_{22}''}{\rho_{11}''}} (2n+1) \frac{\pi}{2} \right] \right\} \tag{30}$$

where the R_{φ}^{σ} notation has been introduced to represent a stressed VDP device at 0 and 90 degree orientations. Note that the previously determined resistivity equations must be transformed once again to the double primed, device orientation. Also, note that further simplification of the product series to only two terms is possible due to $\rho_{11}^{''}$ and $\rho_{22}^{''}$ being very nearly equal.

The normalized resistance change will be defined as

$$\frac{\Delta R_\phi}{R_\phi} = \frac{R_\phi^\sigma - R^0}{R^0} = \frac{R_\phi^\sigma}{R^0} - 1 \tag{31}$$

where R^0 is unstressed resistance, and can be determined by

$$R^0 \cong -\frac{8\rho}{\pi t} \ln\left[\tanh\left(\frac{\pi}{2}\right) \tanh\left(\frac{3\pi}{2}\right) \right] \tag{32}$$

which can be obtained from Eq. 29 using unstressed resistivity and the first two terms of the product series.

Using the first two terms of the product series and reducing Eqs. 29-32 to piezoresistive coefficients and stresses, it has been found by Mian et al. [5] that the difference in normalized resistance change difference (NRCD), whose slope is a good measure of sensitivity because it is temperature compensated , of p-type VDP sensors oriented at 0°/90° is

$$NRCD_{0^\circ}^{p} = 3.157\pi_{44}^{p}\left(\sigma_{11}^{'} - \sigma_{22}^{'}\right) \tag{33}$$

Therefore the sensitivity is $3.157\pi_{44}^{p}$, and is not dependent on the size of the device. It has been determined by Law [9] that the angular dependence of the NRCD with respect to the [110] direction on (100) silicon is as shown in Figure 9.

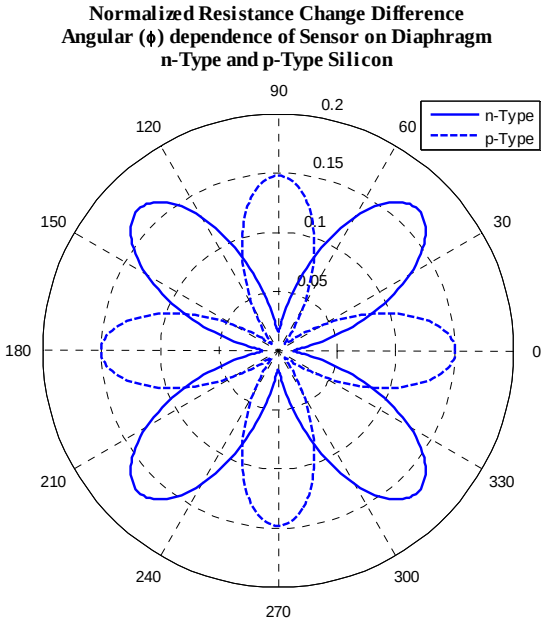


Figure 9: Normalized resistance change difference (NRCD) vs. device angle with respect to the [110] direction.

It can be seen that the maximum NRCD for at 0°/90° sensors occurs with p-type conductors, while n-type conductors have maxima at ±45°. The sensors to be tested experimentally will be of p-type, oriented at 0°/90° to the applied stress field.

The NRCD for a conventional piezoresistive strain gage is [8]

$$NRCD_{0^\circ}^{p} = \pi_{44}^{p}\left(\sigma_{11}^{'} - \sigma_{22}^{'}\right) \tag{34}$$

The sensitivity here is π_{44}^{p}. The VDP strain gage is found to be 3.157 times as sensitive as the conventional strain gage. In addition, the VDP device is able to sense both 0° and 90° configurations with a single sensor. The advantages gained for miniaturization are clear. In addition to miniaturization of the device itself, due to the measurement technique where current and voltage are measured as opposed to resistance, line resistance which connects the terminals of the device to a measurable pad will not

affect sensitivity, and can be miniaturized also. For the resistor devices, it is necessary to either determine the line resistance, or create a large enough line such that the resistance is negligible compared to the resistance of the device itself. The VDP strain gage also exhibits theoretical improvements in sensitivity in the ±45° directions, but these will not be examined in this thesis work.

These advantages, which have been shown analytically, and have been validated numerically by Law [9], must be evaluated experimentally. In this thesis work, sensors will be designed and fabricated which will allow for the comparison of the VDP structure with the serpentine resistor structure, and the testing of VDP sensitivity with respect to size. Additionally, the effect on sensitivity of rotational misalignment of the VDP device with respect to the substrate crystal lattice will be tested. Finally, a frame shaped piezoresistive device will be tested and compared to the VDP. Other sensors will be fabricated for future testing of other parameters for further characterization of the device, but will not be tested for this thesis work, though their design will be described.

TEST WAFER DESIGN

The VDP device has been shown analytically to have a number of advantages over conventional piezoresistive device structures. The theoretical benefits of the VDP device structure have been verified using finite element analysis techniques, and must be further examined experimentally. This thesis presents the work done in design, fabrication, and testing of the VDP devices to achieve experimental validation.

Wafer Selection

Silicon wafers can be purchased in a variety of diameters and thicknesses, with alternatives for polishing, dopant type, and oxide layers. N-type wafers were chosen due to the selection of boron as the dopant for the piezoresistive devices, which is a p-type dopant. P-type dopant for the VDP devices was chosen because it has its highest sensitivity in the 0° and 90° configurations, which we want to measure. Additionally, 45° devices would have a slight amount of jaggedness to their edges from the mask making process. For proper functioning of the devices, it is necessary to have the devices doped into an opposite type substrate. At the junction between an n-type and p-type region, electrons will initially move from the n-type region to the p-type, filling the holes, and creating a neutrally charged area and insulating against further flow through the region, called a p-n junction. If the same dopant type is chosen for the substrate and the device, current will leak into the substrate as in Figure 10.

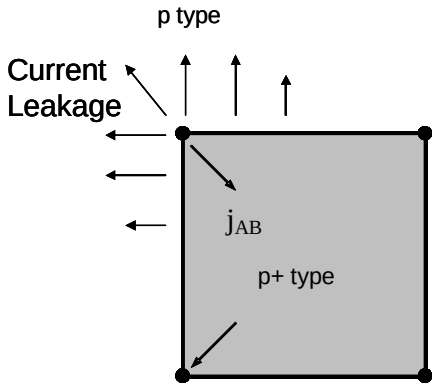


Figure 10: Current leakage will occur if p-type is the chosen dopant for both substrate and device

Note that a p-n junction as described will not perfectly insulate, and a large enough bias will still result in current leakage, as shown in Figure 11.

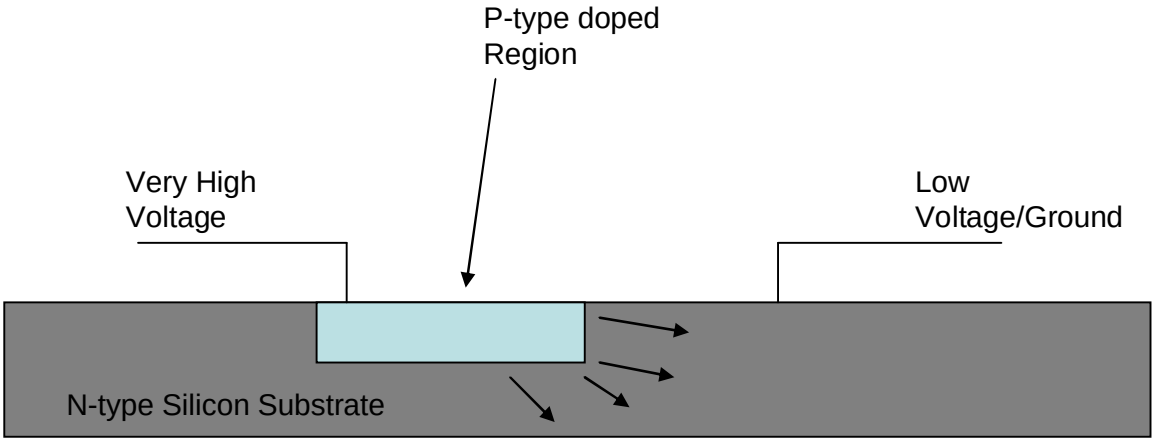


Figure 11: Current leakage can still occur with large enough bias across the p-n junction formed at the doped region interface.

This choice of n-type wafer limited the mask design in that the number and location of wafer flats are as shown in Figure 12.

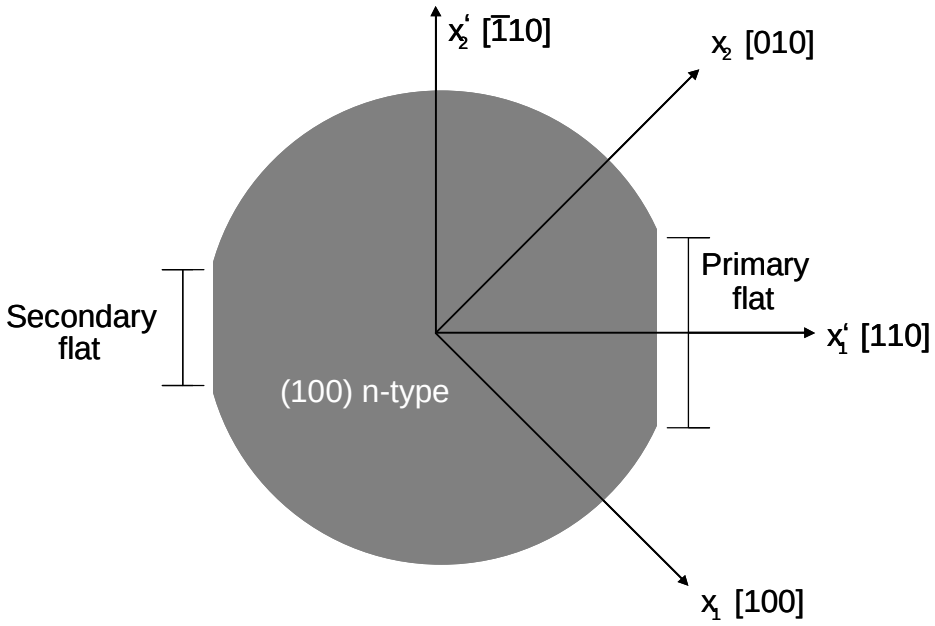


Figure 12: Wafer flats for an n-type (100) wafer.

It was also known that there would be no need for silicon on insulator (SOI) wafers, which contain a layer of oxide underneath a layer of silicon created through thermal oxide growth and subsequent epitaxial layering of silicon [16], as a release step would not be needed for the diaphragms to be built. However, it was necessary for the wafers to be double side polished (DSP) wafers, as a rough surface would make etching of the backside of the wafers unreliable, and attaining a seal during testing difficult. The wafer diameter was chosen to be 100mm (4in.) due to the processing capabilities of the Montana Microfabrication Facility (MMF).

Diaphragm Thickness, Size, and Spacing

The wafer thickness is dependent on the diaphragm size, thickness, and spacing. For a 100mm wafer, diaphragm sizes of approximately .5cm, 1cm, and 2cm were chosen for

ease of testing, and to provide approximately 10-20 diaphragms per wafer to allow a number of parameters to be tested. Silicon is brittle, so failure stress varies significantly due to material flaws. Silicon will fail at approximately 7000MPa, with an elastic modulus of 190GPa [17], but stress concentrations will reduce this significantly. It has been found that stress concentrations due to anisotropic etching will reduce this to approximately 300MPa. Because material flaws may lower this further, to safely ensure failure does not occur in the diaphragms, a value of approximately 70-80MPa will be used to constrain the thickness at the highest pressure difference. A pressure sensor diaphragm can be modeled as a plate with clamped edges, provided the difference in thickness between the diaphragm and wafer is large. It was decided that a 3:1 ratio of wafer thickness to diaphragm thickness would be sufficient to ensure that wafer bending during testing was insignificant, and that the model used in thickness calculations was accurate. It is shown by Urugal [18] that the following relationships are true for a plate with clamped edges.

$$w = 0.00126\frac{p_o a^4}{D} \tag{35}$$

$$M_x = M_y = 0.0513 p_o a^2 = M_{\max} \tag{36}$$

Where M_x occurs at the diaphragm edge, and w occurs at the diaphragm center. To find the maximum stress, equation 3 is used.

$$\sigma_x = \frac{12 M_x z}{t^3} \tag{37}$$

Because the maximum stress is on the surface of the diaphragm, z = t/2. Equation 4 is then used to determine the maximum diaphragm thickness, t, given a diaphragm width, a, and applied pressure, p_o.

$$t = \sqrt{\frac{0.3078 p_o a^2}{\sigma_x}} \tag{38}$$

Initially, a pressure of 100kPa, or approximately vacuum, was used to calculate the diaphragm thickness. It was later determined that the testing pressure chamber was unable to maintain an airtight seal below approximately 50kPa. In order to ensure that the sensors produce a range of values over this area, the thickness was then recalculated with a p_o value of 50kPa. The value of stress used was 80MPa, and the diaphragm width, a, was 1cm. Two cm diaphragms would be much more susceptible to failure than the 1cm diaphragms under the same pressure loading. It was chosen to use a diaphragm width of 1cm, however, as most of the diaphragms to be created are 1cm, and it was desired to have a full range for the 1cm diaphragms. The result of the calculations is shown in Table 1.

Table 1: Calculated Diaphragm Thicknesses

Pressure (kPa)	Diaphragm Width (cm)	Maximum Stress (MPa)	Calculated Thickness (µm)
100	1.0	80	196.2
50	1.0	80	138.7

A thickness of 140µm after the capabilities of the pressure chamber were determined. It should be noted that the thinning of the diaphragms created problems during processing when the wafers were placed in vacuum for various process steps. Two wafers burst due to the excessive pressure difference, coupled with cracking issues developed previously.

Another upper boundary to the thickness was determined by the etching method. Tetramethylammonium hydroxide (TMAH) was to be used for the bulk etching of the diaphragms. TMAH is an anisotropic etchant, meaning that etch rates differ with direction. Anisotropic, strong-base etchants such as KOH or TMAH etch the {100} and {110} planes significantly more rapidly than the {111} planes [19]. The result is features which are always rectilinear and very nearly flat, unlike the curved surfaces and undercutting of wet etch processes shown in Figure 13.

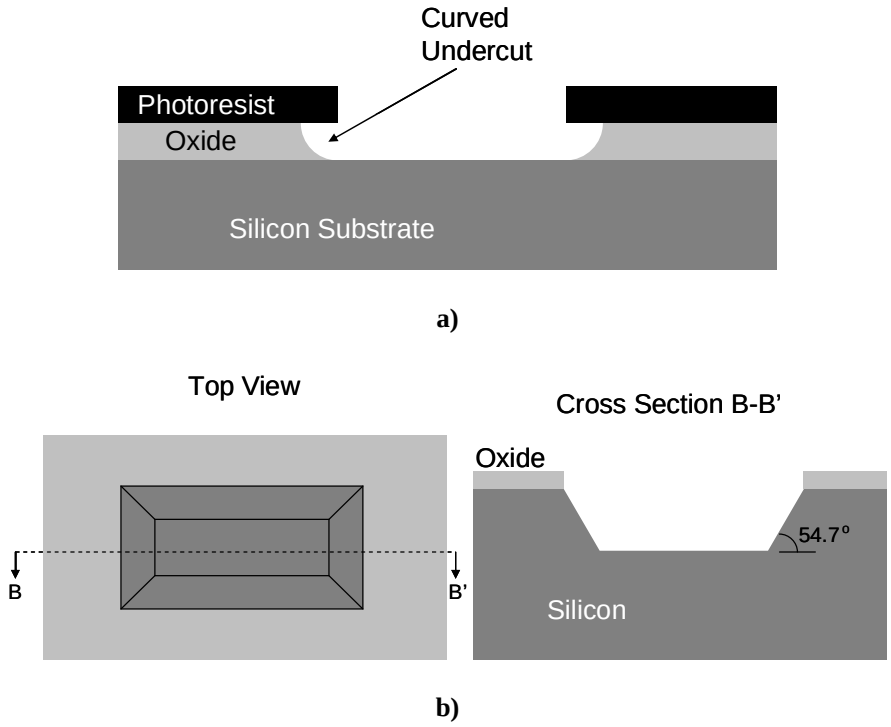


Figure 13: a) Isotropic etch characteristics from BOE oxide wet etching b) Anisotropic etch characteristics from TMAH silicon wet etching

The etching process will form a 54.7° angle between the wafer plane and the etch surface, due to the resistance of the {111} plane to etching. This etch effect is important in the creation of the diaphragms, so wafers with the {100} plane as the surface plane,

referred to as (100) wafers, are needed. The angle of the anisotropic etch restricts the distance between diaphragms given a certain wafer thickness. It is necessary to have the diaphragms separated such that global wafer bending is insignificant while the diaphragm is tested, and also such that a proper seal can be made during device testing. Because the number of diaphragms, their size, and thus their separation had already been determined, a limit on wafer thickness followed. It was found that a wafer thickness of 525µm was commonly available. If etched entirely, the difference between the top edge and bottom edge would be approximately 150µm as shown in Figure 14.

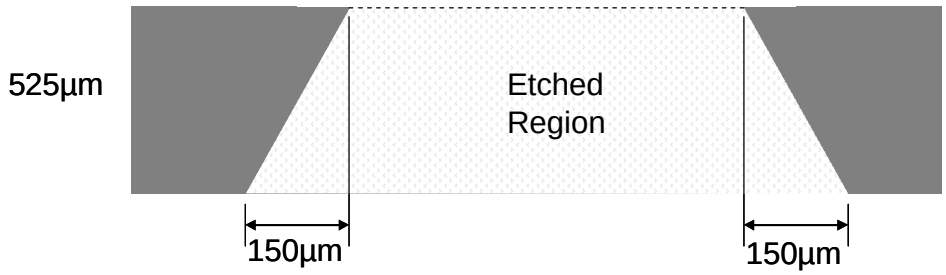


Figure 14: Illustration of maximum width of angled regions

During the early design phase, a wafer much thicker than 525µm was assumed, so there was room to separate the diaphragms much further than double this value.

Because silicon dioxide (SiO_2), commonly referred to as “oxide”, will be used as the mask for the etch process, the selectivity of TMAH with respect to oxide and the maximum thickness oxide layer that can be applied also limit the thickness of the wafer. The highest feasible oxide layer that can be deposited at the MMF is approximately 1µm. The rate at which TMAH etches silicon is found to be approximately 11-13µm per hour, and the rate at which it etches silicon dioxide is found to be much slower, at approximately 0.005-0.008 µm per hour. The maximum depth of silicon that can be

etched before all oxide is etched away is therefore over 1300µm, well over any reasonable wafer thickness that would be used.

A number of other parameters can be specified for commonly available silicon wafers, such as sheet resistivity, bow, total thickness variation (TTV), among others. It was determined that most of these parameters were commonly available well within the limits needed for the sensors to function. The thickness variation was ±25µm, which was found to not effect the resulting data, and was likely much less than ±25µm in actuality.

The final wafer specifications are displayed in Table 2. Eighteen wafers were purchased, and nine processed in order to help ensure a successful result.

Table 2: Wafer Specifications

Diameter	Thickness	Thickness Variation	Dopant	Resistivity	Surface	Orientation	Grade
100mm	525µm	±25µm	n-type	1-20 Ω-cm	DSP	(100)	SEMI Prime

Process Design

Silicon pressure sensor processing is a relatively simple process which is very similar to the processing for simple microcantilevers without the problematic release issues [26]. All process steps will be performed at the MMF, and the work will be funded by a user grant. The basic process flow is modeled after a MEMS lab which produces wafers with a number of cantilever beams and pressure diaphragms, and can be seen in Figure 15.

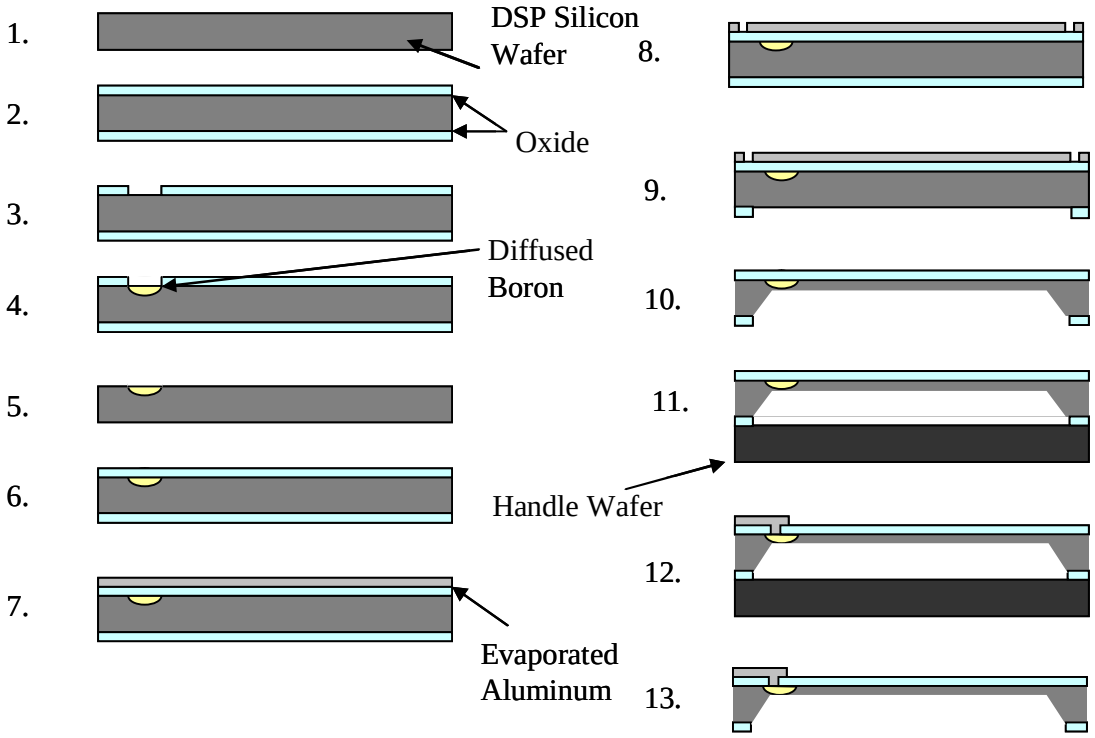


Figure 15: Basic process flow to produce pressure sensor.

Starting with the DSP silicon wafer selected, a thermal oxide layer will be grown (step1-2). This oxide layer will then be patterned and etched (step 3) to create the openings through which the VDP devices will be doped using boron diffusion (step 4). The oxide will then be stripped and regrown (steps 5-6). A layer of evaporated aluminum will then be deposited to serve as both an etch mask and an alignment tool (step 7). Following this, the aluminum layer will be patterned with alignment marks (step 8). Lithography will then be done on the backside to pattern the oxide and etch it (step 9). The wafer will then undergo backside etching in order to create the diaphragms, along with removal of the aluminum layer (step 10). After the diaphragms have been etched, a handle wafer will be bonded to the etched wafer, as the wafer will now be more fragile

(step 11). The remaining layer of oxide will be patterned and etched to provide a mask for the vias. These vias will provide direct electrical contact with the diffused regions. Another aluminum layer will then be deposited and patterned to create the lines to connect the devices to the pads where micropositioners will be used to test them (step 12). To complete the wafer processing, the handle wafer will be removed (step 13).

Note that this basic process flow was modified to remedy issues encountered during processing, which will be discussed in more detail in the wafer processing section of this thesis. Specifically, wafer frontsides were bonded together to prevent pinhole formation during bulk etching, and separated immediately afterwards. Also, the oxide masking layer used in bulk etching was stripped and regrown due to layer quality issues encountered.

Mask Design

The MMF does not have the capability to create photolithography masks, so the masks were created using AutoCAD software, converted to the appropriate GDSII (extension .gds) file type, and ordered from the University of Minnesota.

Mask creation is a complex process which requires careful attention to detail. A number of design considerations must be followed in order to produce an appropriate mask. It was necessary to be aware of minimum feature sizes, as UM's mask maker was unable to create masks with feature sizes less than 1.5µm, and it is required to know the minimum feature size present in each mask. The masks are essentially a raster map of tiny blocks. The result is that any line created in the mask which is not at a 0 or 90° orientation will have jagged edges. Rasterized maps also mean that the mask maker

cannot accept values smaller than some given length. For the UM mask maker, this minimum value restriction means that acceptable design snaps are 1µm, .5µm, and .1µm. Any length given in the GDSII mask file smaller than these values will be rounded. When first designing the mask, this was not known and design snaps were not used. However, it was determined that any rounding that would occur would not create open circuits, and was therefore unimportant.

It's also important to be aware of the process steps when creating masks, as it will be necessary to specify whether a dark field or light field mask is needed. As shown in Figure 16, a dark field mask lets light through the features when it is exposed, whereas light field blocks light through those features.

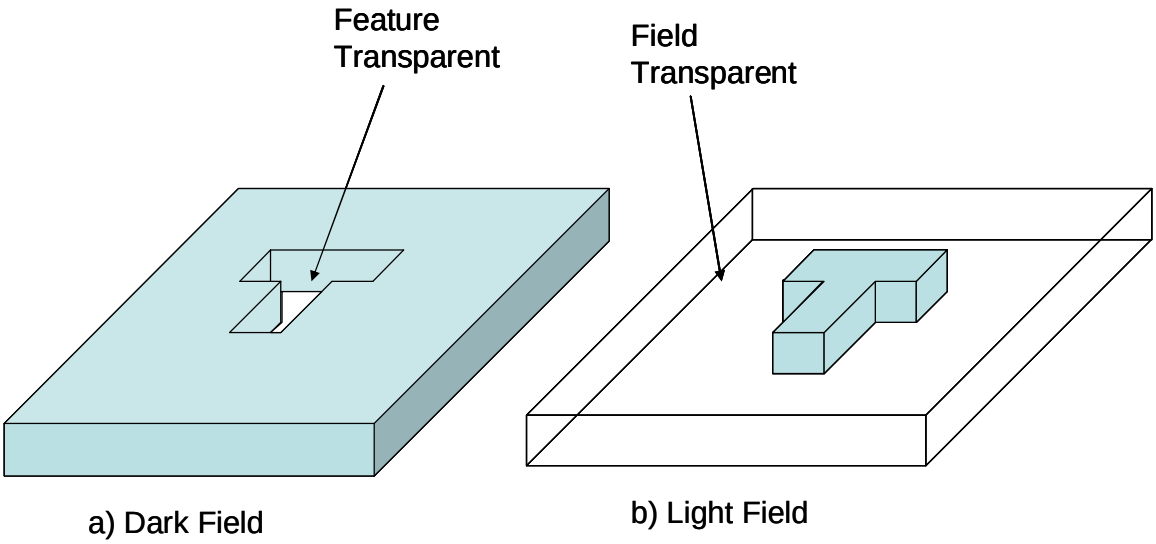


Figure 16: Difference between light and dark field masks

The type chosen depends on the photoresist type, which can be positive or negative, and on the specific process to follow the lithography step. Positive photoresist becomes

soluble in developer when exposed to light, negative photoresist becomes insoluble, as shown in Figure 17.

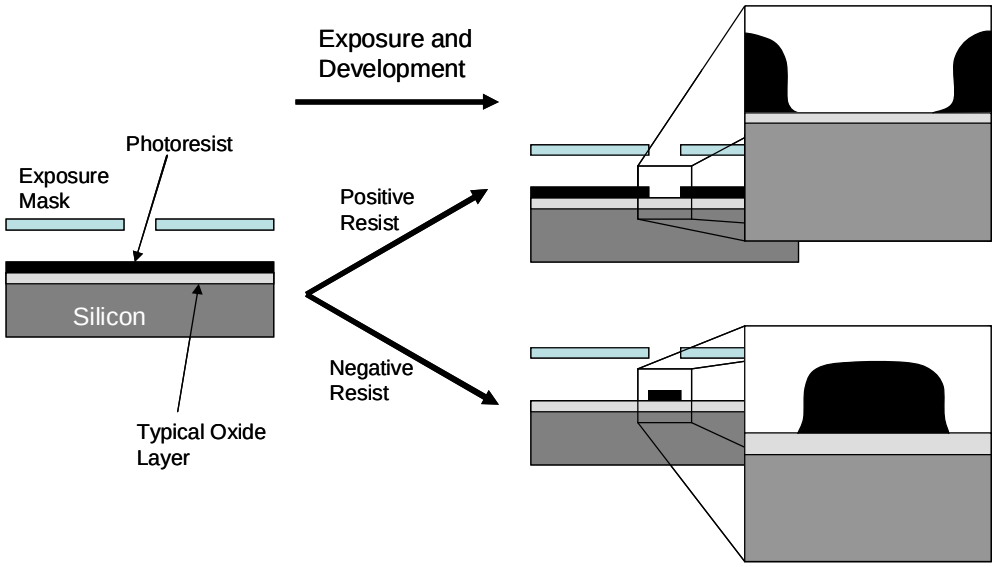


Figure 17: Illustration of differences between positive and negative photoresist

Another design consideration is the construction of features. In particular, features where one element of a feature is set inside another, as seen in Figure 18.

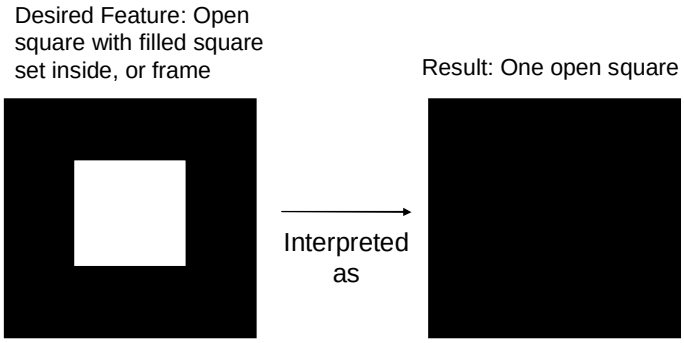


Figure 18: Mask maker feature interpretation leads to inset features disappearing

If we consider the mask in Figure 18 a dark field mask, the mask maker will not recognize the inner feature as one which should closed, but rather as two overlapping

open areas. The solution is to make the feature from a single closed line, with the path crossing the open area overlapping as shown in Figure 19.

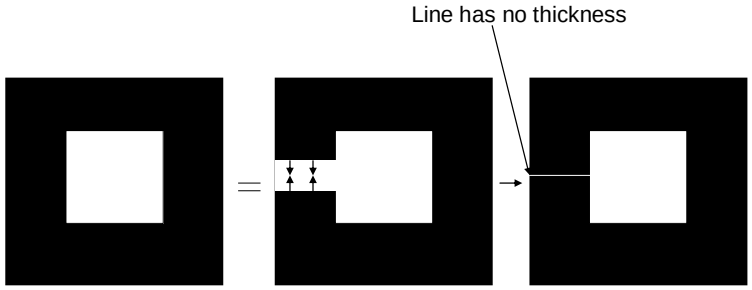


Figure 19: Method for creating overlapping frame-like features.

It is also necessary to ensure that all areas are closed, and that open lines with a given thickness are properly converted when moving from AutoCAD to a GDSII file. Lines with no thickness cannot be interpreted by the mask maker.

With these considerations in mind, it was necessary to create drawing guides which would not be a part of the final masks. These were the 100mm diameter wafer, which was placed entirely in the first quadrant of the design space, such that all coordinate values were positive. Wafer flats were included, but drawn only to relative scale as their actual depth was unimportant. Diaphragms were then laid out in an appropriate fashion based on the approximate separation distance calculations done previously, assuming a much thicker wafer. These diaphragms are not a part of an actual mask, but the result of the backside etching, and as such, they are only a drawing tool. Lastly, the dicing lines where laid out. The finished wafer was not diced, but the approximate lines were drawn in for future use.

The drawing guides provided the overall layout of the wafer, allowing the devices to be designed and positioned. The wafer was designed to measure a number of different

parameters. First, it was necessary to compare the VDP sensitivity with that of a serpentine resistor, and an FTT device. The basis on which the devices were designed was size; specifically, a characteristic length. Each device was designed to be approximately square in terms of the amount of space needed in each wafer direction as shown in Figure 20.

The characteristic length for each device was the length to a side, which was approximately 120µm for each device. The FTT was sized larger due to its relative angle resulting in a smaller overall area, possibly decreasing sensitivity. The actual lengths are shown in Figure 20.

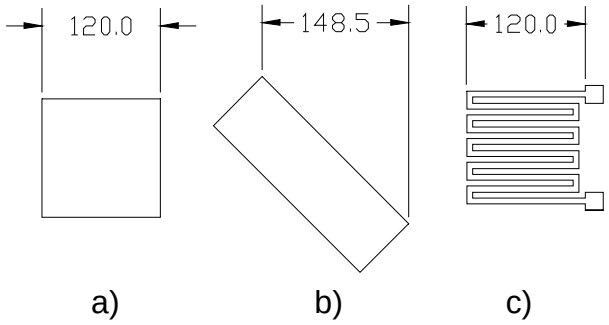


Figure 20: Sizes of the doped device regions for a) van der Pauw (VDP) structure b) Four Terminal Transducer (FTT) and c) Serpentine Resistor. Units are µm.

Six 1cm diaphragms, and six 0.5cm diaphragms were devoted to the comparison of these device types. Four devices were placed on a single diaphragm, with each diaphragm containing only one device type. The devices were oriented in differing directions in order to measure different stresses. The center of each device was placed 250µm from the diaphragm edge, but it was later determined that due to a design change, this would become approximately 375µm.

Effect of VDP size

After designing the sensors for the device comparison, 7 diaphragms remained for testing various other parameters. A diaphragm was used to test the effect of size on diaphragm sensitivity. The size varied from 120µm to 300µm as seen in Figure 21.

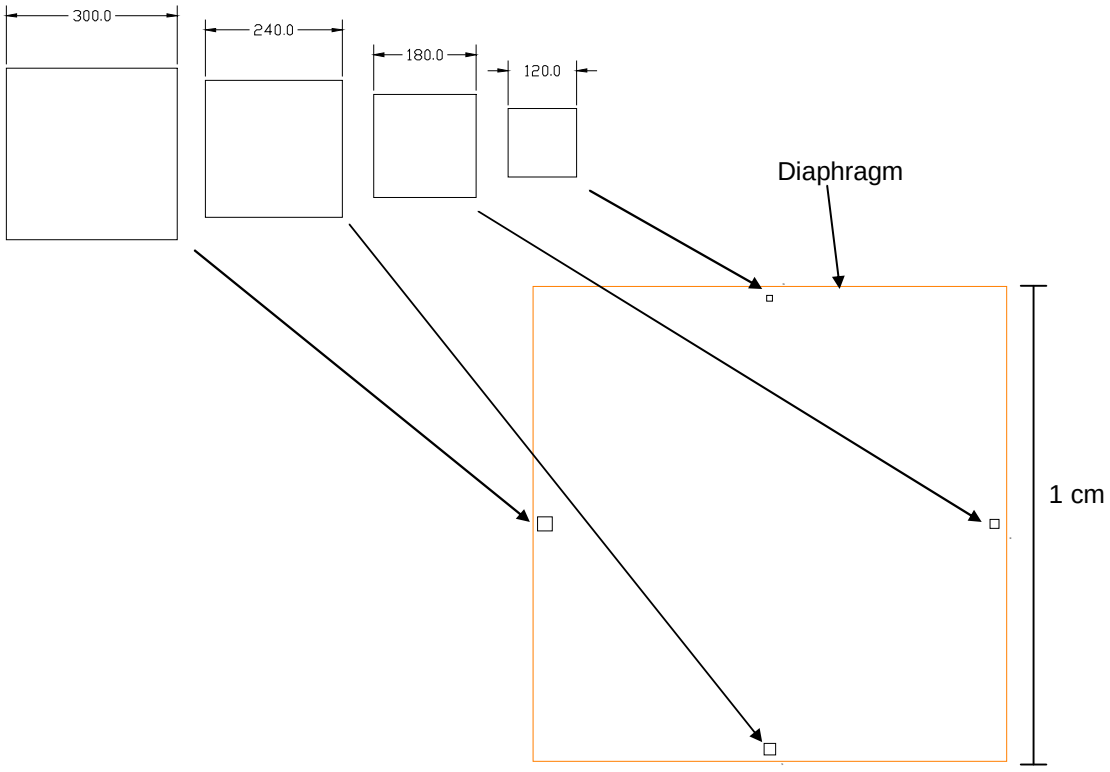


Figure 21: Diaphragm containing relative sized VDP devices. VDP units in µm.

Effect of Rotational Misalignment

Another diaphragm was used to test the effect of misalignment errors on the sensitivity. Misalignments of 1° to 3° CW and CCW were designed into this diaphragm, also shown in Figure 22.

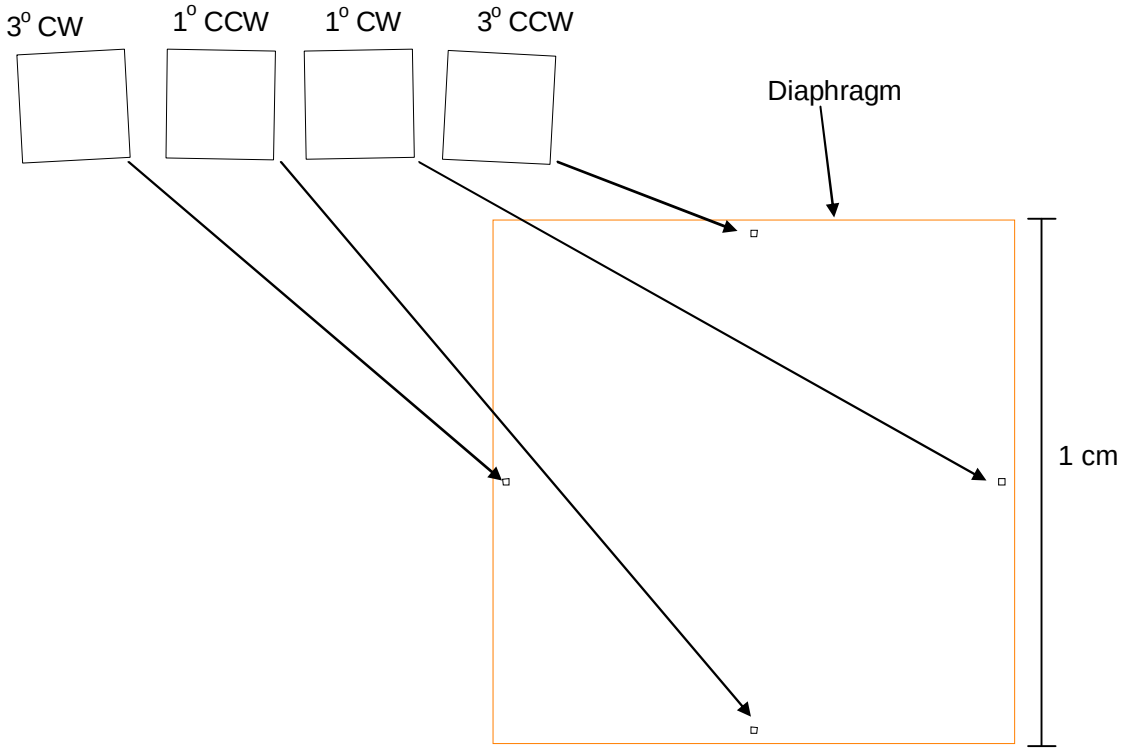


Figure 22: Diaphragm containing misaligned VDP devices. VDP units in µm.

Alternate Conductor Shapes

Two diaphragms were used to test variations of the VDP test structure shape. The first, an eight terminal VDP, was designed and may be studied by our group in the future. Note that this structure has a larger characteristic length than the other devices, as shown in Figure 23.

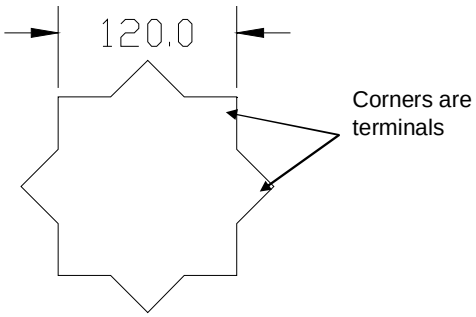


Figure 23: Eight terminal VDP structure. Each corner is a terminal. During use, four terminals will be used, allowing for 0°, 90° and ±45° measurements with one device.

Another structure is a ‘hollow’ device, called a picture frame, which is based on a design by Motorola [19]. This structure, also shown in Figure 24, will be compared to the VDP sensitivity.

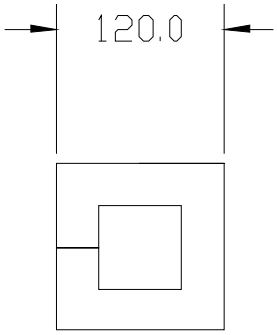


Figure 24: Frame-shaped piezoresistive device designed by Motorola. Units in µm.

Deflection Measurement Using VDP

One of the remaining two 1cm diaphragms was designed with an odd via structure, and will not be discussed in this thesis work. It was later discovered that it would have been more appropriate to use this diaphragm as a backup for the serpentine resistor diaphragms, possibly with more bends, as they were difficult to fabricate and were found to be rather insensitive. The last parameter to design into the wafer was designed to test the viability of the VDP device as a surface deflection measurement device. The other remaining 1cm diaphragm contained a series of VDPs, as shown in Figure 25, to examine the effect of device positioning relative to the diaphragm.

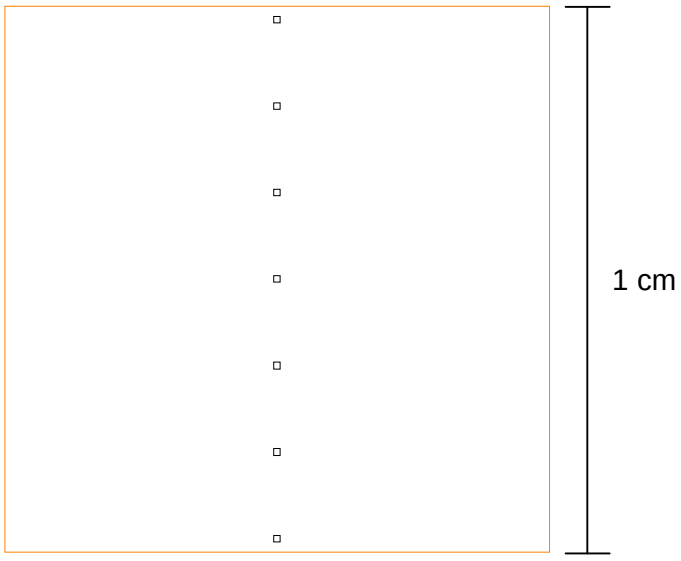


Figure 25: Array of VDP devices across a diaphragm to examine stress variation

A 5x5 array of VDP sensors were positioned on the remaining 2cm diaphragm. The purpose of this diaphragm is to examine the effect of positioning on device output, and

also as a test structure for ongoing work in examining the use of VDP devices in surface deflection measurements. The array can be seen in Figure 26.

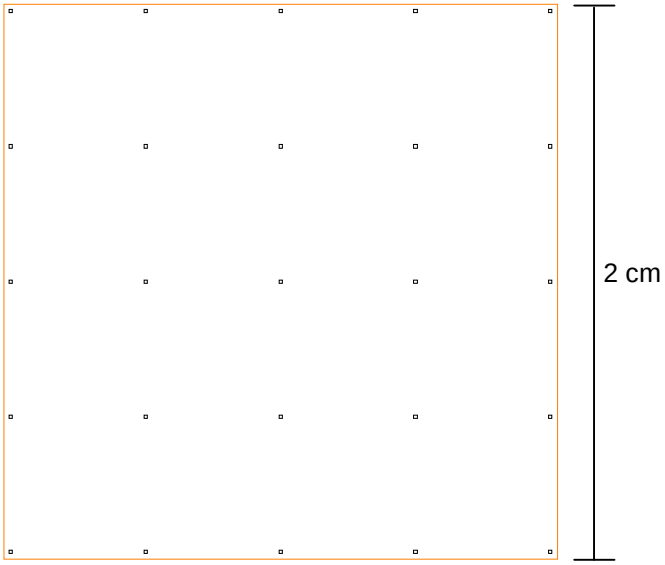


Figure 26: 5x5 Array of VDP devices covering a 2cm diaphragm to examine VDP suitability as surface deflection sensor

These two diaphragms allow for testing of the VDP output based on its position on the diaphragm, which may be used to calculate the plate deflection. Such small scale deflection measurements may have applications in deformable micromirror deflection measurements [20]

Calibration Test Structure

A test strip was also designed into the wafer in order to test the devices response to stress in a 3-point bend tester as opposed to a pressure diaphragm. Each of the three main device types was placed on the test strip in various orientations. This test strip is shown in Figure 27.

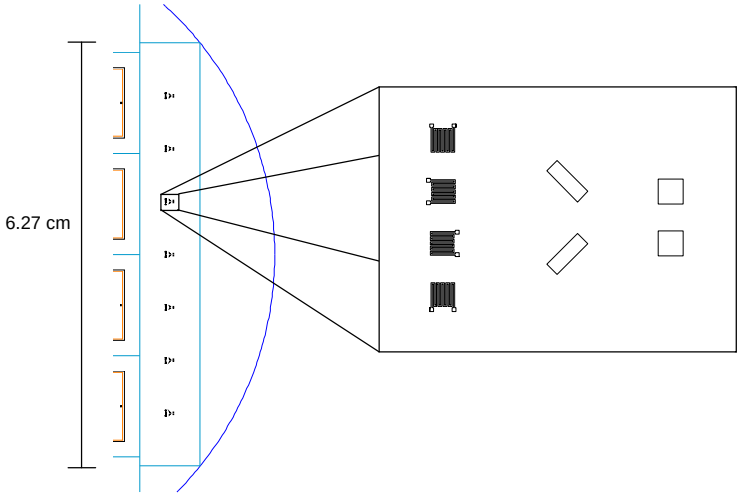


Figure 27: Test strip for testing of the devices under 3-point bend tests rather than pressure diaphragms.

Another test area was created to test the sheet resistivity achieved in the doping step. These areas are large doped rectangles, which served both as a testing area, and as a wafer orientation guide during processing, as they were the only structures that could easily be seen in the early processing stages. These test structures are shown in Figure 28.

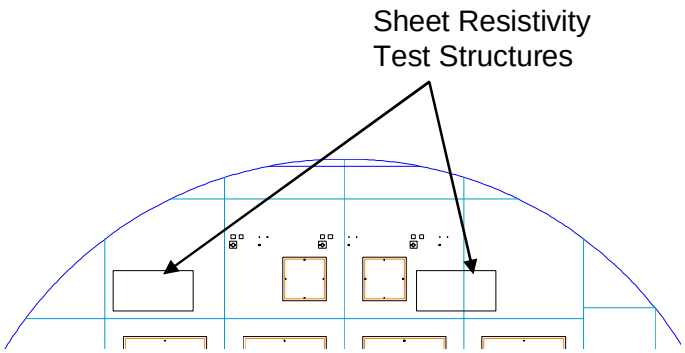


Figure 28: Test structures to be doped with boron for sheet resistivity measurements.

All of the devices explained above were combined into the BORONDOPE mask, which is used in the lithography step preceding the boron diffusion step. The next mask to be designed was the bulk etch mask. The mask is to be applied to the back of the

wafer, but the UM mask maker provides an option for “right reading chrome side down” which is essentially an option to mirror the mask for backside processing. The design process was the same as if the mask were applied to the front side, except that the right reading chrome side down option of ‘no’ was selected.

Backside Etch Mask

The design of the backside etch mask was simple, involving only a scaling of the diaphragm guides created in the first step of the mask design. Because the wafers were assumed to be much larger than they would be, the openings in the mask were oversized. The openings should be approximately 272.6μm wider on each side than the diaphragm guides, or 1.0545cm on a side for the 1cm diaphragms, 0.5545cm for the 0.5cm diaphragms, and 2.0545cm on a side for the 2cm diaphragms. The openings were created 236μm wider on each side, however, which results in smaller diaphragms than intended in the final wafer, at approximately 0.9927cm for the 1cm diaphragm, and 0.4927cm and 1.9927cm for the 0.5cm and 2cm diaphragms, respectively. This amounts to a .73% decrease in diaphragm size for the 1cm wafer, which will not result in additional risk of diaphragm failure. The correct value of diaphragm size will be used in all subsequent calculations. The larger devices were not repositioned due to this change, placing them at ~176.8μm from the diaphragm edge.

The backside mask, along with the drawing guides can be seen in Figure 29.

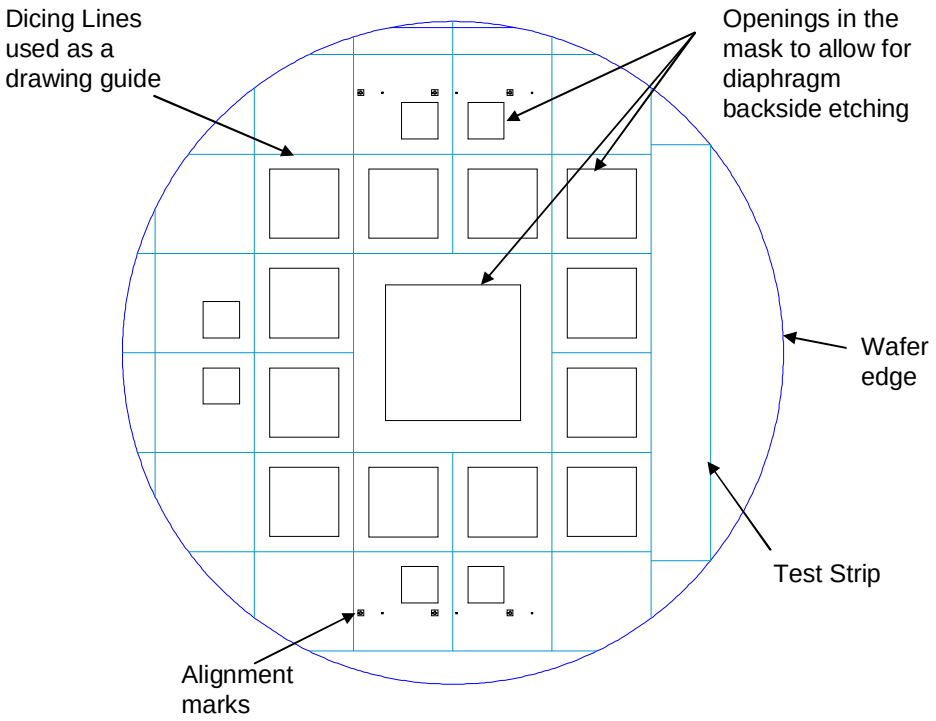


Figure 29: Backside etch mask with drawing guides to illustrate size.

Note that only the diaphragm boxes and alignment marks are in the mask; the drawing guides are not included.

Metal Lines and Vias

Because a layer of protective oxide will cover the doped devices, vias must be created to connect the devices to the aluminum lines which will lead to the exposed pads. Without these vias and lines, measurement would be difficult not only due to the size of the devices in relation to the testing apparatus, but also because a native oxide layer continually forms over the devices, inhibiting proper connection to the devices. Vias are often created in arrays for ease in resizing. The vias for each device were the same size,

3µm square elements in arrays, but the FTT via had more elements in the array as shown in Figure 30.

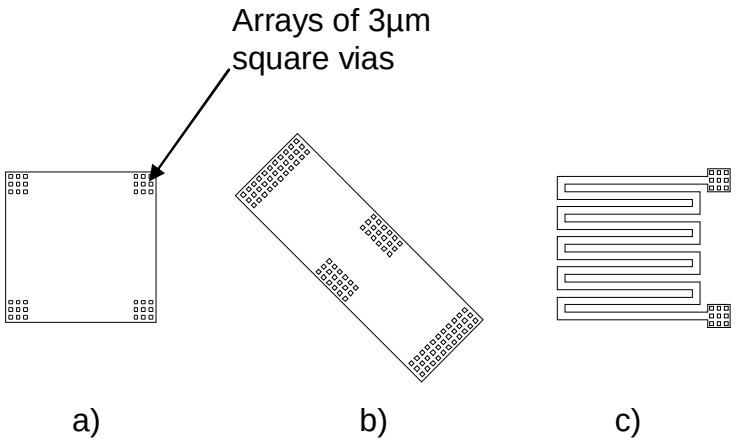


Figure 30: Via positioning for a) van der Pauw (VDP) structure b) Four Terminal Transducer (FTT) and c) Serpentine Resistor.

Rather than dope in pads to which the vias would connect, it was decided that the vias would connect directly to the underlying doped region. The choice was made to avoid unwanted affects due to unusual doped region shapes, as shown in Figure 31.

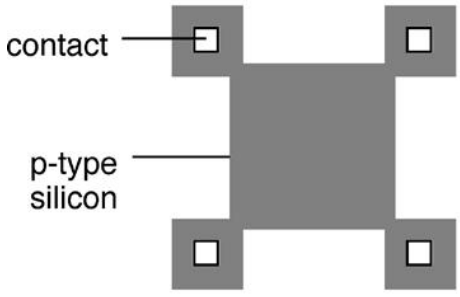


Figure 31: Alternative form for VDP device utilizing doped pads and vias outside the primary device region.

A large array of vias was created in an open area near the diaphragms. These vias connect to an aluminum pad created in the aluminum lines step. The purpose of the pad is

to maintain a grounded background and prevent current leakage. The array of vias can be seen in Figure 32.

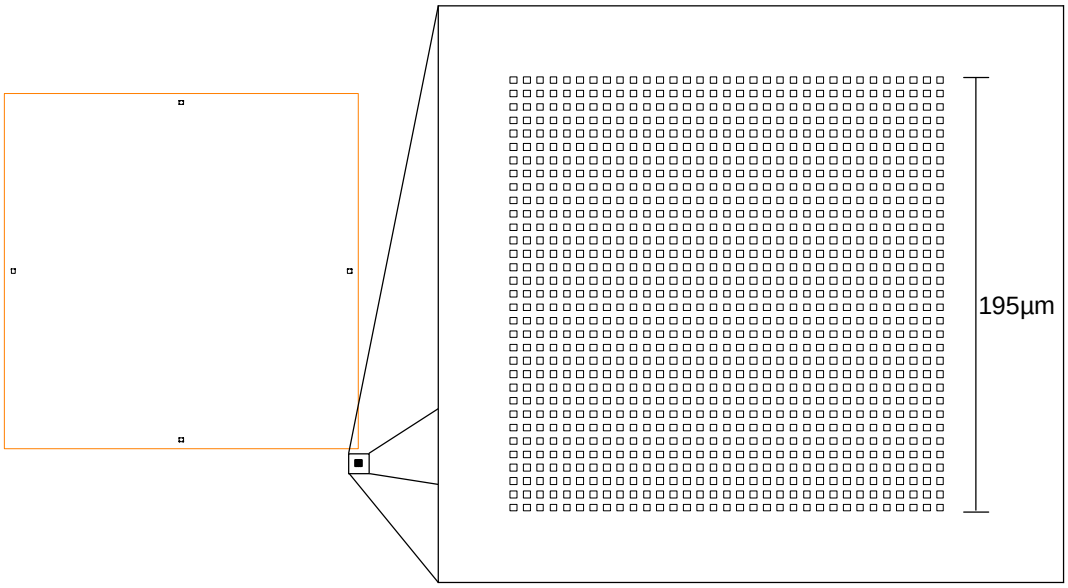


Figure 32: Large array of vias for the purpose of biasing the wafer to avoid current leakage in the device. These arrays are placed near the diaphragms.

The via size was later found to be problematic. A 3µm feature size was achievable during processing, but rounded features were created. In subsequent designs, it is recommended that at least 5µm vias are used. Plasma ashing was necessary to fully remove the photoresist from the vias. The ashing is an etch process which etches vertically, allowing removal of the photoresist in the vias without widening them.

The final step in creation of the sensors is to create the aluminum lines and pads. The pads cover the vias, which will fill them with aluminum when processed. The lines were created using open lines with a specified thickness of 10µm in AutoCAD. Prior to conversion, this mask was split into two masks. One mask contained the pads, which are closed areas, created with closed lines. The other contained the lines, which are open

lines. Each mask was converted separately and reinserted into the GDSII file which contained all masks. The two split masks were then combined into the final ALCOMP mask shown in Figure 33.

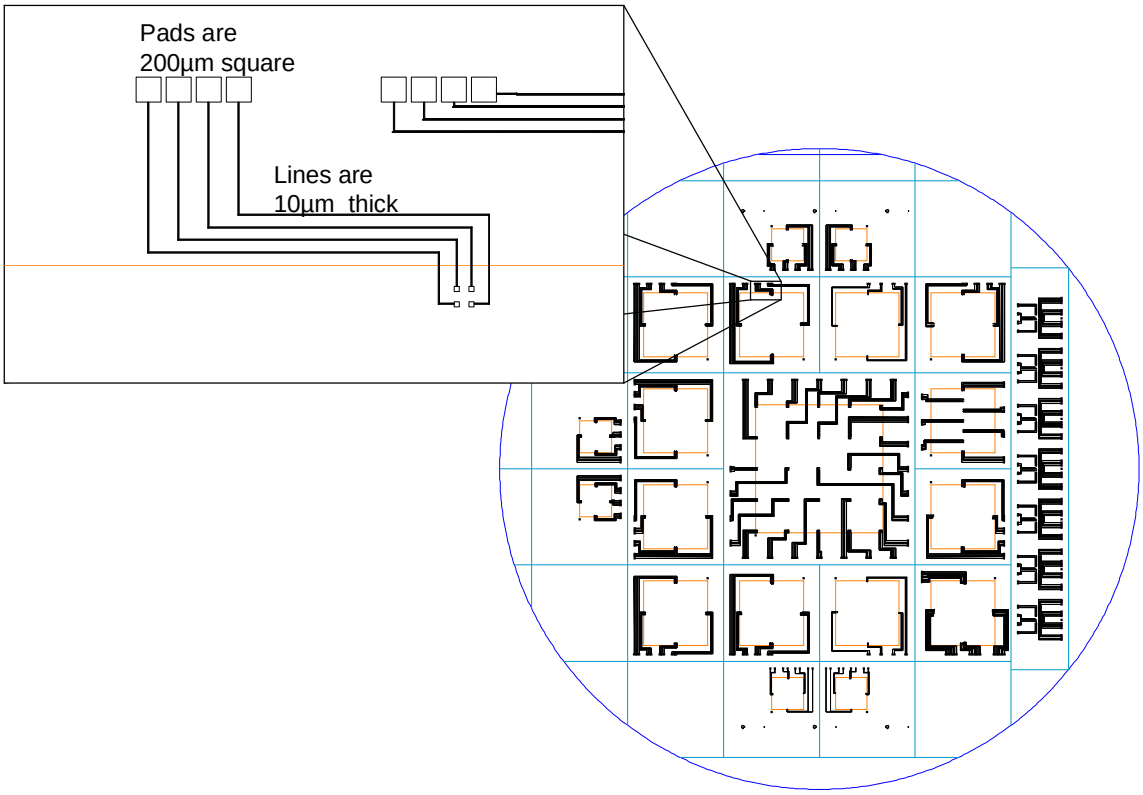


Figure 33: ALCOMP mask with small section magnified

The VDP and FTT devices require four lines and pads for each device; two for current input, and two for voltage measurement. The serpentine resistor devices require only two for resistance measurements. The lines were positioned such that little aluminum would be on the pressure diaphragm itself to avoid abnormalities in stress. On the center diaphragm, where the devices are in an array, this was difficult to achieve. The pads were positioned near each other, and grouped, for ease of measurement. It was

necessary to place the pads a significant distance from the dicing lines to ensure that the pads weren't damaged due to chipping during dicing. The distance chosen was 1mm.

Alignment Markers

In order to position masks relative to the wafer during processing, alignment marks are needed. On the first photolithography process, alignment is done with the wafer flats, and is imprecise. This misalignment of the masks, and consequently the devices, with respect to the crystallographic axes leads to reduction of the sensitivity of the device [9]. The effect of misalignment has been examined analytically by our group, and will be characterized by the diaphragm with misaligned devices. With this first photolithography process, it is necessary to apply alignment marks which will allow for much more precise alignment, both rotational and translational, for all subsequent photolithography processes to the first mask. A common form for alignment marks is the cross and box form shown in Figure 34 [26]. It was chosen to align a cross on the mask to a box on the wafer.

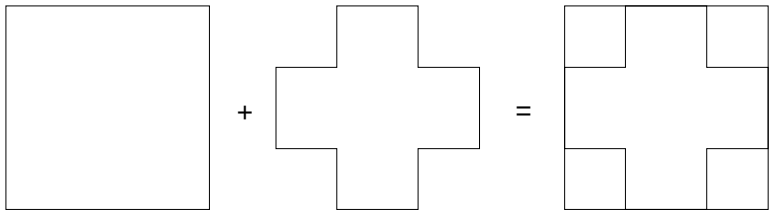


Figure 34: Cross and box alignment markers.

It was necessary to ensure the proper areas would be shielded and open on the masks, which was determined by the whether the mask was dark or light field. All masks aside

from the ALCOMP mask were dark field, which requires the cross to be placed as a shielded area inside an open area, as in Figure 35. The ALCOMP mask did not require this open area, as its field is light.

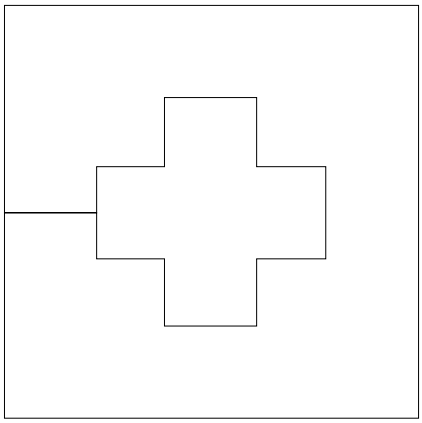


Figure 35: Alternative form of the cross alignment marker to prevent shielding of the underlying box.

Typically, masks contain one cross to align to the previous marker, and one box to create the marker for the following mask. For pressure diaphragm creation, a backside process must be done, which requires backside alignment. Alignment markers created from the previous step could not be seen from the backside. To remedy this, a mask was designed for patterning an aluminum layer to be deposited on the frontside of the wafer for the purposes of etch masking and alignment. The mask contained alignment markers, and a few open areas to aid in alignment, which were later removed due to etch masking issues. The contact aligner used to align the wafer has the ability to shine infrared light onto the backside of the wafer. Infrared light does not penetrate aluminum, but it will penetrate silicon, silicon dioxide, and photoresist. The infrared light, along with the

alignment markers in the aluminum layer, allows for the alignment of a backside mask to the frontside of the wafer.

It was a concern that after the backside etch process was completed, and the aluminum masking layer removed, that the box marker placed by the backside etch process would be easily seen from the backside, but undetectable on the frontside without any material to block the infrared light in the area around the alignment marker. This would make alignment of the via mask impossible. To solve this issue, the first mask, BORONDOPE, contains two boxes, one for the alignment of the aluminum layer mask, and another for alignment of the via mask which follows bulk etching. The alignment box placed by the aluminum layer was placed to the inside of the previous marker, as shown in Figure 36.

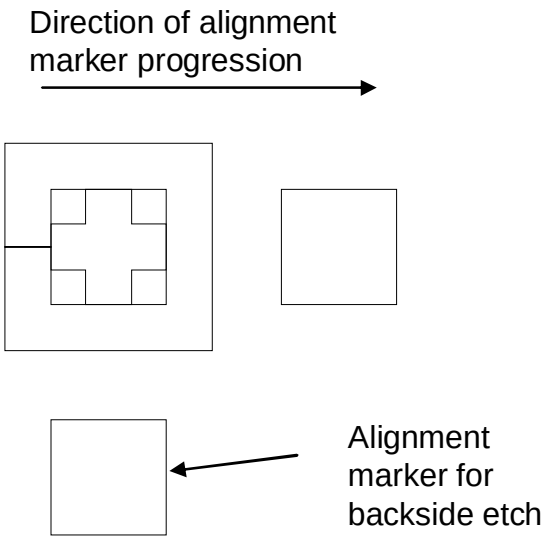


Figure 36: Backside alignment marker in aluminum layer placed offset to the inside to ensure an alignment marker was present for following via alignment.

The marker was positioned in this way to indicate which box to use in alignment of the backside etch. It also had the additional benefit of allowing more infrared light through the markers due to the position of the infrared sources on the contact aligner. Had the markers been positioned at the original distance, the infrared sources would have been positioned such that markers on only one side of the marker could be seen, making rotational alignment very difficult.

Two sets of alignment markers were used. The larger set had a box size of 500µm square, and the smaller, 100µm square. Three of these sets of larger and smaller alignment markers were positioned on the wafer such that rotational alignment would be simple. One set of the larger and smaller alignment markers can be seen in Figure 37.

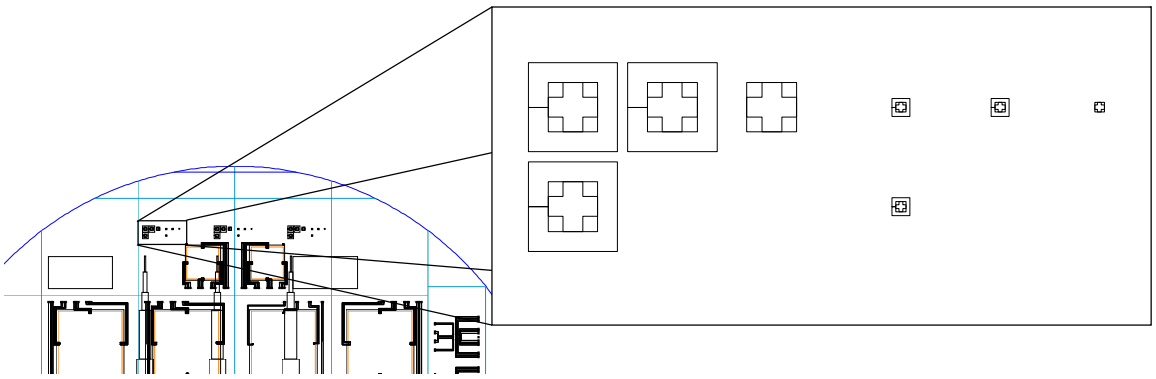


Figure 37: One set of completed alignment markers as they would appear with all masks superimposed.

The final masks were converted to GDSII format using LinkCAD trial software. After conversion, L-EDIT was used to verify the conversion and appropriately combine the layers as needed. A table of relevant mask data is shown in TABLE 1, and more complete mask figures can be found in APPENDIX A.

TEST WAFER PROCESSING

With the wafer design complete, fabrication of the pressure sensors began. In processing the wafer, the first general task is to dope in the piezoresistive devices, followed by diaphragm etching, and finally via and line creation.

Device Fabrication

Oxidation (Step 2)

Recalling the process flow outlined in the Process Design section of this document (Figure 15), oxidation is the first process to be performed on the wafer. Oxidation is the process by which silicon is converted to silicon dioxide (oxide). Silicon undergoes this conversion in the presence of oxygen, so a thin layer of oxide is formed when exposed to air under ambient conditions. This layer of oxide is called ‘native oxide,’ and is on the order of approximately 1-2nm thick [21]

For the diffusion process, it is necessary to have exposed silicon in the areas where the devices are to be created, and mask the remaining area of the wafer. One method of achieving this mask layer is to use photoresist from a lithography process to mask the diffusion. However, this is typically not a suitable masking method due to the high temperatures and other extreme conditions during the processes for which the mask is needed. A better method is to grow an oxide layer on the surface of the wafer which can then be patterned and etched to be used as the masking layer. To create a mask out of

oxide, it is necessary to have a much thicker layer than the native oxide provides. Diffusion of the dopant will still occur in the oxide, however, it will not reach the silicon underneath the masking layer. Figure 38 illustrates this effect.

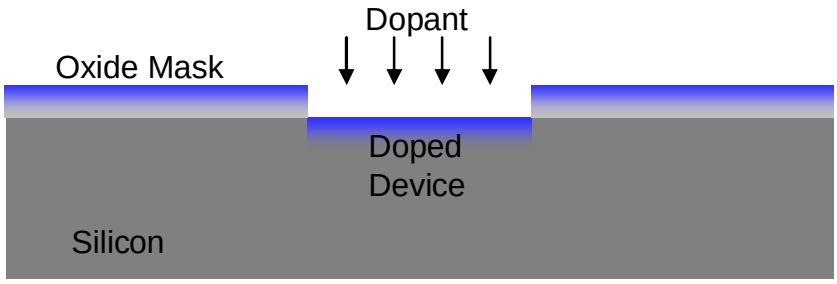


Figure 38:Dopant will penetrate into oxide, but will not reach the silicon below.

The oxidation process is accelerated at higher temperatures, allowing thicker oxide layers to be created in a furnace. Oxides grown through thermal processes are called ‘thermal oxides.’ During growth of a thermal oxide, the growth rate slows as the oxygen has to diffuse through the oxide layer to react with the silicon as the silicon-oxide interface. This limits the achievable thickness of thermal oxide to 1µm

If an oxide layer of 1µm is desired, it is typically done through a wet thermal oxidation process. This process is identical to a dry thermal oxidation, except that water vapor, in addition to oxygen, is passed into the furnace during processing. The reaction of silicon with the water vapor produces silicon dioxide more rapidly, but at the expense of oxide quality. The quality of the oxide, in terms of its density and breakdown voltage, is better with a dry oxide, so an oxide to be used as a critical insulating layer would perform better if it is created using a dry oxidation method. For diffusion and etch mask oxides, wet oxides are preferable. [22]

Growth of oxide also consumes silicon. The amount of silicon wafer thickness lost due to oxide growth is approximately 44% of the final oxide thickness [23]. This effect is illustrated in Figure 39.

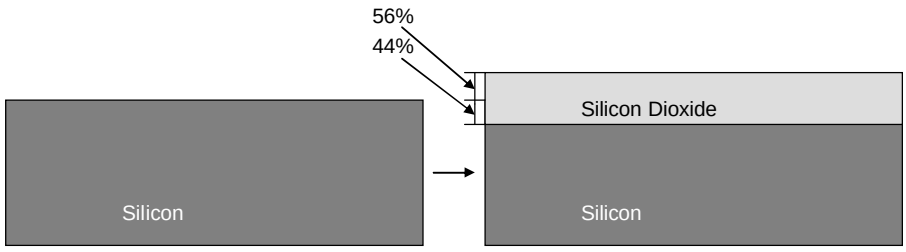


Figure 39: Silicon consumed during thermal oxidation

Because the silicon wafer used is 525µm thick, and the final diaphragms 140µm, the effect of silicon consumption during oxidation is small. With no more than three oxidation steps, all creating less than 1µm of oxide each, the amount of silicon thickness consumed is no more than 2-3µm, approximately 2% of the final diaphragm thickness.

The oxidation process used for the first oxide layer was a typical wet oxidation at 1050°C for 90 minutes. The furnace used can be seen in Figure 40.

Figure 40: MODU-LAB Oxidation furnace

The oxide furnace was first heated to 600°C, with nitrogen gas flowing to the chamber. At 600°C, a quartz rod was used to remove a quartz wafer boat from the furnace. These can be seen in Figure 41.

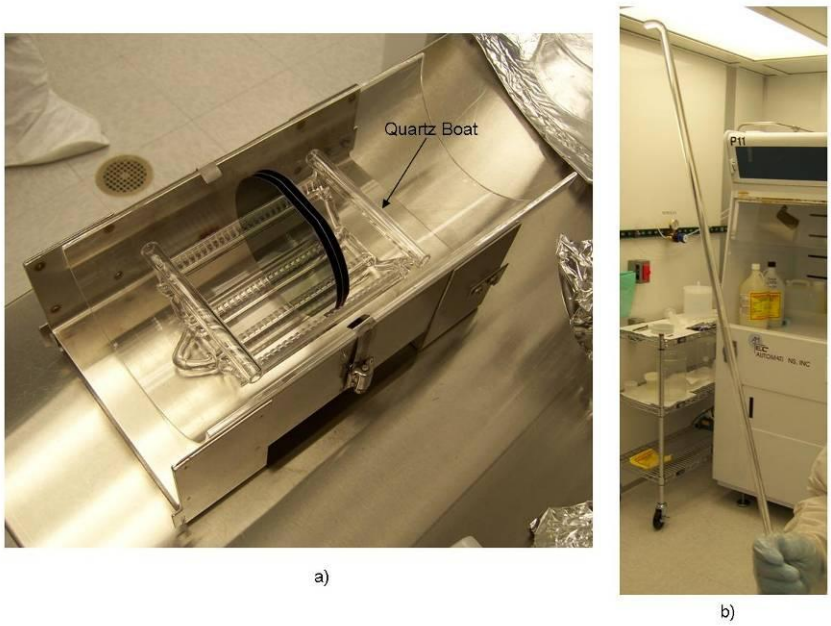


Figure 41: a) Quartz boat which hold wafers during oxidation. b) Quartz rod used to insert the quartz boat into the oxidation furnace.

Nine wafers were then placed in the boat at even increments using the entire length of the quartz boat. Dummy wafers were placed at the ends of the boat, as gas flow through the chamber often leads to thickness variation between the end and middle wafers. The boat and wafers were slowly slid back into the furnace, at a rate of approximately 6 inches per minute, in order to ensure that thermal shock would not crack the wafers. The furnace was raised to 1050°C, nitrogen flow was disabled, and oxygen flow enabled for 90 minutes, which is the approximate time needed to create a sufficiently thick masking

layer. The oxygen flowed through a bubbler which contains boiling water. This carries water vapor to the oxidation chamber, enhancing the oxidation rate. After the 90 minutes had elapsed, the oxygen flow was disabled, the nitrogen flow enabled, and the temperature allowed to fall slowly. At approximately 600°C the wafers were removed, again at a rate of 6 inches per minute. At 300°C the nitrogen flow was disabled, completing the process.

The thickness measured using a device called a Nanospec (Figure 42), was found to be approximately 0.58-0.61µm.

Figure 42: Nanospec equipment used to determine thicknesses of various films.

Photolithography (Step 3)

In order to create the openings in the oxide to create devices, it must be patterned first. Photolithography is the method used to pattern micro-scale features. Three primary steps are involved in photolithography: spin coating, exposure and development. Spin

coating is the process by which liquid photoresist is applied with a consistent thickness to a wafer. Exposure is done to expose the photoresist to light which changes the solubility of the resist to developer. Development removes the soluble photoresist from the wafer, resulting in a wafer patterned with developed photoresist.

To spin coat a wafer, it is placed on a vacuum chuck, photoresist is poured directly onto the wafer, and the wafer is rapidly spun in order to create a uniform thickness. The spinning of the wafer produces an outward force on the photoresist, as shown in Figure 43.

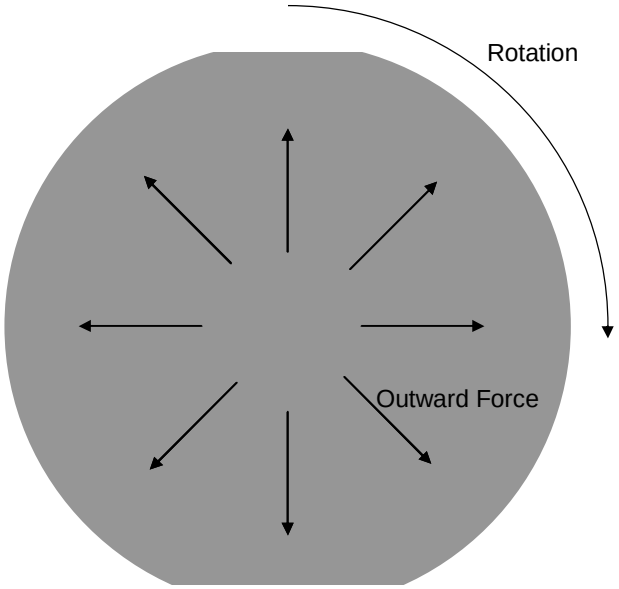


Figure 43: Illustration of spin-coating process

The most significant parameters affecting film thickness are the spin speed and spin time. The photoresist used was Shipley 1813, which specifies that it will produce a film approximately 1.2-1.3µm thick at 4900 rpm spin speed for 30 seconds. The thickness can be controlled by varying the spin speed and time if necessary. A thicker film may be

desired if uniformity is poor to ensure full wafer coverage, and is easier to achieve, while a thinner film is advantageous for small mask feature sizes. Another parameter which can affect film thickness is the exhaust volume. Because the photoresist will dry as the spin coating occurs, higher volume of exhaust speeds the drying and makes for a thicker film. This increase in thickness results in a poor thickness uniformity, however, so exhaust volume is typically desired to be low. [24]

Film uniformity can be affected by a number of factors in addition to exhaust volume, such as spin speed, wafer cleanliness, and dispense amount. If the spin speed is too high, streaks can appear on the wafer, as in Figure 44.

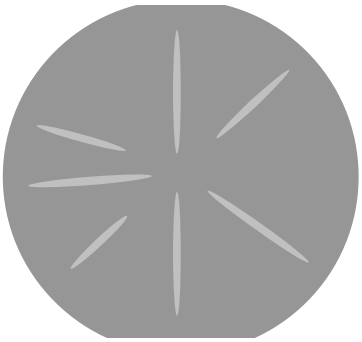


Figure 44: Streaks in the photoresist due to high spin speed. Note that the streaks are typically multi-colored due to interference produced by the thickness change.

A wafer that has particles on it will also produce these streaks, in addition to pinholes in the resist. With an insufficient dispense volume, areas of the wafer may be uncoated entirely as in Figure 45.

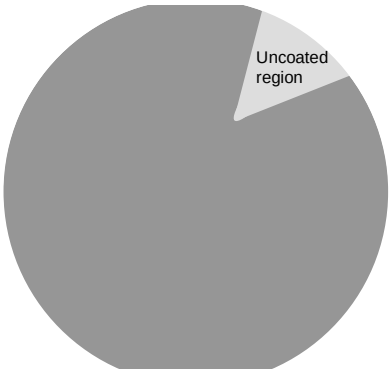


Figure 45: Wafer partially uncoated due to insufficient dispense of photoresist

Before the spin coating process could be done, the wafers were first placed in a vapor prime oven, pictured in Figure 46.

Figure 46: Vapor prime oven used to dehydrate wafers prior to spin-coating

The purpose of this oven is to dehydrate the wafer, improving photoresist adhesion. The oven cycles vacuum, nitrogen, and hexamethyldisilazane (HMDS) in order to excess water from the wafer. During this process, the S1813 photoresist was filtered and poured

into a 50mL beaker. After the vapor prime process, the wafers were allowed to cool prior to spin coating.

The spin coating process was done on a BREWER spin-coater shown below in Figure 47.

Figure 47: BREWER spin-coater and attached hotplate in fume hood.

The process began with centering the wafer. Following centering, a previously configured program was initiated which begins with a 2000 rpm, 3 sec spin to attempt to force particles off of the wafer. This was followed by a 15 second rest period during which the photoresist was applied by pouring enough photoresist to cover approximately 50-75% of the wafer. It was found that only about 5 seconds are needed to pour out the resist, so only the last 5 seconds of the pouring period were used in order to avoid resist thickening prior to spinning. The wafer then accelerated at a rate of 500 rps to a final speed of 4900 rpm, which continued for 30 seconds until decelerating to a stop. The

wafer then underwent a ‘soft baking’ process at 115°C for 60 seconds on the hotplate pictured in Figure 48.

Figure 48: Hotplate used in wafer ‘baking’.

This soft bake step serves to promote adhesion, and a visible improvement in thickness uniformity was observed after soft baking. The resultant photoresist film produced using this method was measured to be 1.3-1.5µm thick (using the Nanospec).

Immediately following the spin coating process is exposure. Exposure is the process by which the solubility of the photoresist to developer is changed using UV light. It is important that exposure is done immediately following spin coating. Ambient white light will slowly expose the photoresist, creating undesired results. For this reason, cleanroom lithography areas are lit with a yellow light in order to eliminate wavelengths which affect the resist.

Photoresist can be either positive or negative as discussed previously, meaning that light either increases solubility or decreases it, respectively. The commonly used resist available in the MMF is positive Shipley 1813, and was used for all lithography steps.

The quality/resolution of exposure depends on exposure intensity and exposure time. Exposure dosage is the product of exposure intensity and time. The plot of exposure dosage vs. photoresist thickness is shown in Figure 49. [25]

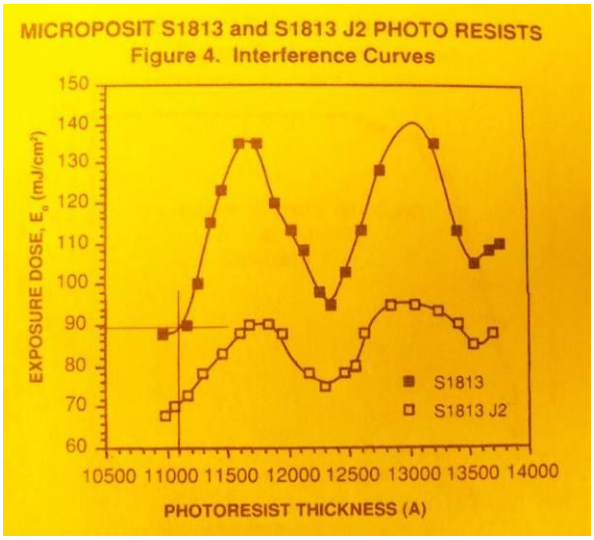


Figure 49: Image of plot of exposure dose vs. photoresist thickness to achieve proper exposure. S1813 was used.

For approximately 1.3-1.4μm of photoresist, an exposure dose of around 110mJ/cm^2 is required to fully expose. The approximate light intensity was 19.7mW/cm^2, meaning about 5-5.5 seconds is required to fully expose the resist. It was found in practice that 5 seconds of exposure produced unwanted effects, and was reduced.

The of incorrect exposure dosage will affect the resolution of the masks. Too high of an exposure time will lead to extra photoresist being exposed, creating jagged edges cut into the photoresist. Too low of an exposure time will create jagged edges of photoresist

in open areas, and may leave photoresist spots or thin layers of photoresist in open areas which will prevent subsequent etch steps from proceding properly. The edge effect issues due to exposure issues are illustrated in Figure 50. Spots of photoresist are shown in Figure 51.

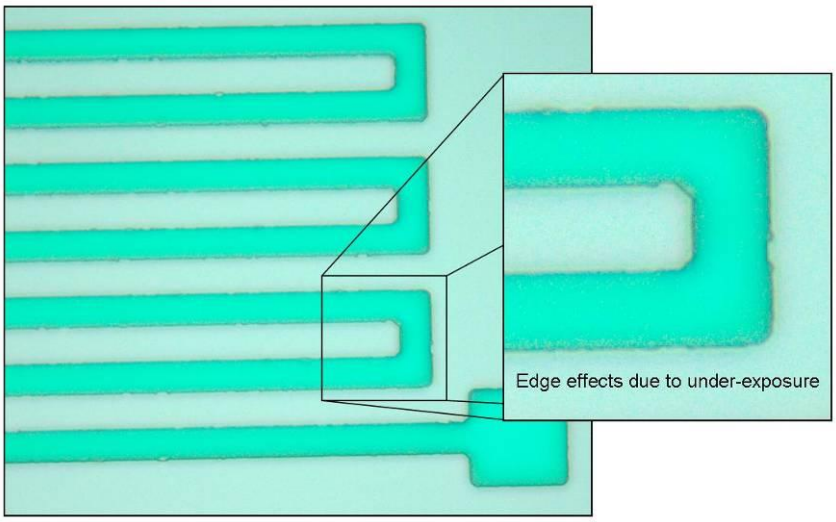


Figure 50: Image of edge effects resulting from underexposure.

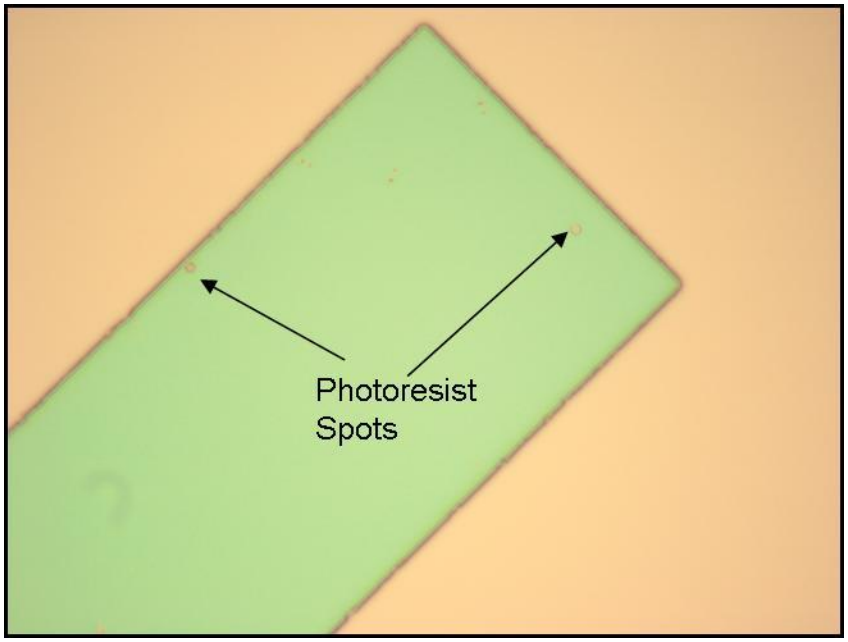


Figure 51: Image of photoresist spots which may occur if photoresist is underexposed.

The exposure process was done on an ABM contact aligner as shown in Figure 52. Contact aligners place the mask and wafer in contact in order to produce high resolution features, but this comes at the expense of possible damage due to particles that may be present between the mask and wafer.

Figure 52: ABM contact aligner used for alignment and exposure.

The wafer was placed in a vacuum chuck, and the mask placed on a vacuum stage which could be raised (Figure 53).

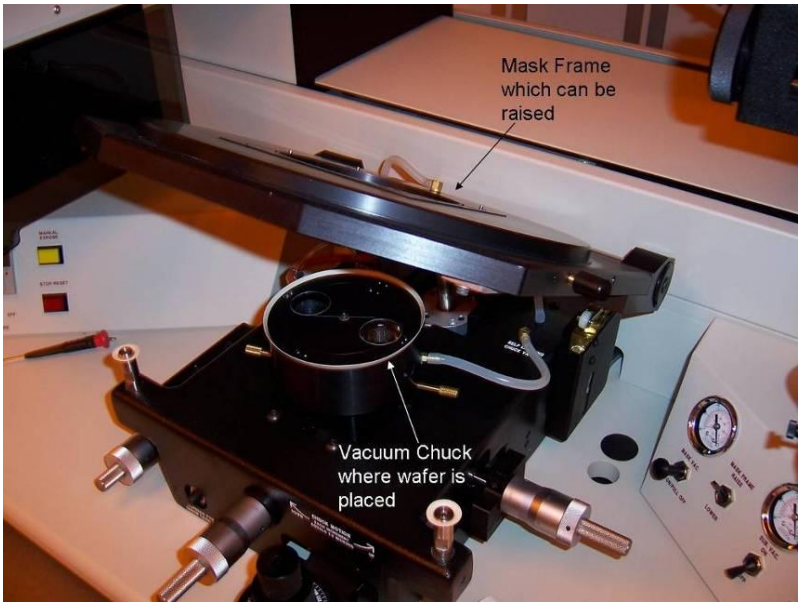


Figure 53: Vacuum chuck on which the wafer is placed. Mask frame on which the mask is placed is raised. Note the lenses for the infrared light source used in backside alignment.

The wafer chuck was lowered to avoid contact with the mask as it was lowered. At this point, the wafer was raised into contact using a slip micrometer. Typically, the wafer would then be lowered and aligned, however, there is no need for alignment during the first photolithography process. Due to the method of mask creation and the positioning of the wafer chuck, the applied masks were rotated 90° clockwise from their position in the mask file. It was determined that this would have no effect on the final sensors, aside from an easily compensated rotated crystallographic alignment.

The masks were placed in vacuum contact and exposed to a Mercury light source at 19.7mW/cm^2 intensity for 2-4 seconds depending on the desired minimum feature size.

The light source in position above the vacuum chuck and mask frame is shown in Figure 54.

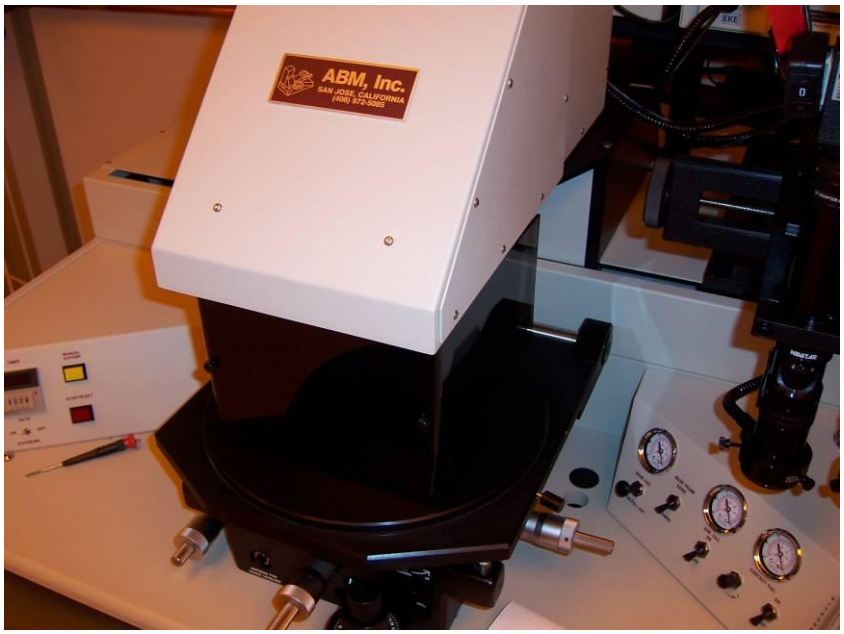


Figure 54: Light source in position above the wafer chuck.

For the first lithography step, the exposure time was low in order get a more accurate result for the small features. The exposure dose was slightly increased in subsequent exposures due to a thin layer of photoresist which remained after development. Increasing the exposure time resulted in poorer resolution, but alleviated the need to remove this photoresist layer prior to etching.

Following the exposure, the wafer is immediately developed, for the same exposure reasons stated previously. The wet bench used in developing the photoresist is depicted in Figure 55.

Figure 55: Wet bench used in development of the photoresist.

The developer used in this case was MF-319, a dilute solution of TMAH. A small amount of developer was poured into a dish, and the wafer was submerged, with gentle agitation, for 45 seconds. During the first few developments, it was found that removing the wafer from the dish was difficult, which often resulted in overdevelopment. It was later found that this overdevelopment created significant rounding of the corners in the patterns, as shown in Figure 56.

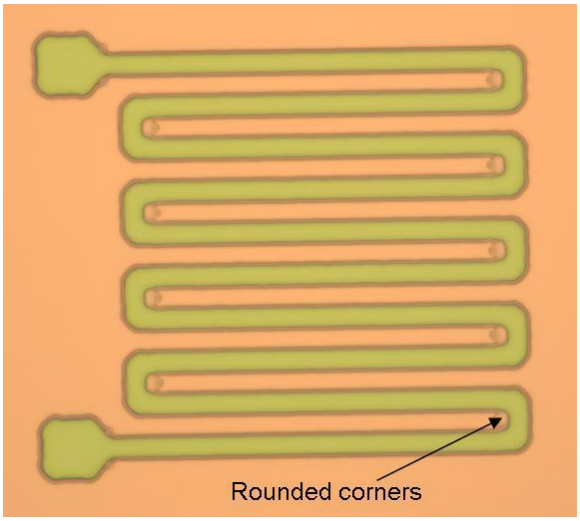


Figure 56: Overdeveloped serpentine resistor device exhibits rounding of corners.

The devices all contain some degree of rounding, but because current flows largely away from corners, this rounding should prove insignificant. It was possible to achieve at least 3µm grid feature sizes with the parameters used above, with 2 and 1.5µm feature sizes being created less reliably. This resolution was deemed appropriate for all layers, with only the via layer being challenging with 3µm feature sizes.

After the development was finished, the wafers were hard baked for another 60 seconds to remove solvents and promote adhesion. Hard baking was not performed for the first lithography step, due to human error, which resulted in poor adhesion during the subsequent etch process, to be discussed later.

Some of the resultant devices after the initial lithography step can be seen in Figure 57.

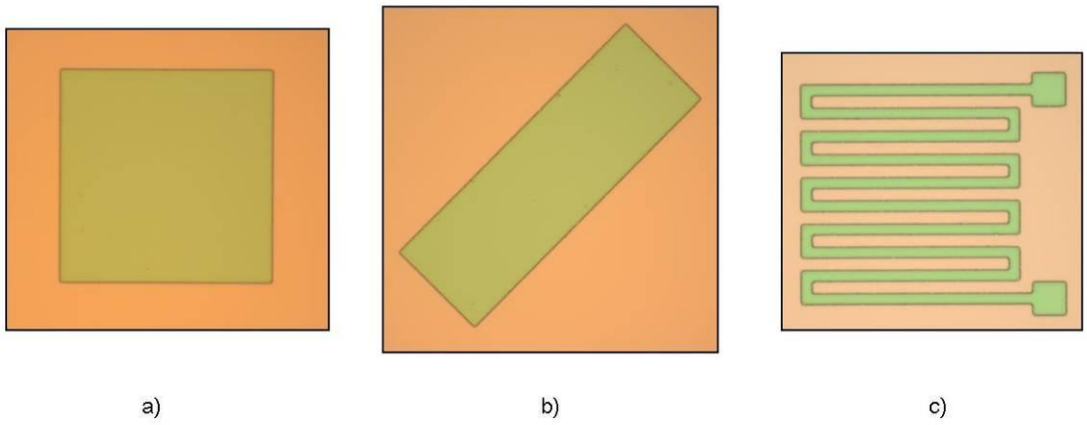


Figure 57: Device regions in photoresist after first lithography process a) van der Pauw (VDP) structure b) Four Terminal Transducer (FTT) and c) Serpentine Resistor.

Oxide Etch #1 (Step 3)

As discussed previously, the patterned photoresist serves as a poor mask for most processes, however, it serves well as a mask for oxide etch. The oxide etch process is simply the immersion of the wafers in a buffered oxide etch (BOE) solution for a set period of time. The BOE solution is a 6:1 solution of hydrogen fluoride (hydrofluoric acid) and water. The HF rapidly etches thermal oxide at a rate of 910Å/min. Our oxide layer was approximately 0.58-0.61µm, requiring 6-7 minutes of etch time.

Because pure silicon lies underneath the oxide, the etch time calculation is only for approximation, as other indicators can be used to determine the completion of the etch. First, the oxide layer is a transparent layer, which appears to be a purple or green color depending on the viewing angle. Silicon, however, is opaque and a silver color. The color difference can be seen in Figure 58.

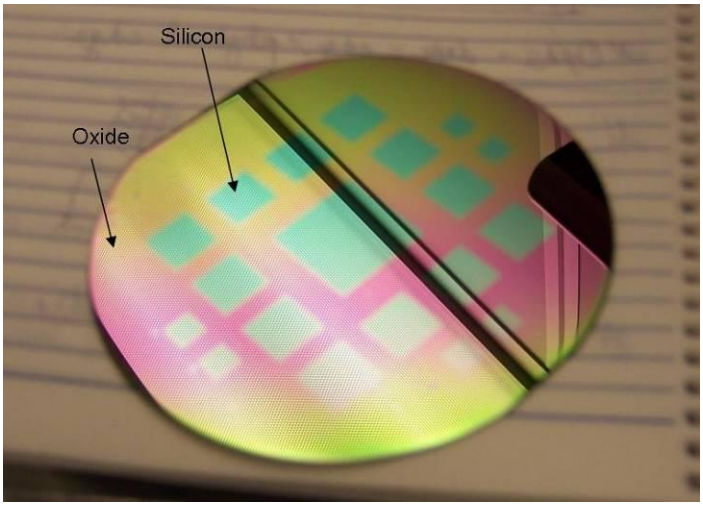


Figure 58: Color difference between bare silicon and silicon dioxide.

While color is a fair indicator of oxide thickness, thin oxide layers look very similar to pure silicon. A better indicator is the behavior of water on the surface of silicon and oxide. Oxide is a hydrophilic, meaning that water forms a thin film on the surface, adhering to the wafer, while silicon is hydrophobic, meaning water will form beads on the surface of the wafer, and more rapidly flow off the wafer. This effect, shown in Figure 59, is a very clear indicator as an etch stop.

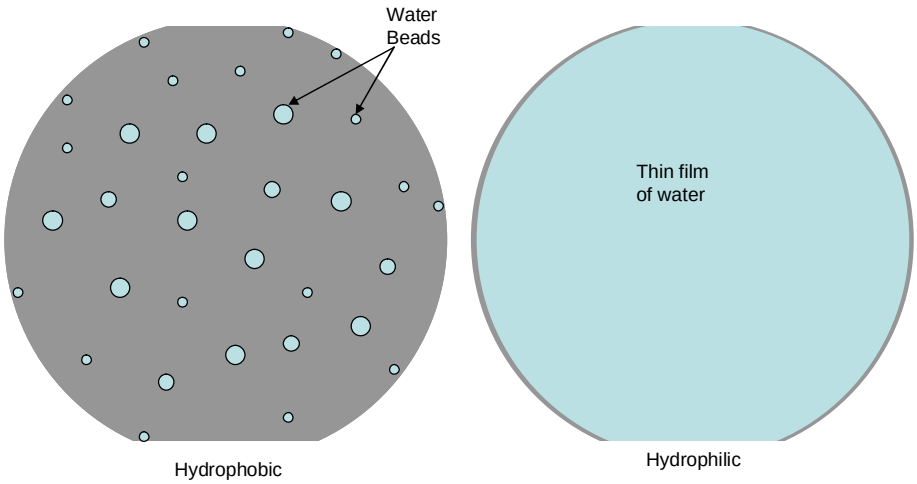


Figure 59: Illustration of the difference between hydrophilic oxide and hydrophobic silicon surfaces.

For the first bulk oxide etch process, the backside of the wafer was not coated with photoresist, leaving the oxide unprotected. The behavior of water on the backside of wafer was therefore used as an etch stop indicator. Initially, one wafer was etched in order to get an approximate etch time, then the remaining eight wafers were etched. After examining the etched devices, it was found that many looked as expected, while many looked similar to the devices in Figure 60. It was determined that this phenomenon was likely the result of a thin layer of photoresist inhibiting the etch in the region, while the color surrounding the device was likely an adhesion issue resulting from the lack of a hard baking step combined with the etching process.

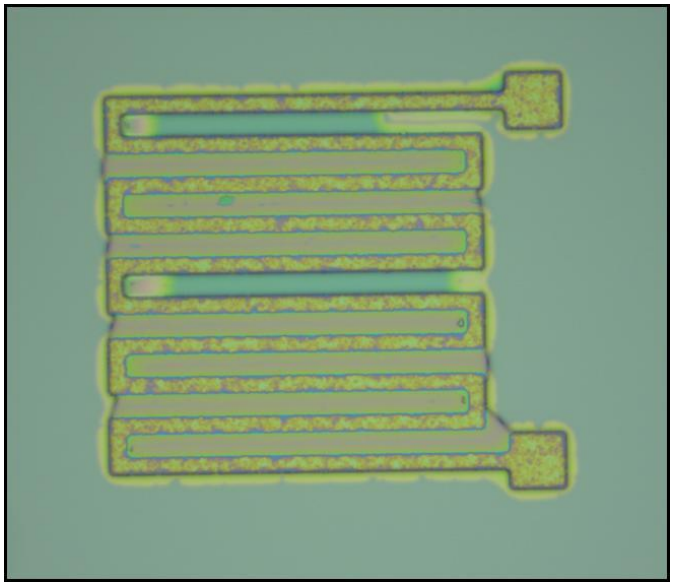


Figure 60: Poor device after oxide etch, prior to removal of photoresist.

Many of the devices appeared to be severely undercut due to this adhesion issue, while others appeared to be unaffected as shown in Figure 61.

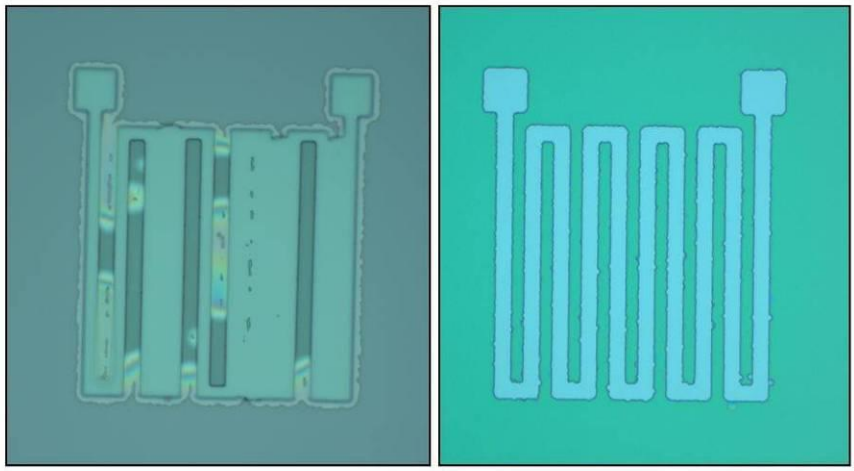


Figure 61: a) Destroyed device oxide mask resulting from poor lithography. b) Poor, but acceptable serpentine resistor oxide mask. Note that the photoresist has been stripped.

Based on this diagnosis, it was determined that a plasma ashing process would be used to remove the thin photoresist layer. The wafer would then be etched in BOE to remove the remaining oxide under the photoresist layer. Because the oxide layer is thin, the degree of undercutting was found to be small, nearly undetectable, and acceptable to avoid stripping the oxide and beginning again. The undercutting led to slightly more rounding of corners in the devices, but once again, this is assumed to be insignificant.

The ashing process uses an oxygen plasma by exciting the gas in vacuum with a radio frequency electromagnetic field. This ionizes the gas, and directs it downward onto the surface of the wafer. Ashing is a specific type of plasma etching used to remove photoresist. Plasma etching can be used to etch many different materials, and is often called dry etching or reactive ion etching. Plasma ashing was done on the March Plasma Etcher shown in Figure 62.

Figure 62: March Plasma Etcher used in plasma ashing process. The black box on the left is the RF power controller.

After initial power and gas flow setup, the ashing process involved first placing the wafer in the process chamber and evacuating the chamber. Oxygen was then flown to the chamber. After the chamber pressure had equilibrated, RF power was enabled in the system, and a plasma was created in the chamber, creating a faint white/purple glow through a small viewing window. It was found that the power needed to be enabled for 45 seconds in order to completely remove the photoresist layer, because many of the larger VDP devices also contained the photoresist layer. The larger inner open area of the VDP made it clear when a device had not had its layer completely removed. The device shown in Figure 63 is one which had undergone BOE after an insufficient amount of ash time.

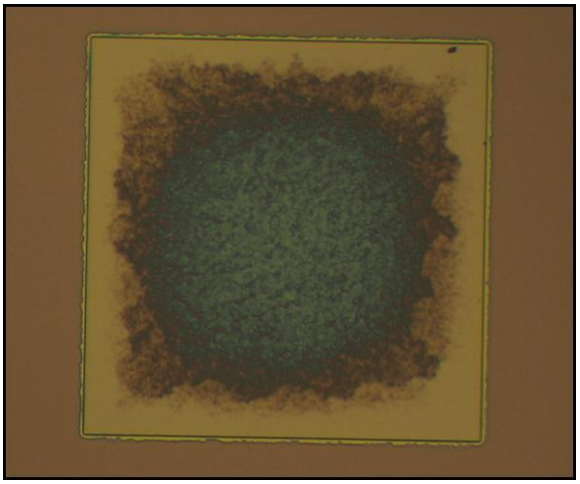


Figure 63: VDP device region which has had the thin photoresist layer partially removed through plasma ashing, and has been oxide etched. Further ashing and oxide etch removes the residue.

It can be seen that the areas near the edges of the device have been etched, but increased etch time would not significantly affect the inner area. After more ashing was done, the inner area of the device etched properly. Once all wafers had been properly etched, the photoresist was removed using Nanostrip, which is a pre-mixed solution of sulfuric acid and hydrogen peroxide.

Upon inspection after resist stripping, it was found that a number of devices would clearly not function due to the undercutting joining legs of the serpentine resistors. These devices were considered destroyed. All destroyed devices were serpentine resistors, while some of the VDP and FTT devices were enlarged due to undercutting. While the affect on VDPs and FTTs was undesirable, the device functionality will be unaffected due to the positioning of vias within the doped region. Some destroyed resistor devices can be seen in Figure 64.

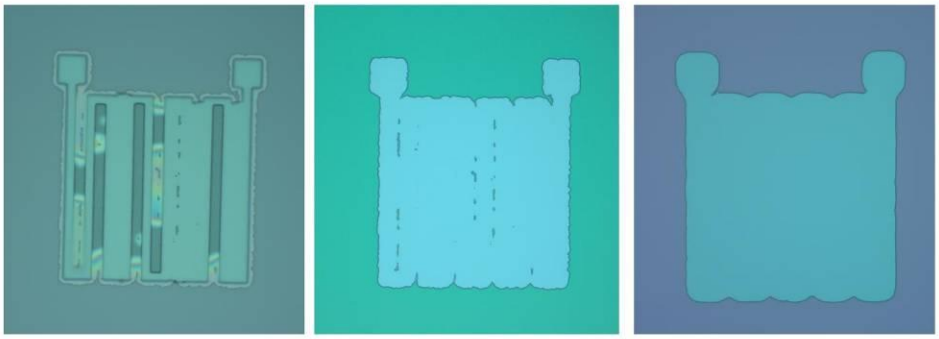


Figure 64: Three destroyed serpentine resistor devices due to the poor photoresist adhesion and resulting undercutting.

Each wafer was mapped for destroyed resistor devices to determine which wafers would likely work properly, and which would have few working serpentine resistors. The mapping was done partially to determine the extent of the damage, and partially due to the capacity of the boron diffusion oven used in the following step being limited to six wafers. Three wafers with the worst damage were discarded.

Diffusion (Step 4)

The diffusion process, also called doping, is the process by which impurities are added to the silicon lattice, changing conductivity. Silicon has four valence electrons, and rather poor conductivity. To improve the conductivity of a silicon region, silicon atoms in the crystal lattice are exchanged for atoms with either one extra valence electron, called n-type doping, or one less valence electron, called p-type doping. The introduction of these atoms is done through diffusion by placing the wafer in a high temperature oven in the presence of sources of these atoms.

The doping done to the wafers was a p-type doping, using boron (B). The oven used was similar to the oxidation furnace, and the overall procedure the same, with a few differences. Primarily, no oxygen was enabled during the process, as oxide growth was undesired. The process was run for 120 minutes rather than 90, and the quartz boat contained three BORONPLUS Boron diffusion sources as shown in Figure 65.

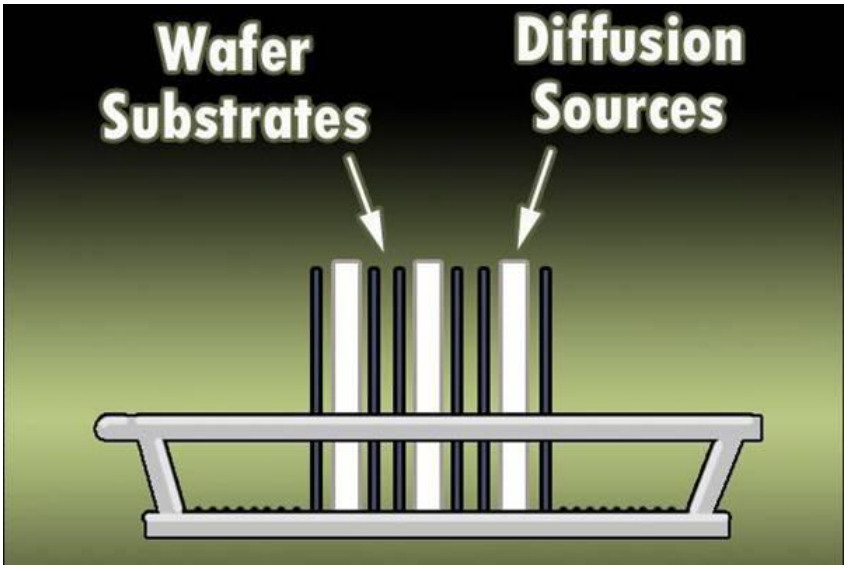


Figure 65: Illustration of diffusion sources and wafers in quartz boat for boron diffusion. [26]

The diffusion process changed the bare silicon regions (created in the previous step) into brown colored regions. It should be noted that holes and scratches in the masking oxide layer created some additional doped regions, particularly at the edges of the wafer. The extra doped areas should have no effect on the functioning devices, provided that they do not contact any of the device doped regions.

After the diffusion was complete, the oxide was etched using the same BOE process used to pattern the oxide mask. At this point in the process, the first overall step of

piezoresistive device creation was complete. The next overall step was creation of the thinned pressure diaphragms, which begins with another oxidation.

Bulk Silicon Etch of Diaphragms

Wet Oxidation (Step 6)

Because the etch process for creation of the pressure diaphragms is long, and the etchant, TMAH, slowly etches oxide, it is desirable to have a thick oxide layer of approximately .9-1µm. To perform this oxidation, the procedure is the same as that of the initial oxidation don in step 2, except that the oxidation time is longer. The process time is also increased to three hours to achieve a thick oxide layer. The thickness of the oxide was approximately .9-1µm.

Al PVD (Step 7)

The frontside of the wafers contains the alignment markers, but for backside etching, it is necessary to align a backside mask to the front of the wafer. As stated in the wafer design section, this can be accomplished by first applying a layer of aluminum to the frontside of the wafer, patterning it with alignment marks, and etching these alignment marks such that infrared light, which is transparent to silicon but not aluminum, applied to the frontside can be seen from the backside of the wafer. The first process step to achieve this is the deposition of a layer of aluminum.

The application of a layer through vapor means is referred to as physical vapor deposition (PVD). A similar process called chemical vapor deposition (CVD) involves a chemical reaction of two species in proximity to the wafer. In physical vapor deposition, no chemical reaction occurs. Typically, PVD is used to deposit metal layers. Two methods of PVD are available in the MMF: evaporation, and sputtering. Evaporation is the simpler of the two, and is done by simply heating a sample past its melting point under vacuum. The material vapor produced then diffuses throughout the chamber, coating the walls of the vacuum, and the wafer side facing the sample. Sputtering PVD is done by bombarding a sample with atoms under vacuum, typically Ar, which ejects atoms from the sample, which then travel to the wafer and are deposited onto it. The advantages of sputtering is that materials with very high melting points, for which evaporation is difficult or impossible, can be sputtered relatively easily. Evaporation, however, is a simpler, and much quicker, process.

Because Al has a low melting point relative to other metals at around 660°C, evaporation was chosen. Before Al evaporation can be performed, the necessary sample size must be determined. The sample size is directly proportional to the resultant Al film thickness. If the Al is assumed to radiate outward evenly in all directions, the following equation can be used to determine the resultant film thickness

$$thickness = \frac{W * L * t_{foil}}{4\pi(13.5cm)^2} \tag{39}$$

Where W is the width of the aluminum foil sample, L is the length of the aluminum foil sample, and t_{foil} is the thickness of the cleanroom aluminum foil, which is 50.8µm.

The 13.5cm^2 in the denominator is the approximate distance from the filament to the wafer surface. This equation is a result of dividing the volume of the aluminum by the surface area of the sphere it projects.

Initially, it was a concern that the previous alignment markers would be difficult, or impossible to see underneath the aluminum layer, so it was desired to have the aluminum layer relatively thin at about 0.5-0.6µm. This proved to be an unnecessary concern, however, as will be discussed later. Using this thickness, it was determined that a sample size of 22cm^2 would be needed. It was suggested that a sample size of between 30 and 40cm^2 be used, based on the empirical data of previous users, and the ease and accuracy of cutting a sample. The choice was made to use 30cm^2.

The aluminum evaporator equipment is shown in Figure 66.

Figure 66: MODU-LAB aluminum PVD system.

Performing the PVD involved first cutting an appropriate sample size, which was rolled and placed in a tungsten filament inside of the Al evaporation tool. Some tungsten filaments are shown in Figure 67.

Figure 67: Tungsten filaments used in Al PVD.

The wafers were placed in a hanging assembly above the filament. The hanging assembly held only four wafers, and required clips to attach the wafers. The clips left small marks on the wafer.

The evacuation then began with a rough pump of the chamber and turbopump. Once roughed, the turbopump was engaged and the chamber was slowly evacuated to below 50 mTorr. Power to the filament was then enabled, and slowly increased. As the filament power increased, the Al began to melt and evaporate. With the increase in particles in the chamber, the vacuum worsened, decreasing the mean free path between the sample and the wafer. It was important to balance power to the filament with vacuum quality in order to ensure this mean free path would be long enough such that the Al particles could freely move to the wafers. Under perfect vacuum circumstances, it would be ideal to rapidly heat the filament to ensure the aluminum would evaporate rather than melt and drip away. During the process, it was possible to see the filament and sample to determine the quality of evaporation.

Once the sample had been completely evaporated, filament power was disabled, and the chamber was vented. After waiting for the system to cool, the wafers were removed.

Inspection of the wafers revealed that it was very difficult to see the alignment marks under a microscope, and would be difficult to see them under the contact aligner microscopes. Upon observing under dark field illumination, it was found that the features were much easier to observe. The dark field illumination images can be seen in Figure 68.

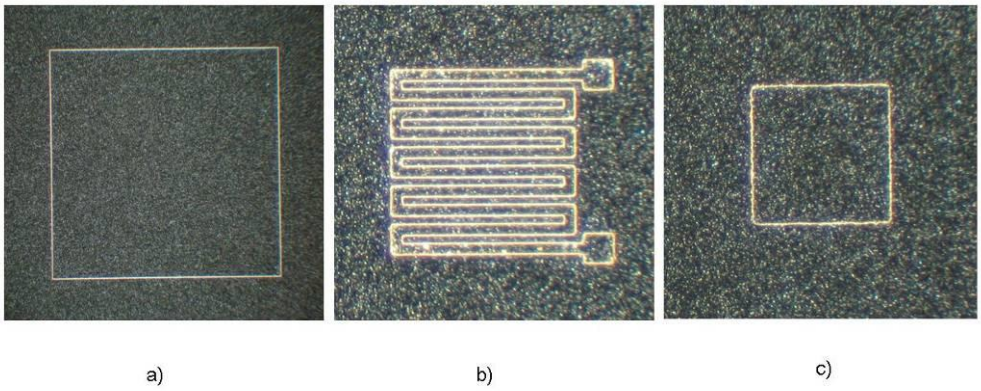


Figure 68: a) Large alignment marker box, b) serpentine resistor device, c) small alignment marker box after aluminum PVD under dark field illumination.

Dark field illumination is used to highlight physical edges. It does this by shining light around the field of view which diffracts off of edges and can be seen. Because the doping phase changed the composition of silicon in the doped areas, subsequent oxidations created oxides at different rates inside and outside of these regions. This rate difference led to a physical step at the edges of the doped regions. The edges are nearly undetectable under normal light field, as both sides of the step have the same aluminum surface, but they are easily detectable under dark field illumination.

Photolithography #2 (Step 8)

The photolithography process used to pattern the alignment markers onto the Al layer was the same as that used to etch the doping mask layer, with a few exceptions. First, the ALALIGN mask was used. This mask needed to be altered in order to avoid bulk silicon etch issues later. Guides were previously created to make identification of the alignment marks easier during mask alignment, but it was later realized that these areas would allow for BOE to etch the underlying oxide, leaving the silicon to be etched by TMAH during bulk etching and destroying the wafer. In order to remedy this, these areas were simply blocked from being exposed to the infrared light by covering them with an opaque material during exposure, leaving only the alignment markers exposed.

Another change was alignment to previous alignment markers now needed to be done to ensure the devices were placed properly on the diaphragms. Recall that the features on the wafer were very difficult to see under light field due to the Al layer, so all alignment was done using dark field light sources. Alignment was simplified by attempting to orient the wafer correctly by eye prior to fine adjustment. Fine adjustment was done by translating or rotating the wafer underneath the mask with the optics shown in Figure 69.

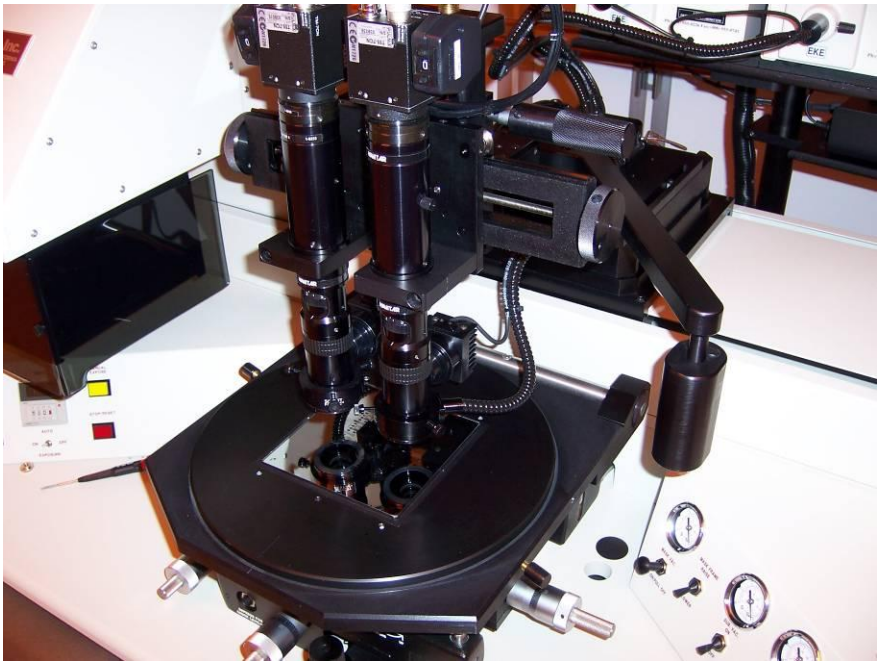


Figure 69: Optics used to align wafers to mask atop the mask frame.

With six sets of alignment markers, rotational alignment was reliable, while translational alignment proved slightly more difficult. Two of the remaining six wafers had slight translational misalignments of approximately 10-15µm as shown in Figure 70.

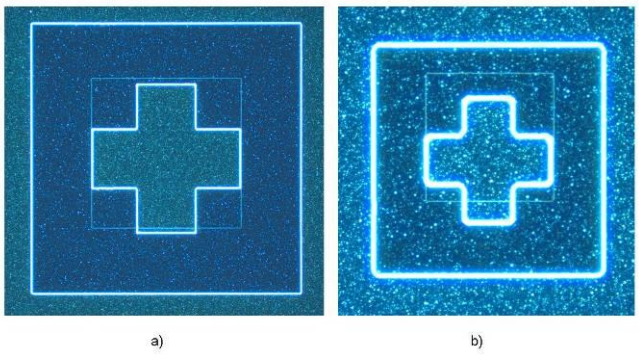


Figure 70: Downward misalignment seen on a) a larger alignment marker and b) a smaller alignment marker

While this degree of misalignment would be unacceptable for via and line placement, it is acceptable for the diaphragms due to their large size and the distance of the devices

from the diaphragm edge. Also, the alignment marks during the bulk silicon etch portion of the processing are not used during via and line mask alignment, so misalignment will not propagate. More accurate alignment is shown in Figure 71.

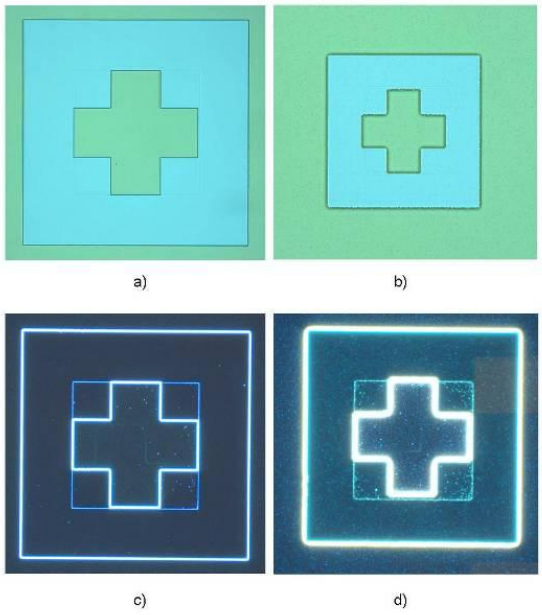


Figure 71: Larger (a and c) and smaller (b and d) alignment markers under light field (a and b) and dark field (c and d) illumination. The cross marker is in photoresist, while the box is the physical edge caused by doping

A final change that was made was to increase the exposure time to 3.5 seconds, and slightly increase development time to about 45-50 seconds. This was done because the alignment marker rounding is not critical, and it was desired to avoid the thin photoresist layer which requires plasma ashing to remove.

Al Etch (Step 8)

The etch used to remove the aluminum from the areas not masked by photoresist uses PAN (Phosphoric, acetic, and nitric) acid etch (PAE). The etching of the aluminum is

similar to that of oxide etch, except that each wafer was etched individually. Each wafer was placed in a Pyrex dish with enough PAE to submerge the wafer, and to etch all wafers without a significant decrease in concentration. The etch time was approximately 5-10 minutes using a 16-1-1-2 mixture of phosphoric acid, acetic acid, nitric acid, and water, respectively. An odd characteristic of aluminum etching with PAE is that a visible etch front can be seen moving across the wafer. With only alignment markers on the wafer, this was not as apparent, but still visible. The resulting alignment markers under light field can be seen in Figure 72.

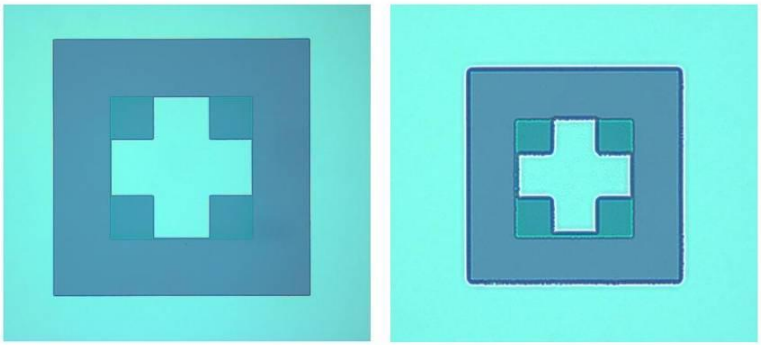


Figure 72: a) Large and b) small alignment markers in aluminum after aluminum etch.

All alignment markers etched properly, without issues resulting from remaining photoresist in the alignment markers. Plasma ashing and subsequent re-etching was therefore avoided.

Backside Photolithography (Step 9)

The photolithography processes for the backside etch regions were all done on the backside of the wafer. Resist was spun onto the backside, followed by exposure on the backside. Alignment was achieved using the alignment markers in the aluminum and a infrared light source being shone from the backside through the alignment markers. The infrared light sources were positioned relative to the alignment markers such that only the center two alignment markers and their smaller equivalents could be seen from the backside during alignment. The infrared light sources shone through the windows shown in Figure 73.

Figure 73: Infrared light sources on the ABM contact aligner vacuum chuck

At times, small areas of the bottom set of alignment markers could be seen, but these served only to aid in rotational alignment, and were not consistently present.

The alignment markers used were placed to the inside of the previous markers set by the boron doping step. The markers were placed in this way to emphasize that these markers are to be used, and that they could not be used for subsequent alignment, as they would be undetectable from the frontside. Another benefit, while unintentional during design, was that this allowed the alignment markers to be seen much easier during backside alignment, as shown in Figure 74. Had the markers been placed in line with the other markers, backside alignment would have proved very difficult.

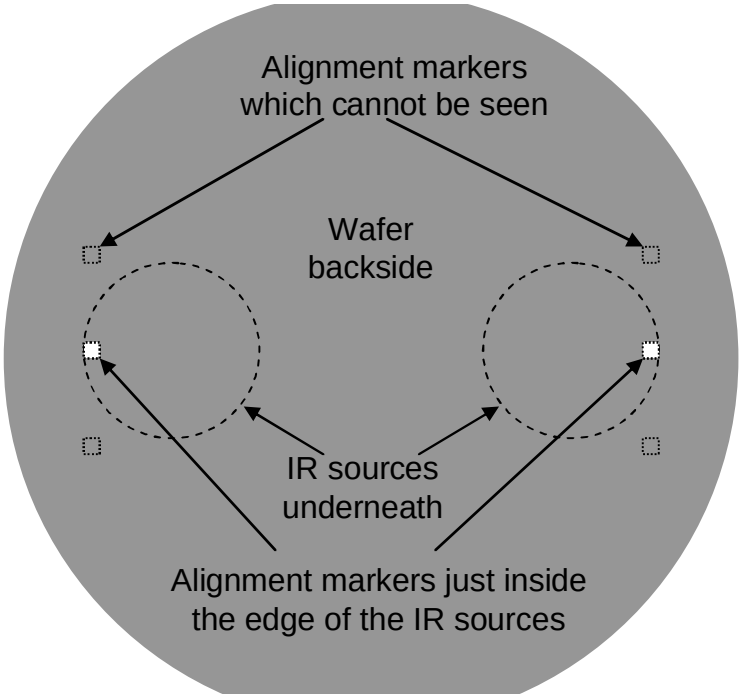


Figure 74: Wafer as seen from the backside during alignment. Note that the alignment markers are not to scale. Had the markers been placed any more outward, they would be undetectable.

Backside alignment was less accurate due to the fact that it was impossible to focus on both the frontside aluminum markers and the backside mask simultaneously due to the wafer's thickness. Focus was done on the cross markers on the mask, while the infrared

light boxes were moved beneath into rough alignment. Due to the size of the diaphragms and relatively large distance from their edges to the devices, the small misalignments due to the lack of focus can be considered insignificant.

As in the aluminum alignment marker photolithography, the exposure time was 3.5 seconds, and the development time 45-50 seconds. Any jagged edges or rounded corners would be insignificant compared to the size of the diaphragms.

Bulk Silicon Etch (Step 10)

After the completion of the photolithography process, photoresist on the backside, and aluminum on the frontside were still present. It was determined that the photoresist could cause problems during the bulk etching process, and was removed with Nanostrip [27]. It was also decided that despite the TMAH etch rate of aluminum being near that of silicon, leaving the layer would not negatively affect the process significantly, but would rather serve as an additional frontside protection layer. Unfortunately, the Nanostrip used to remove photoresist also rapidly etched the aluminum layer, leaving the underlying oxide layer as the only masking protection.

Two methods of TMAH bulk etching were used. Initially, one wafer was placed in a small Teflon cassette and inserted into a large beaker of 25% concentration TMAH at approximately 85-90°C, which was accomplished by heating a hotplate to 135°C. A magnetic stirrer was also used to increase etch rates. The cassette and wafer were then placed in the TMAH solution. After approximately 4 hours of etching, the wafers were removed to determine the etch rate. The TMAH etches silicon rapidly, and oxide slowly.

Using the Nanospec, it was possible to determine the oxide etch rate, which was found to be acceptable when compared to the silicon etch rate. The silicon etch rate was determined using the profilometer shown in Figure 75.

Figure 75: AMBiOS XP-2 Profilometer.

The silicon etch rate was found to be between 13-16µm/hour, depending on the native oxide thickness. That is, the initial few hours appear to have a slower etch rate due to the initial difficulty of etching the native oxide. The wafer was then reinserted into the etchant. The etch depth and rate was checked periodically until the final etch depth of 385µm was achieved after approximately 21-22 hours of etching. The profile of one edge of a completed diaphragm from later wafers can be seen in Figure 76.

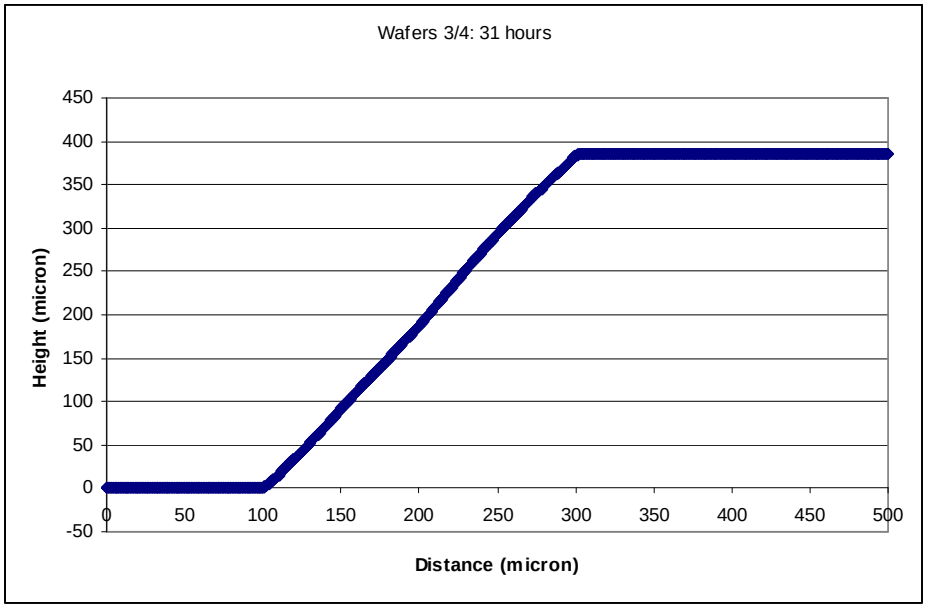


Figure 76: Profilometer data for the edge of one diaphragm. The bottom of the diaphragm is on the left, at 0, and the top is on the right, at approximately 384µm.

Note the sloping wall due to the anisotropic etching TMAH exhibits. In Figure 77, a picture of the wafer after etching can be seen.

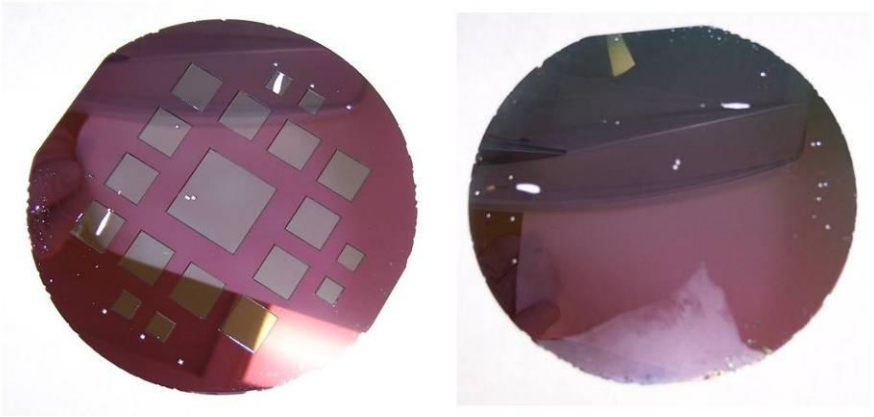


Figure 77: First TMAH etched wafer. Note the numerous imperfections and jagged edge. a) Backside b) Frontside.

Where the wafer has been etched unintentionally, but not entirely through the wafer, imperfections in the masking oxide exist, exposing bare silicon. The edge of the wafer, where the wafer tweezers are used is particularly poor. Where the wafer has been etched completely through, scratches and other imperfections which exposed the silicon on the frontside have etched to meet a diaphragm or other feature on the backside. Note that the alignment markers have been etched entirely through, because bare silicon was exposed on both the frontside and backside. Figure 79 below shows some 10x magnification images of the areas where the etch has completely penetrated the wafer.

While these wafer imperfections are certainly undesired, if a particular diaphragm does not contain any unintentionally etched areas, that diaphragm is still acceptable for testing. The imperfections make lithography difficult, as these holes in the wafer make proper spin coating nearly impossible in areas.

Additionally, oxide imperfections on the frontside create the problem of pinholes. These pinholes are areas where small holes exist in the frontside oxide, allowing TMAH through. Examining the wafer, it was found that these imperfections range from approximately 5µm to 80+µm square. Because TMAH etches anisotropically, it can be determined that these imperfections penetrate approximately 3.53µm to over 56µm into the silicon, and form a sharp point at the tip of a pyramidal pit. Figure 78 illustrates this concept.

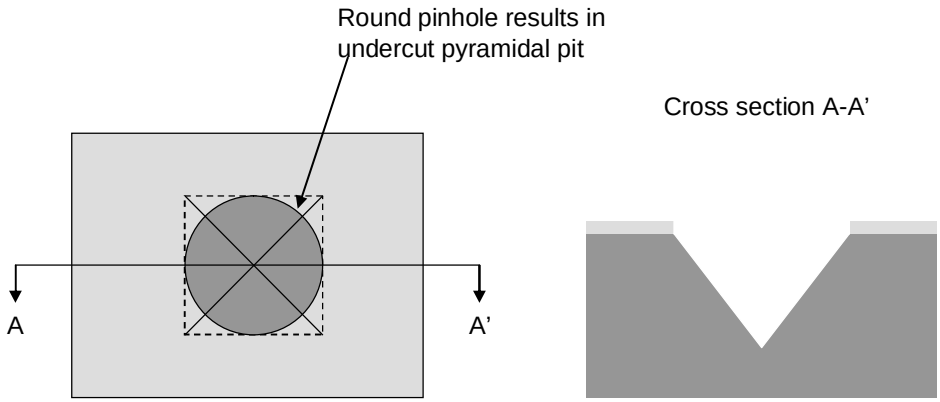


Figure 78: Pyramidal pit formation under pinhole in masking oxide layer.

Images of the pinholes in the wafer under various magnification can be seen in Figure 79. These pinholes will create significant stress concentrations in the diaphragm, thereby reducing the strength of the diaphragm possibly to the point of failure even under low pressure difference. In addition it will greatly alter the resultant stress field under pressurization. Because these pinholes occur throughout the wafer, it is unlikely that any diaphragm will be unaffected. For this reason, it was determined that a process needed to be developed to eliminate pinhole imperfections on the frontside of the wafer.

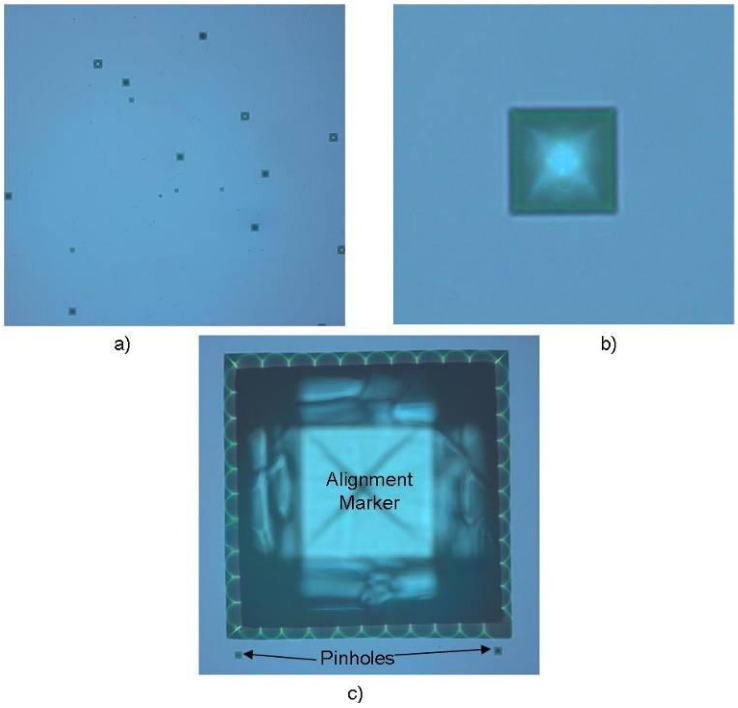


Figure 79: a) Image to illustrate pinhole density. b) Single pinhole. Note that the pyramidal structure is not clear due to the small size and inability to focus over the whole depth. c) Pinholes near the completely etched alignment marker to demonstrate pinhole size.

Two possible solutions were conceived. One is to deposit a layer of chromium (Cr) to the frontside of the wafer, which undergoes negligible etching in TMAH. However, Cr must be deposited by sputtering, which is a lengthy process and can only be done on individual wafers. Another method was to bond a sacrificial wafer to the frontside of the wafer, protecting it from the TMAH. The WaferGrip used in wafer bonding is shown in Figure 80, and a relevant brochure is in the appendix.

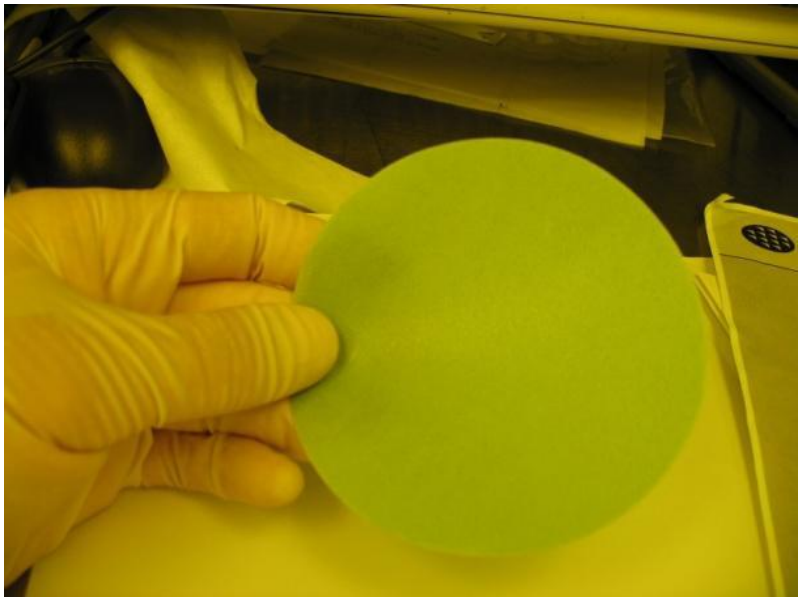


Figure 80: High temperature WaferGrip adhesive. [26]

Unfortunately, the high-temperature WaferGrip adhesive [28] that was used has a melting point of 115°C, which is above the 85-90°C temperature of the TMAH solution, but close enough to where softening and debonding is a concern. To test the possibility of wafer bonding, a small sample of the WaferGrip was bonded between two small test die and placed into the TMAH solution with the hotplate at 115°C. A small sample of unbonded WaferGrip was also placed in the solution. After 1.5 hours, both samples were unaffected. After 3 hours, the bonded sample appeared unaffected, but the unbonded sample had torn into smaller pieces. After approximately 15 hours, the bonded sample had become unbonded and the unbonded sample remained in smaller pieces. It was hypothesized that the unbonded sample had softened from the temperature, and been torn apart by the magnetic stirrer, rather than etched by the TMAH. The bonded sample becoming unbonded was assumed to be also due to debonding, which was worsened by the fact that the bonded sample was resting on the bottom of the jar near the hotplate,

where the temperature was nearer 115°C, combined with the thinning die at some point being agitated by the stirrer. It was later found that the bonding procedure was likely performed improperly.

For these reasons, it was determined that WaferGrip bonding may still be a feasible option for etch protection. A new etching setup was used, which is likely to have a more uniform temperature, and concentration should stay more constant. The pot on the photolithography development bench used is shown in Figure 81.

Figure 81: Pot used for TMAH bulk etching.

No magnetic stirrer or other agitation was used, and the temperature was set to 75°C to avoid softening. A new wafer was bonded to another wafer with thick oxide, this time using a slightly higher bond temperature of 140°C, and slightly longer time of approximately 20-30 seconds. The wafer was placed in a Teflon cassette, but offset slightly as shown in Figure 82.

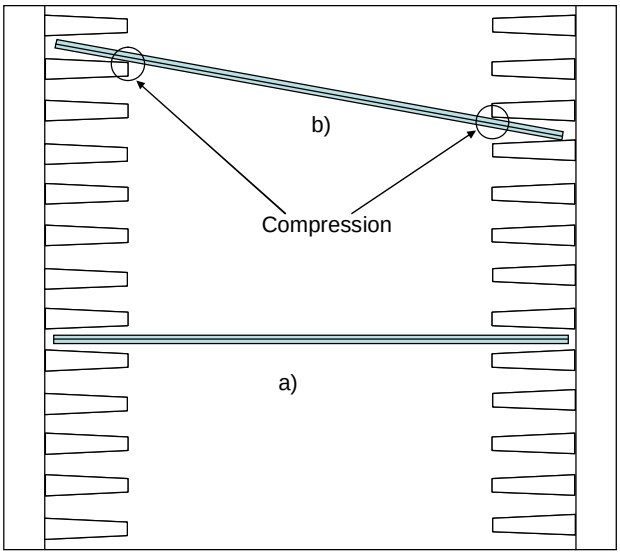


Figure 82: Top view of two bonded wafer pairs in a Teflon cassette. Bonded wafer pair a) is positioned conventionally, while wafer pair b) is placed at an angle to press the bonded wafers together.

This offset was done to create a slight force against debonding that may be caused by slight agitation from the fluid flow induced by temperature and concentration gradients.

The wafer was inspected for debonding or reaction of the TMAH with the WaferGrip at three-hour intervals. It was determined that the TMAH does attack the WaferGrip, but at a rate near that of the silicon etch. Because only the edges of the WaferGrip pad were exposed, the wafer was protected in all but those areas for the majority of the etch time. Due to the reduction in temperature for the process, the etch rate was slightly lower, at approximately 13.25µm/hr. Near the end of the etch process, at around 30 hours of etch time, the wafers began to debond more significantly, allowing TMAH to slightly etch the frontside of the wafer.

When the etch had proceeded through the necessary 385µm, the wafer was removed and rinsed. The debonding process was done by immersing the wafer in SVC-175

positive photoresist stripper at 100°C. Upon completion of debonding, it was found that the frontside of the wafer appeared rough and unclean. After allowing further WaferGrip stripping in the SVC-175 over night, and an overnight acetone bath, it was determined that rough surface was due to TMAH etching of the oxide in areas which were unprotected by WaferGrip. The unprotected area was much larger than expected, but pinholes appeared to be reduced despite this. To return to a smooth surface and reveal the underlying silicon, an oxide etch was performed. The etch also allowed for simpler assessment of the extent of pinhole formation.

Upon inspection, it was determined that pinhole formation had not been entirely eliminated, but significantly reduced such that an acceptable number of working devices would result. Images of pinholes and the front at which pinholes are largely eliminated can be seen in Figure 83.

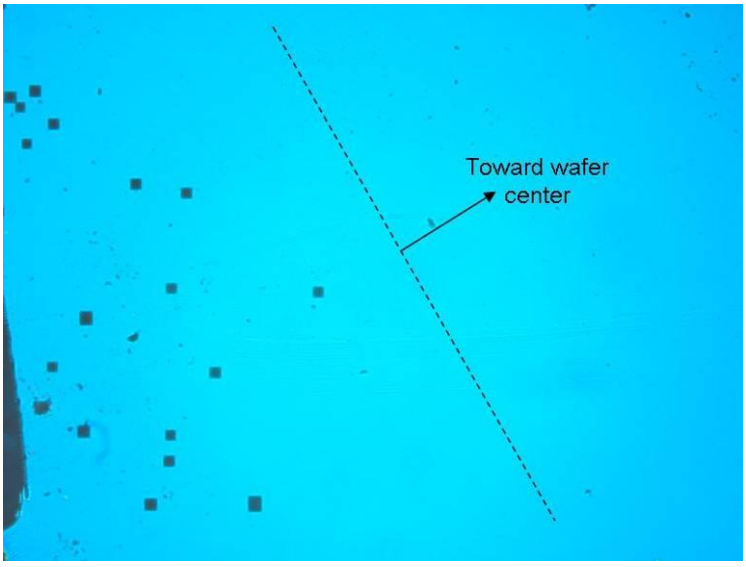


Figure 83: Pinhole number significantly reduced a certain distance from the wafer edge.

Following the etch process, that a borosilicate glass (BSG) layer that commonly forms over the doped device regions during the boron diffusion was noticed [26]. This BSG produces color variations in the doped regions due to interference as light reflects off of the silicon and BSG surface, making it clearly detectable. BSG is not crystalline and not piezoresistive, so it was undesired and was removed. BSG is etched in BOE, but etches at a slower rate than silicon dioxide. The wafer was allowed to etch further until this BSG layer had been entirely removed. Upon completion, it was noticed that the doped device areas were detectable only by a slight physical edge, and no color variation was present.

The wafer was then re-oxidized using a wet oxidation to create the protective layer for the devices into which vias could be etched. It was a concern that the etched features would create significant stress concentrations under the high temperature oxidation process. This stress, combined with the compressive stress induced by oxide formation, may buckle the diaphragms or possibly crack the wafer. Extra care was taken not to exceed the six inch per minute rate for loading and unloading of the wafer into the oxidation chamber. It was found that the oxidation did not lead to wafer failure, and an oxide thickness of approximately 0.6μm was achieved.

The remaining four wafers were then processed in pairs by bonding the frontside of two wafers together, exposing backside on either side of the bonded pair. It was determined that this served to further protect the wafer, as the oxide on the wafer frontsides inhibited TMAH intrusion into the region between the wafer and the wafergrip. When silicon was at the interface between wafergrip and wafer, the TMAH would etch

the silicon and easily pass into the interface, debonding the wafer more rapidly. With the oxide layer protecting the wafer edges, pinhole formation was eliminated entirely in all but the wafer edges. The wafers were also allowed to etch for the complete process, without interruption for more than 5-10 minutes. This was done because it was impossible to fully wash out the TMAH from between the wafers. Any time when the wafers were not being bulk etched in the TMAH bath, this very small amount of leftover TMAH would slightly attack the WaferGrip, but bulk etching was not occurring. Avoiding the time when this could occur meant the ratio of WaferGrip attacking time to bulk etch time was kept low.

The etch times for all four remaining wafers were approximately 31-33 hours, which was slightly longer due to the reduced TMAH concentration, as the same solution was used for all wafers. All wafers were etched approximately 380-387μm.

None of the four remaining wafers exhibited more than a few millimeters of debonding at the edges. While this served to eliminate pinholes, it made debonding difficult. When the wafers were placed in a 100°C SVC-175 solution, the wafers remained bonded after 48 hours. The SVC-175 was unable to penetrate into the wafergrip due to the relatively low temperature of the solution compared with the melting point of the wafergrip at 115°C, leaving the solution only able to attack at the edges of the wafer. To remedy this, the wafers were heated on a hotplate to 130-140°C, and very slowly slid apart with a pair of wafer tweezers. While this was effective in separating the wafers, the force needed to prevent slipping of the tweezers during sliding was enough to create a

small crack in two of the wafers. One crack destroyed a diaphragm, while the other appeared to not affect the sensors.

The remaining wafers were then oxide etched and oxidized just as the initial test wafer had been. During oxidation, the wafer which had been cracked also had a large (~2cmx1cm) chip snap off due to thermal stresses. It was found that neither the crack nor the chip appeared to affect any sensors.

Aluminum Lines and Vias

Via Lithography (Step 12)

Before the vias could be patterned on the oxide layer, it was necessary to first bond a handle wafer to the backside of the wafer (step 11). This was necessary due to both the fragility of the wafer, and because spin-coating would be impossible, as a vacuum seal is used to secure the spinning wafer. The wafer bonding technique was exactly that described for frontside bonding to mask the TMAH etch (the additional process added for step 10). A new complication arose due to the air trapped inside the diaphragms, and the temperature difference between bonding and room temperature. As the wafers cooled after bonding, the trapped air in the diaphragms dropped in pressure, causing the diaphragms to bend inward, as they would during testing. This effect can be seen in Figure 84.

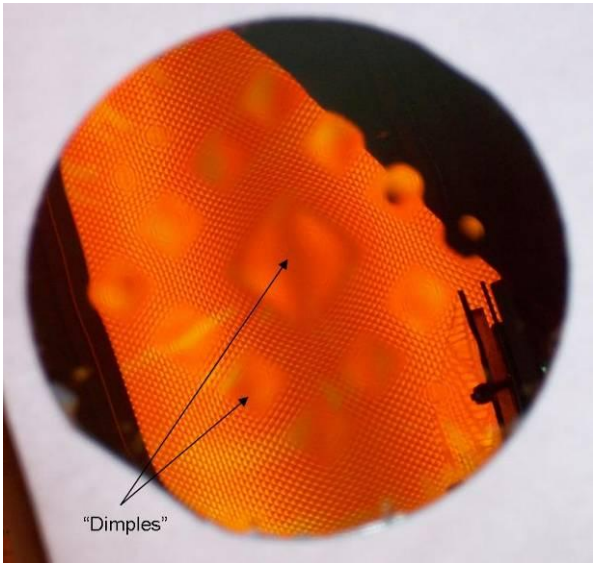


Figure 84: Inward "dimples" formed by the pressure difference between the air between the handle wafer and the diaphragms, and the atmosphere.

It was determined that there was no simple method for eliminating the 'dimpling' in the wafer, and that it should be unlikely to significantly affect processing, which was later found to be a false assumption. Once the wafers had been bonded, they were put in the vapor prime oven to prepare them for the via photolithography. The vapor prime oven subjects the wafers to cyclic vacuum, and a temperature of 125°C. The vacuum environment applied to the wafers caused them to bend outward, and the elevated temperature of 125°C, only slightly less than the bonding temperature of 140°C, reduced the counteracting inward bending. This caused the diaphragms to bend outward and inward repeatedly. The wafer that had been previously chipped due to the mechanical separation of the bonded wafers shattered due to the bending. The shattered wafer can be seen in Figure 85.

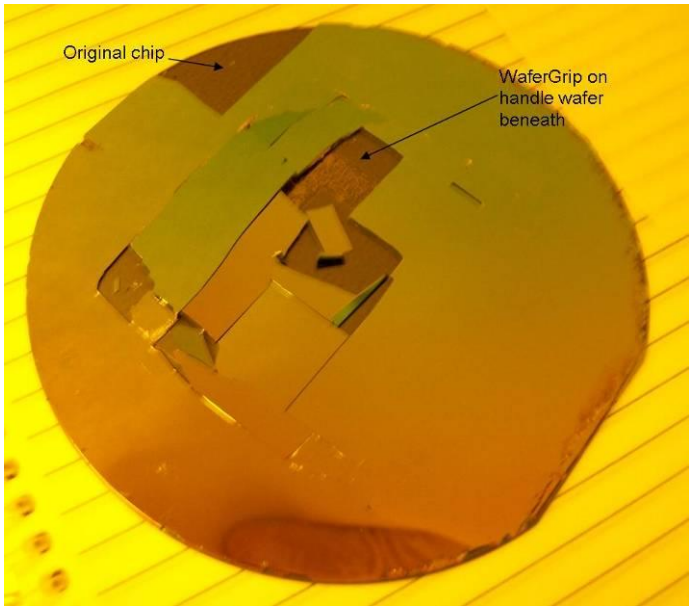


Figure 85: Wafer which burst due to cracks formed during mechanical wafer separation causing the wafer to shatter when under vacuum in the vapor prime oven.

The remaining wafers were unaffected, and it was supposed that the shattered wafer was simply weaker due to the crack from mechanical separation. The scrapping of this wafer left five remaining wafers. The wafers were then spin-coated with photoresist, as in previous lithography steps, and it was found that the dimpling caused an uneven distribution of photoresist on the wafer surface.

Using the Nanospec, it was determined that the photoresist thickness differed by only approximately 0.2µm, with a thickness of approximately 1.4µm, which was found to still allow for proper patterning.

It was also found that the first wafer to undergo TMAH etching could not be properly spin-coated due to the density of the pinholes on the surface. This wafer was scrapped, leaving four remaining wafers

Exposure of the first wafer was done for 3.5 seconds, and the development time was 45 seconds. It was found that this combination of development and exposure times was insufficient for via creation, as many vias were not present in the resulting pattern, and the vias that were created were small and did not appear to fully penetrate to the silicon surface. Images of the smaller vias can be seen in Figure 86.

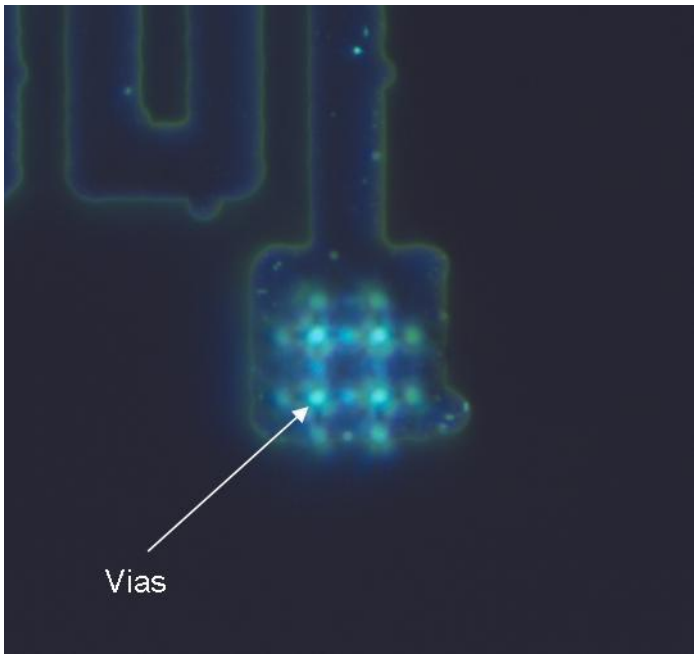


Figure 86: Small vias under dark field illumination.

The exposure time was therefore increased to 5 seconds, with a development of 50-60 seconds. While the increase in time did allow for all vias to be created, they were significantly larger, and in places may contact silicon regions outside of the boron-doped regions. Also, it appeared that the vias still had not penetrated to the boron-doped regions. Finally, the array pattern in the resulting resist layer did not match that of the exposure mask. The difference can be seen in Figure 87.

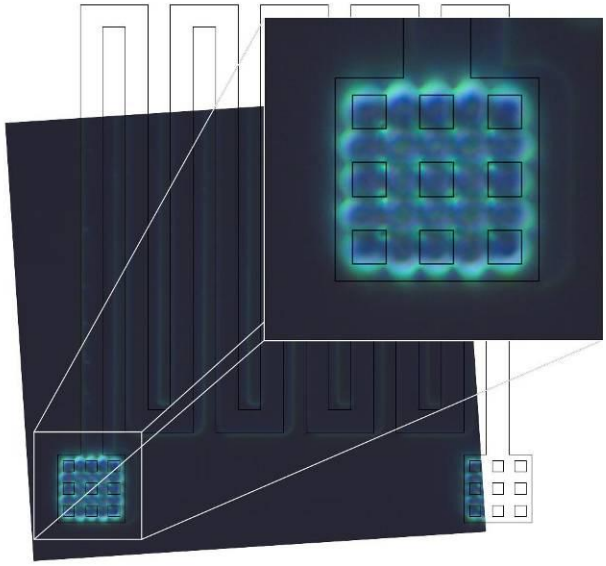


Figure 87: Oddity in the vias. The resistor and via design has been overlain on a dark field image of the vias in the photoresist. The design was then shifted to match the via misalignment.

In another wafer, which had much less dimpling in the 1cm diaphragms, it was found that the via patterns did, in fact, match those of the exposure mask as seen in Figure 88.

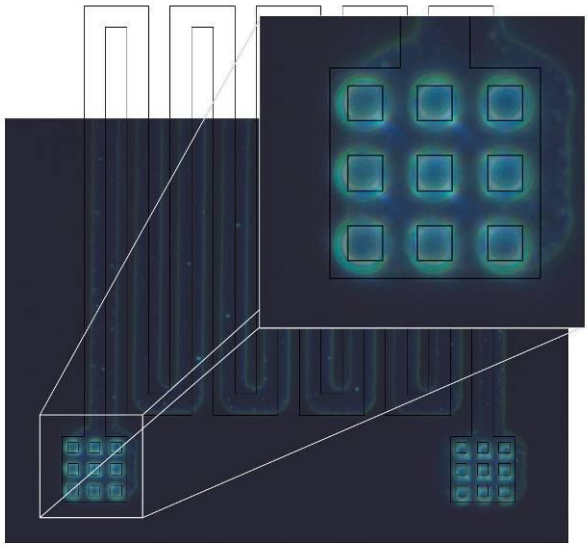


Figure 88: Wafer with proper vias. The wafer had much less dimpling than the others. The resistor and via design has been overlain on a dark field image of the vias in the photoresist. The design was then shifted to match the via misalignment.

It is hypothesized that this mismatch is due to lack of contact between the exposed region and the exposure mask due to the dimpling. The result is slight diffraction off the edges of the exposure mask, spreading the light and possibly resulting in a diffraction pattern. This effect is illustrated in Figure 89.

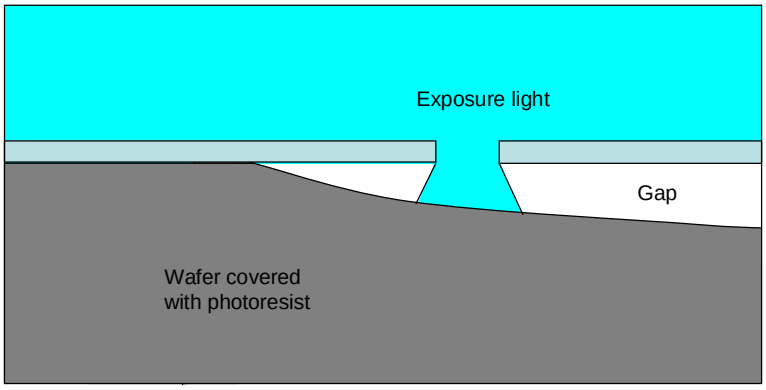


Figure 89: Possible explanation of via oddity. Due to lack of contact during exposure of the via regions, light may be diffracting off the edges of the mask.

Because none of the wafers had a photoresist mask which had vias that penetrated to the silicon surface, it was necessary to plasma ash the resist. Plasma ashing is an anisotropic etch, unlike wet etching. The sidewall etch rate is insignificant compared to the rate of etch of the photoresist surface. This aspect of plasma ashing allowed for the removal of the remaining photoresist in the vias, just as it allowed for the removal of the thin photoresist layer remaining in the device areas. The plasma ash was done for approximately 2 minutes, at about 100W using oxygen gas. Some images before and after plasma ashing can be seen in Figure 90.

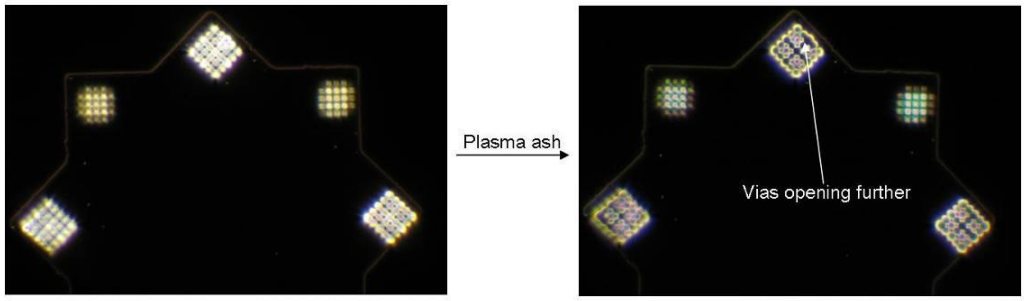


Figure 90: Dark field images of an eight terminal VDP device on test wafer before and after approximately 3-4 minutes of plasma ashing.

Following the plasma ashing, the oxide layer was etched with 6:1 BOE. Images of the resulting vias can be seen in Figure 91. The larger, box shaped vias are more typical in all but the test wafer due to the increased development time.

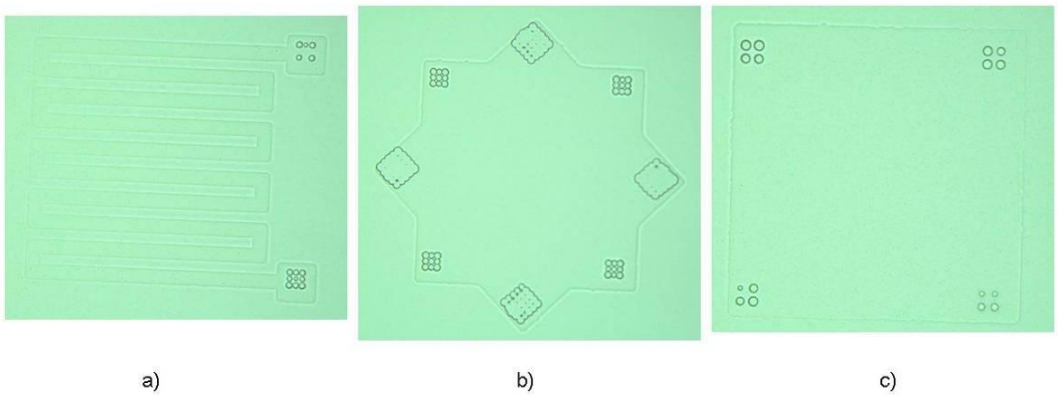


Figure 91: a) A serpentine resistor b) an eight terminal VDP, and c) a VDP device showing the variations in via results. Note that these images were taken after an aluminum layer was deposited.

It should be noted that the plasma ashing process through to the removal of the handle wafer was completed on one test wafer to ensure that the processes could be performed without any issues. Using this wafer it was determined that debonding of the wafer was near impossible using previous methods, as will be discussed later in this thesis. The test

wafer eventually was scrapped due to problems resulting from debonding. All subsequent discussion pertains to the three remaining wafers.

Al PVD (Step 12)

After the vias had been created, the next step was to fill them with aluminum, and to create the aluminum layer in which the lines and pads would be created. This was done with aluminum evaporation, which was done exactly like that of the deposition of the aluminum layer for the alignment markers, with two exceptions. First, $40cm^2$ of aluminum was used to produce a film thickness of approximately 0.6-0.7μm rather than $30cm^2$ as was previously used. Secondly, during the deposition, the heating element was given too much power, which degraded the vacuum. It was degraded far enough to where the instrument stopped supplying power to the filament, preventing evaporation during times when the mean free path was insufficient. Once the vacuum was restored a few seconds later, the filament was supplied power in full. This rapid cooling and heating caused three diaphragms on one wafer to burst. This wafer had also previously been cracked by the mechanical debonding of the wafers in the TMAH step, and was also the wafer which had significantly less dimpling of the diaphragms which resulted in proper vias. The wafer was not entirely scrapped, as many of the diaphragms on the device were unaffected by the bursting diaphragms. At this point, two entire wafers remained, along with another ‘half’ wafer.

Lines and Pads Lithography (Step 12)

The lines and pads are created by etching all the aluminum where a line or pad is not intended. Because photolithography creates a mask which protects areas from etching, and because the majority of the aluminum film must be etched, the mask used in this photolithography process was a light field mask. Light field indicates that chrome does covers only the areas specified, while light field indicates that chrome does not cover the areas specified.

A light field mask does not add any complexity to the lithography process, but rather made alignment much easier with the wafer surface easily visible.

The exposure time used was 3.5 seconds, with a development time of approximately 45-50 seconds to fully remove the large amount of exposed photoresist from the wafer. The resulting feature size was not as critical as the via lithography, at 10µm lines rather than 3µm arrays, and was easy to achieve. Images of the resulting devices can be seen in Figure 92.

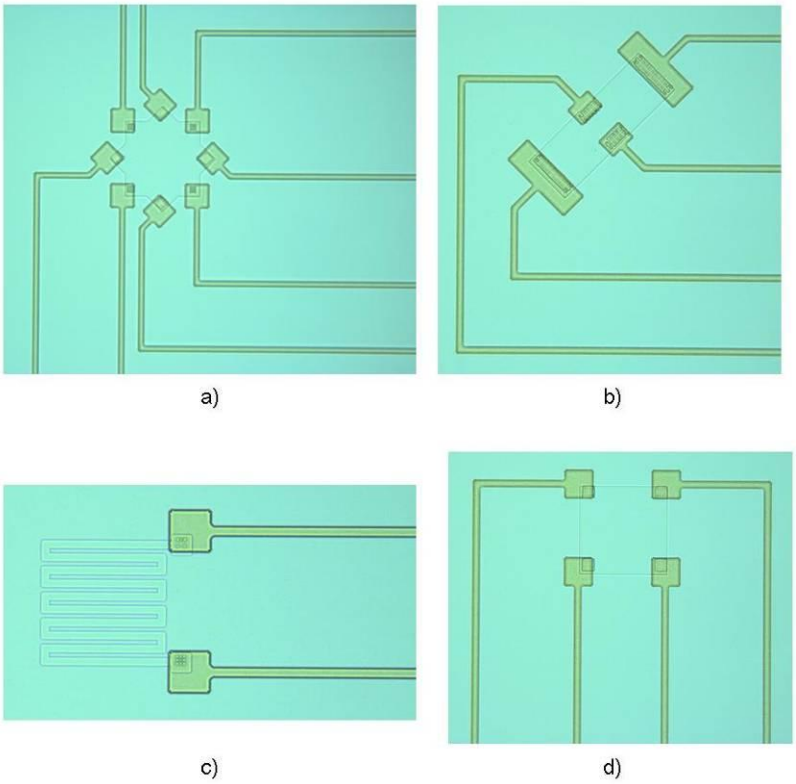


Figure 92: Images of the devices with the photoresist to mask the aluminum etch to create the lines and pads.

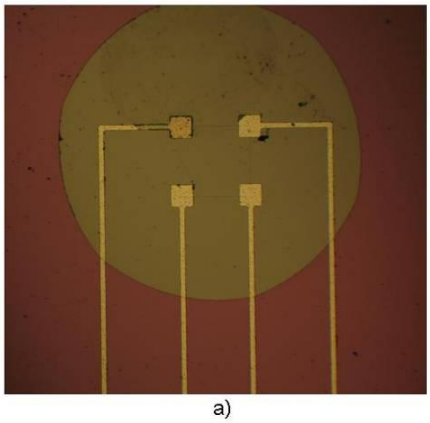
Process Finalization (Step 13)

Following the lithography step, the wafers were etched in PAE etchant as was done in creating the alignment markers for backside etching. The etch time varied from approximately 5-8minutes to fully etch the exposed aluminum.

The last remaining process is annealing, but due to the high temperatures involved in annealing, the wafers must first be debonded, as the WaferGrip would be unable to withstand such temperatures.

Debonding proved to be much more difficult with the handle wafer bonded to the backside rather than the frontside. Using the test wafer, a hotplate was used to bring the

wafer temperature up to 140°C, the handle wafer and the sensor wafer were slid apart using two wafer tweezers. It was found that after they had been slid a small amount, that it became very difficult to continue separating them. It was hypothesized that this issue is also a result of the dimpling, which has created a pressure difference that acts to keep the wafers bonded, and as the wafers are pulled, the movement and pressure difference act to bring the wafers into direct contact, greatly increasing the friction between the two. After severely cracking both the test sensor wafer and handle wafer attempting to separate the two, it was determined that a new debonding method was needed. In addition to cracking the wafer, the lines had been scratched severely, making them useless. Images of the damaged wafer can be seen in Figure 93.



a)

b)

c)

Figure 93: Damaged wafer a) VDP device where the photoresist for via placement had very poor adhesion, causing expansion of the vias. Inner circle is bare silicon. b) Lines damaged due to scratching, resistance is either very high or circuit is open. c) Lines completely broken apart

Previously, it was determined that SVC-175 alone, without agitation, would not be adequate for debonding two wafers, even without the issue of dimpling. The ineffectiveness of the SVC-175 is largely due to its low flash point of 104°C constraining the temperature of the solution to well below that of the melting point of the WaferGrip material, at 115°C. Also, the inability to provide effective agitation in a single wafer setup inhibited debonding. To remedy the issue of temperature, StripAid [29] was purchased from Dynatex, Inc., which has a much higher flash point of 212°C. The complete MSDS for StripAid is in the appendix of this thesis. The StripAid was tested on the test wafer at 140°C solution temperature, and it seemed to be more effective, separating the remaining sensor wafer from the handle wafer pieces after approximately three hours. Once the remaining wafers had been brought to the debonding step, a large amount of StripAid was placed into a large beaker and set atop a hotplate. The hotplate was raised to 160°C initially, and later brought to 185°C after it was determined that this was acceptable, and recommended by the Dynatex support staff. A magnetic stirrer was placed in the beaker which rotated at 1000rpm to agitate the mixture. The three wafers to be debonded were placed in a small Teflon cassette and placed in the beaker. The wafers were checked after in approximately 8 hour increments. After about three days, the wafers could be wedged apart by the wafer tweezers. Large amounts of WaferGrip remained in the diaphragms and on the handle wafers where the diaphragms had been, indicating that the pressure difference was, in fact, preventing the solution from attacking

the WaferGrip in those areas. Once exposed, the remaining WaferGrip was dissolved rapidly, in less than an hour.

The wafers were then cleaned in acetone and isopropanol to remove the StripAid, as it is relatively insoluble in water. After drying, the wafers were annealed. To anneal, the wafers were placed in the boron diffusion furnace away from the boron sources to prevent diffusion. The furnace was brought to 450°C while the wafers annealed for 45 minutes. The purpose of the anneal is to improve contact between the aluminum in the vias and the boron-doped silicon surface. It was a concern that the wafers would crack during the process, so this step was done twice with two sets of wafers, one containing the ‘half’ wafer and a completed wafer, the other containing a completed wafer and the test wafer. Images of the completed wafer devices can be seen in Figure 94.

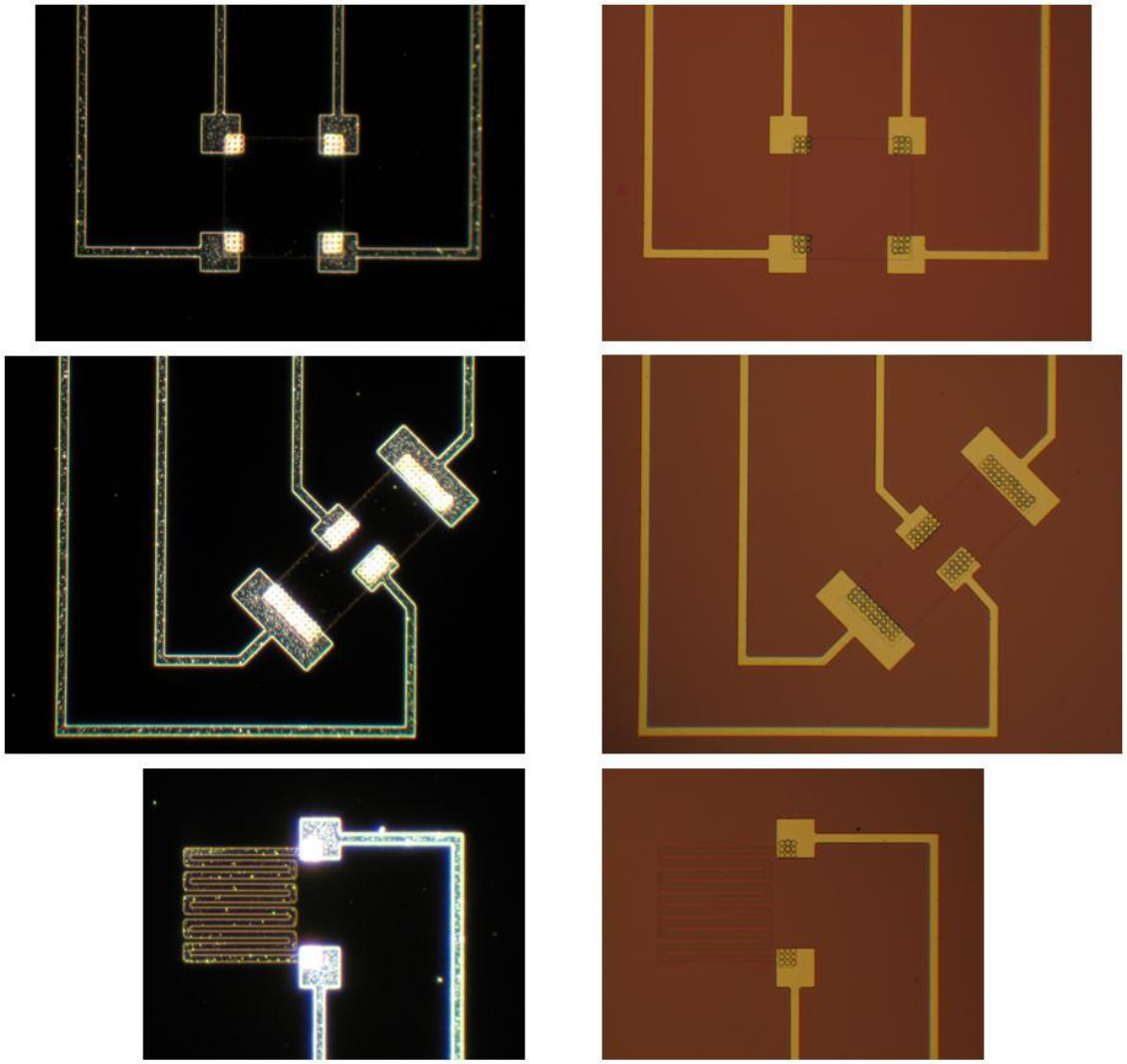


Figure 94: Completed devices under a) dark field and b) light field illumination.

DEVICE TESTING

Pressure Chamber Test Apparatus

Device Testing was done wafer-level, though the wafers had been designed to be diced if required for future testing. The wafer was taken out of the cleanroom to a lab where a pressure test apparatus had been constructed. The pressure test apparatus, or pressure chamber, is designed to apply a controlled pressure to the backside of the wafer in a specific location such that the diaphragm can be stressed.

The pressure chamber apparatus works primarily using an aluminum pressure chamber of 5in diameter and 3.25in height which is pumped down using a small, oil-free, GAST mechanical vacuum pump. The pressure chamber and pump can be seen in Figure 95.

a) b)

Figure 95: a) Test Setup b) Vacuum Pump.

The pressure is controlled via an SMC regulator with a maximum flow rate of approximately 2 liters per second, containing a pressure sensor. The regulator is controlled by inputting 0-10V to the regulator, the scale corresponding to the desired regulator pressure between vacuum and atmosphere. It was quickly determined that the regulator is poor at fine regulation, and a control system was created which allows for pressure regulation to remain within approximately 0.5 kPa of the desired pressure.

An in-situ pressure transducer was used to determine chamber pressure, because the regulator may experience a pressure different than that of the chamber due to line effects. Calibration of the pressure transducer was done using a factory calibrated vacuum gage, and should be accurate to within ±3kPa. The chamber system is controlled electronically using a National Instruments SC-2345 Data Acquisition System and LabVIEW software. The LabVIEW software controls the chamber pressure by comparing a desired pressure to the transducer pressure and properly supplying voltage to the regulator, which slowly bleeds air into the chamber as the vacuum pump removes it, creating a near static pressure.

The pressure chamber lid has a small opening of approximately 1/16in (~1.6mm) diameter which transmit the chamber pressure. An opening in the chamber lid can be seen in Figure 96.

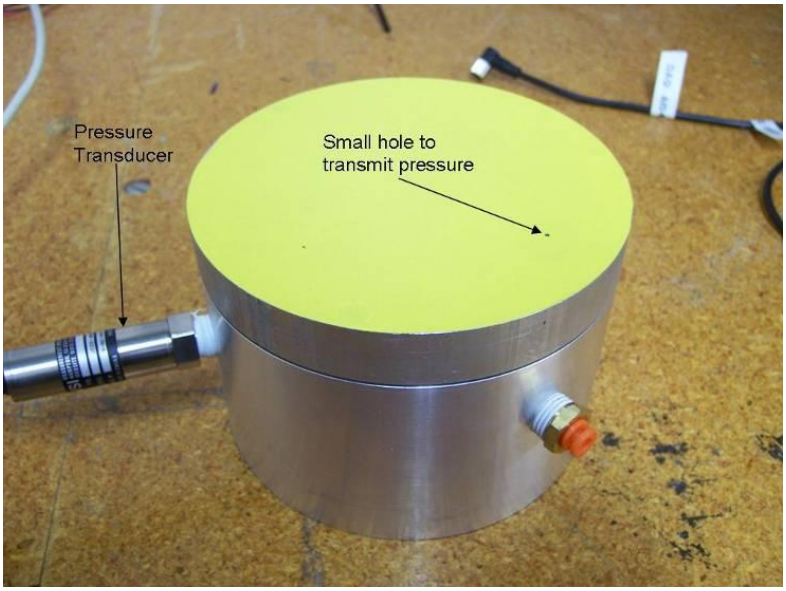


Figure 96: Pressure chamber with contact paper covering and small hole for pressure transmission

The pressure diaphragm is centered above the opening, and a seal is maintained to transmit the chamber pressure into the diaphragm. This creates a pressure difference between the surface of the diaphragm, which is at atmosphere, and the backside of the diaphragm, which is at the chamber pressure.

Maintaining a seal has proved difficult. Initially, electrical tape was used to achieve a seal, which was only successful under low pressure differences of under 10-15kPa. A wax paper surface has been used with much more success, with pressure draining at a rate of approximately 0.25kPa/s with the vacuum pump off.

To obtain voltage and resistance measurements and provide current to the VDP sensors, the pressure chamber is placed under a stage. The stage can move relative to the surface on which the chamber is placed, however it has been found that moving the chamber itself is more convenient, due to the need to have it be mobile for initial wafer

placement. The stage has a large opening, approximately 5.75in. in diameter, which allows for access to the wafer from above. Light field illumination shines down through the opening onto the chamber surface, and a Nikon SMZ8000 microscope is positioned above the opening for observation and positioning. Four micromanipulators, shown in Figure 97, are positioned on the stage.

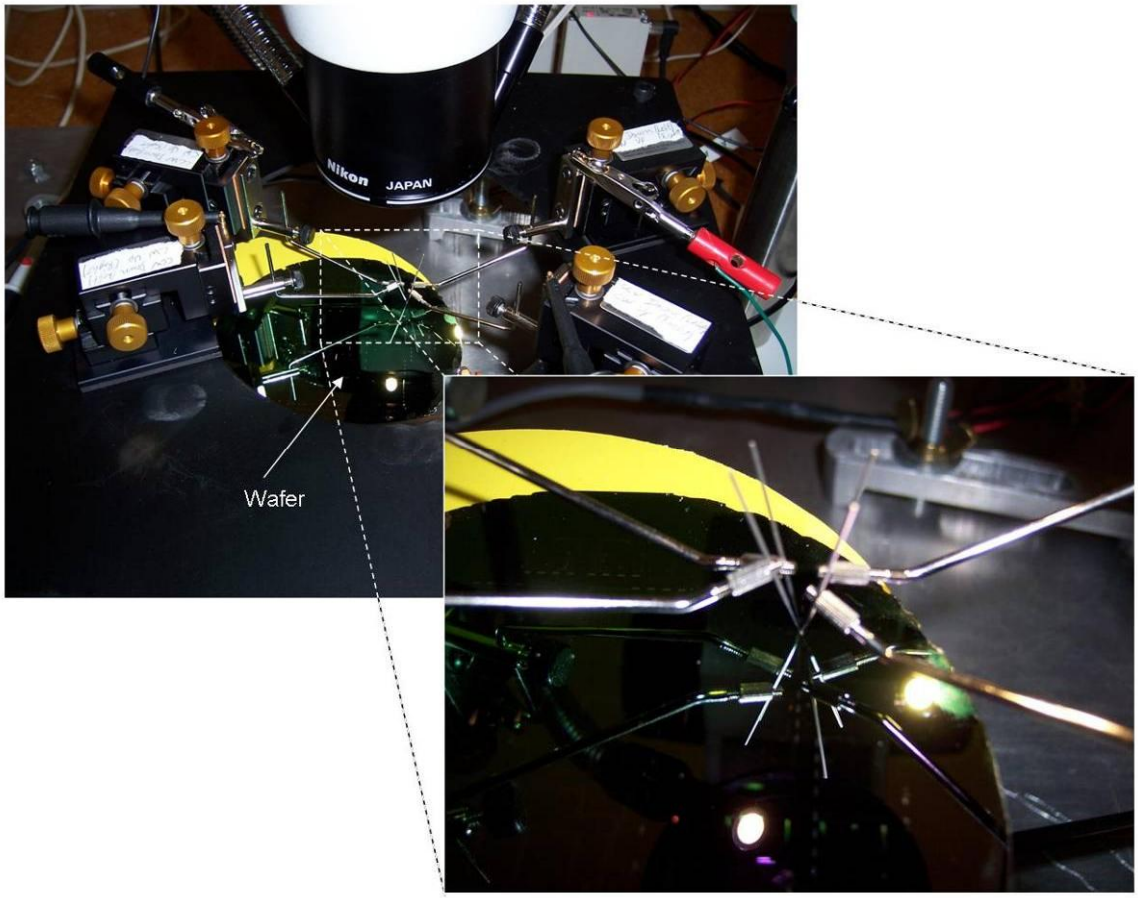


Figure 97: Micropositioners located on the stage making contact with the pads on the wafer

The four micromanipulators are used to make contact with the small pads on the wafer, and are then connected to an Agilent 34410A digital multimeter, or an Agilent

E3631A DC power supply as a voltage source for the VDPs. Micromanipulators making contact with the aluminum pads can be seen in Figure 98.

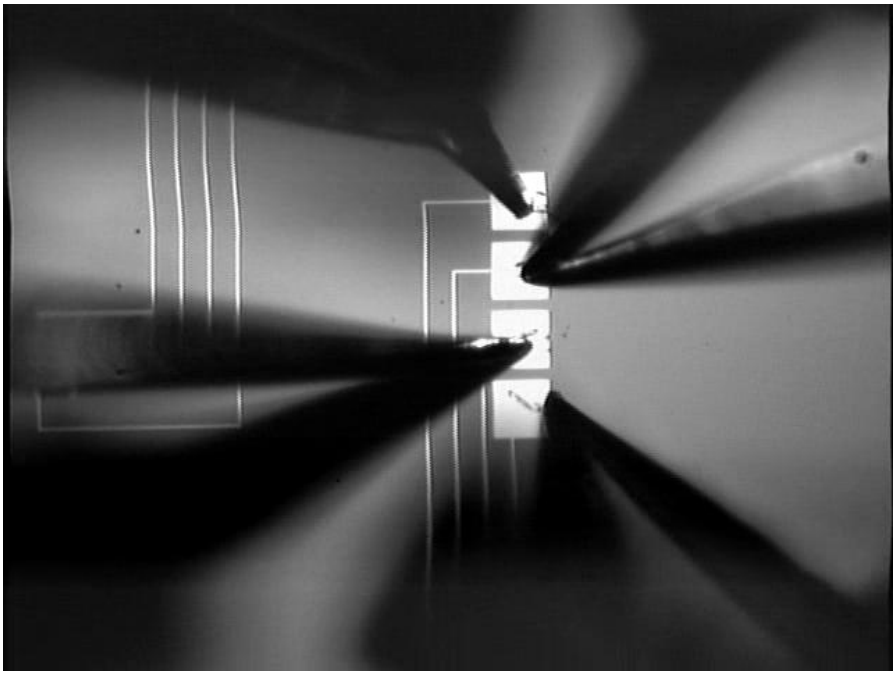


Figure 98: Micropositioners making contact with the VDP pads.

The microscope is connected to a television which allows for convenient viewing. The signal is also sent to a PC card which allows for collection of video and still images.

Device Testing Methodology

It was desired to test the VDP device against a number of parameters, with the sensitivity of the device under certain circumstances being the primary quantity measured. As was shown in the Introduction section of this thesis, the normalized resistance change difference (NRCD) of piezoresistive devices is linearly proportional to the stress at the position of the device. In reality, it is the average of the stress over the

area of the device which the resistance depends on, but with small devices on relatively large diaphragms, the device area is small and can be approximated as point-like. Therefore, physical distance measurements will not be performed, and the devices will be assumed to be point-like to associate stress and pressure.

Measurements that will be performed are ones which will allow for the determination of the NRCD. For VDP devices, the measurements required are a current through two terminals, and a voltage across the other two. The voltage and current will then be measured across the other terminal pairs to obtain a 0° and 90° set of voltages and currents. Using these data it is possible to obtain the values of $R_{AB,CD}$ and $R_{AD,BC}$ which are essentially R_{φ}^{σ} and $R_{\varphi+90}^{\sigma}$. These values can then be compared with the same data obtained at atmospheric pressure to determine the unstressed resistance and obtain a normalized resistance change (NRC) given by

$$\frac{\Delta R_{\phi}}{R_{\phi}} = \frac{R_{\phi}^{\sigma} - R^{0}}{R^{0}} = \frac{R_{\phi}^{\sigma}}{R^{0}} - 1 \qquad \text{(31 repeated)}$$

Subtracting the 90° NRC from the 0°, the NRCD is obtained for the VDP. The slope of the NRCD for a device is its sensitivity. This is the same procedure used to determine the NRCD for all VDP devices, including the ‘frame’-style devices.

To determine the NRCD for the serpentine resistors, a pair of resistors is needed, where only one VDP was needed. The resistance of a 0° resistor is first determined both under a pressure difference and at atmosphere, and then the same is done for a 90° resistor at the same pressure difference and at atmosphere. The convention used for VDP and Resistor devices for the 0° and 90° degree configurations are as shown in Figure 99.

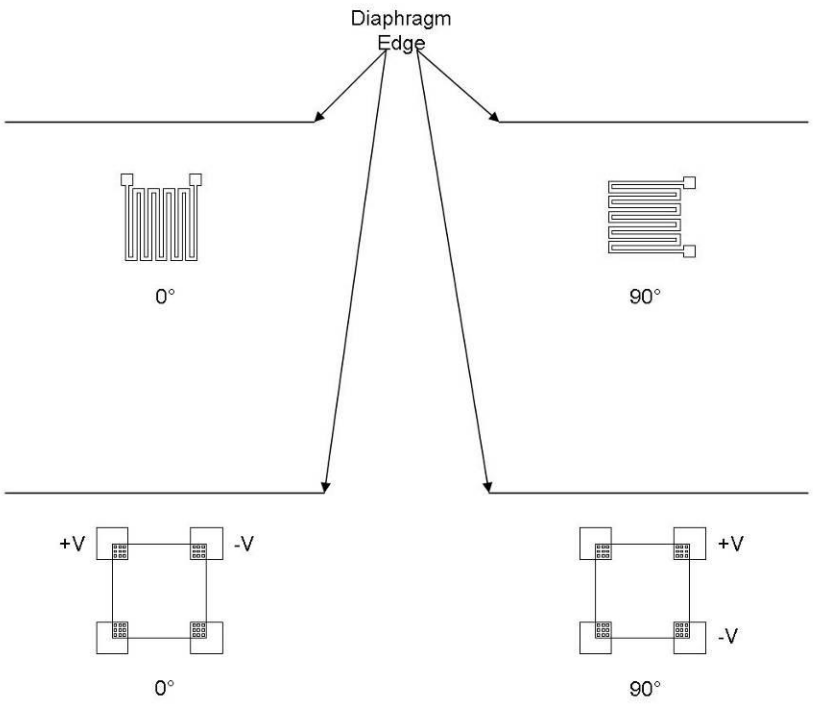


Figure 99: 0 and 90 degree orientations for the devices is based on their orientation with respect to the nearest edge. For the VDP, the orientation is based upon the contacts from which voltage is measured.

It was later found that it was necessary to determine the resistance of the lines to the resistors. The reason for this is that the line resistance was significant, ranging from ~25-150Ω, when compared to the resistance of the sensors, ~225-600Ω. When calculating the normalized resistance change, the intention is to normalize with respect to the unstressed resistance of the piezoresistive area only. The effect of the line resistance in the original calculations was to decrease the apparent sensitivity of the device. Note that this is not necessary for the VDP devices. A known current is being passed through the VDP, which will be the same through the line and the device, so the line resistances have no effect. Also, because a voltmeter is used to read the voltage across the other terminals, and

because voltmeters ideally pass no current into the circuit, the line resistances can produce no voltage drop and once again do not effect the measurement.

Pressure differences of 25.6, 38.6 and 45.1 kPa were used in addition to atmospheric pressure, allowing for an NRCD linearity check in addition to determining NRCD only at approximately the maximum pressure difference possible using the test apparatus.

Data Analysis

VDP Linearity

The first task was to determine the linearity of the devices. Collecting the necessary voltages and current at varying pressures for both the 0° and 90° configurations from a single VDP on one of the full wafers, the plot of NRC was obtained as shown in Figure 100.

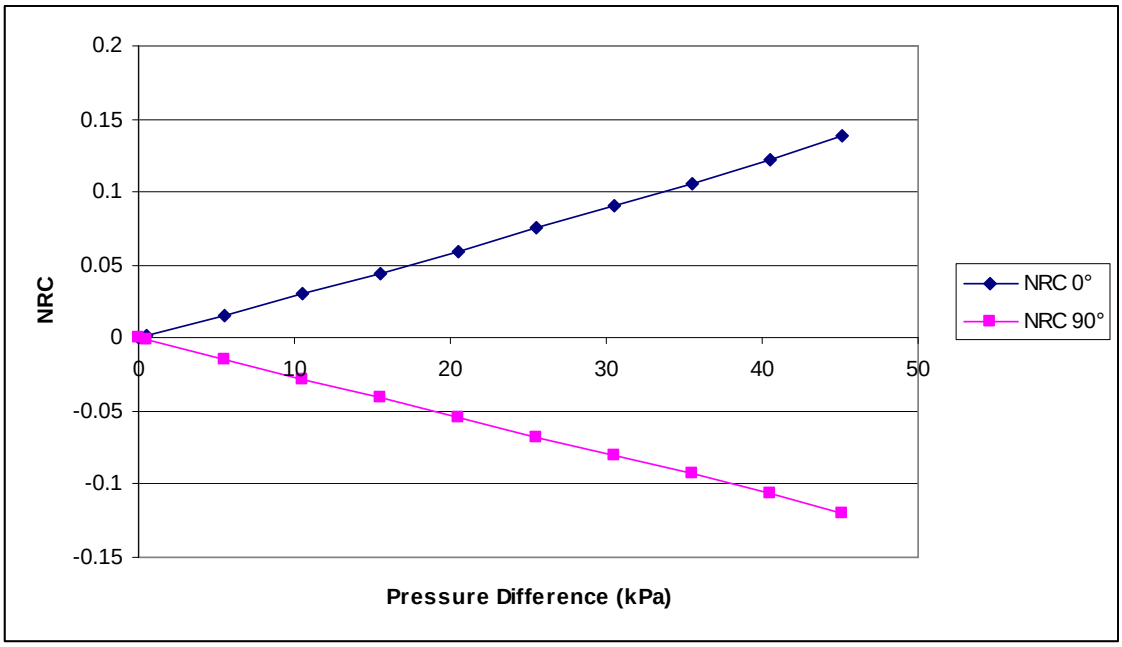


Figure 100: NRC of a single VDP device.

Taking the difference of these lines, the NRCD was obtained and plotted in Figure 101.

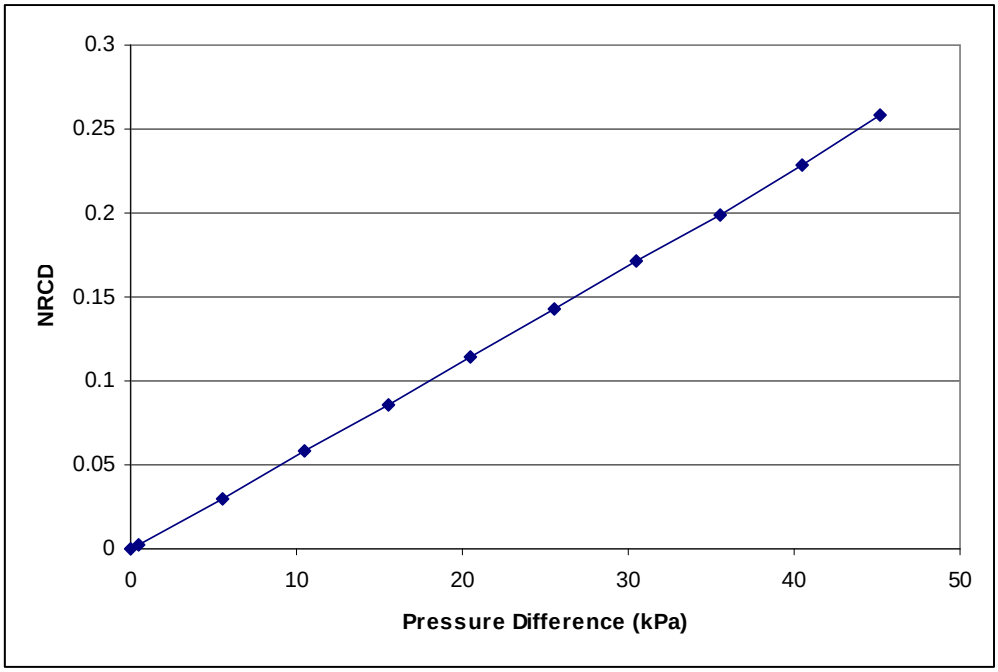


Figure 101: NRCD of a single VDP device.

It can be seen that the data can be reliably represented as linear. The sensitivity of this particular VDP with respect to pressure was found to be 5.72MPa^{-1}. Table 3 summarizes the sensitivities found from the devices on the three wafers.

Table 3: VDP Sensitivity for each wafer. Sensitivity is NRCD over Pressure Difference

Wafer	VDP Sensitivity (1/Mpa)
Half Wafer (3 VDPs)	5.61
Full Wafer 1 (4VDPs)	4.46
Full Wafer 2 (5VDPs)	5.63

A plot of the mean of all VDPs tested for each wafer vs. pressure with standard deviation error bars is shown in Figure 102.

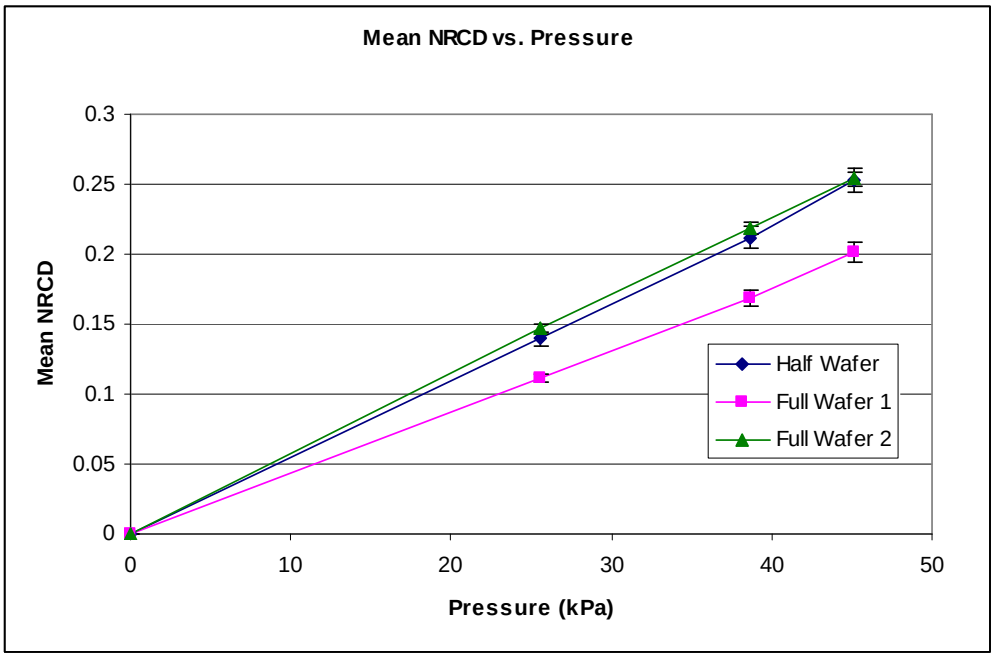


Figure 102: Wafer mean VDP NRCD vs. Pressure.

VDP vs. Resistor

The primary characterization of the VDP device is its sensitivity, specifically in comparison to the conventional serpentine resistor device. Previous work by Law [9] has shown through 2D and 3D finite element analysis that the VDP sensor is in fact much more sensitive than the conventional serpentine resistor. The results from the 2D analysis by Law are shown in Table 4.

Table 4. Summary of Law's 2D analysis results [9]

Sensor	Value	Sensitivity	Units
VDP	Theoretical Sensitivity	4.401	GPa^{-1}
	Uniaxial Stress Sensitivity – MATLAB	4.358	GPa^{-1}
	Uniaxial Stress Sensitivity – ANSYS 2D	4.351	GPa^{-1}
Serpentine	Theoretical Sensitivity	1.381	GPa^{-1}
	Uniaxial Stress Sensitivity – ANSYS 2D – 4 legs	0.825	GPa^{-1}
	Uniaxial Stress Sensitivity – ANSYS 2D – 6 legs	1.076	GPa^{-1}
	Uniaxial Stress Sensitivity – ANSYS 2D – 8 legs	1.185	GPa^{-1}

	Uniaxial Stress Sensitivity – ANSYS 2D – 16 legs	1.298	GPa^{-1}

The results shown by Law [9] show that the VDP device is between 3.15 and 5.33 times more sensitive than the conventional serpentine resistor device, depending on the analysis type used, and the number of legs in the serpentine resistor structure. The analysis of the serpentine resistors utilized a different serpentine resistor structure than the one designed for wafer testing. In addition to a differing structure, Law analyzed the effect of increasing the number of legs, or bends, in the serpentine resistor. The 8 leg structure is shown in Figure 103.

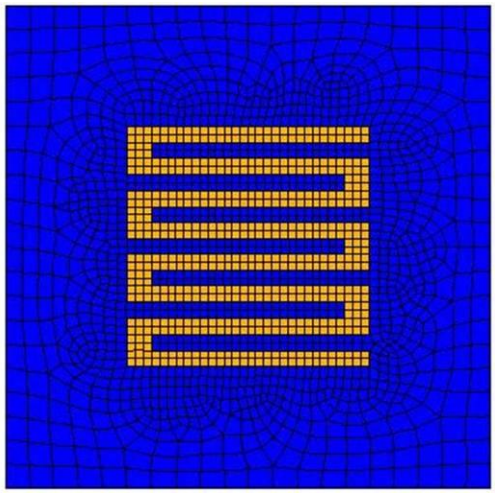


Figure 103: Eight leg serpentine resistor device and mesh used by Law in 2D uniaxial stress analysis. [9]

The plot of NRCD for the VDP device in 2D and 3D FEA which corresponds to Table 4 is shown in Figure 104.

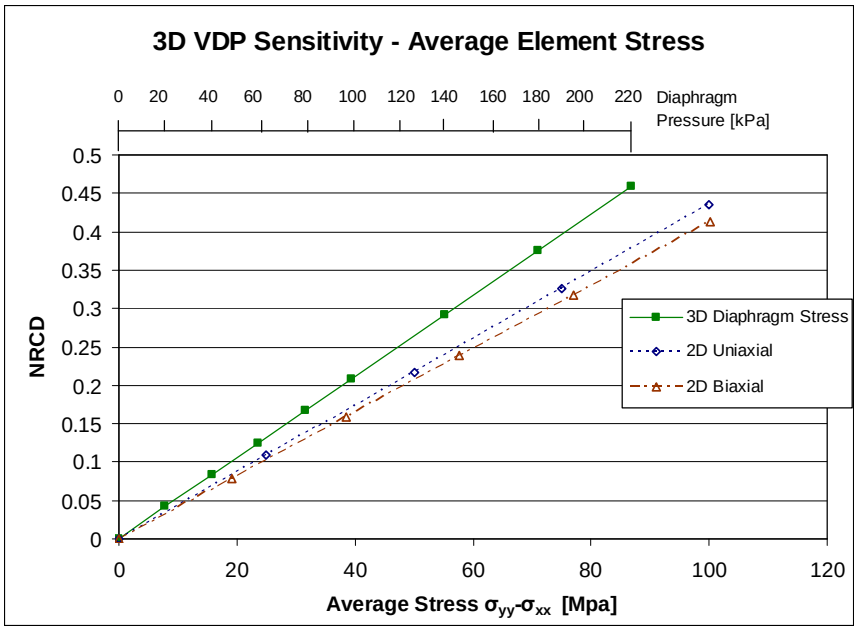


Figure 104: VDP NRCD in 3D diaphragm FEA. 2D Uniaxial and 2D Biaxial analysis results are included. [9]

Due to the lack of knowledge of the piezoresistive coefficients for the fabricated devices, and the differences between the FE model used by Law and the fabricated devices, quantitative comparisons are difficult to make. For this reason, Law's finite element analysis has been performed again with parameters that match the fabricated devices. Also, a pressure range which matches that of the data obtained was used in the FE analysis to make comparison more clear. The piezoresistive coefficients are still unknown for the fabricated wafer, however, so comparison must remain largely qualitative, however.

A set of VDP devices on each wafer were measured according to the methodology described previously. On the damaged half wafer, referred to as Half Wafer (HW), only three VDP devices remained functional, and all were measured. On the first full wafer, referred to as Full Wafer 1 (FW1), all VDP devices were functional, and all four on one

of the two VDP diaphragms were tested. On the final full wafer, referred to as Full Wafer 2 (FW2), only one VDP device was functional on the primary VDP diaphragm, which was measured in addition to all four functional VDP devices on the oppositve VDP diaphragm. The mean for each wafer, with standard deviation error bars, are plotted in Figure 105, along with the result obtained from FEA.

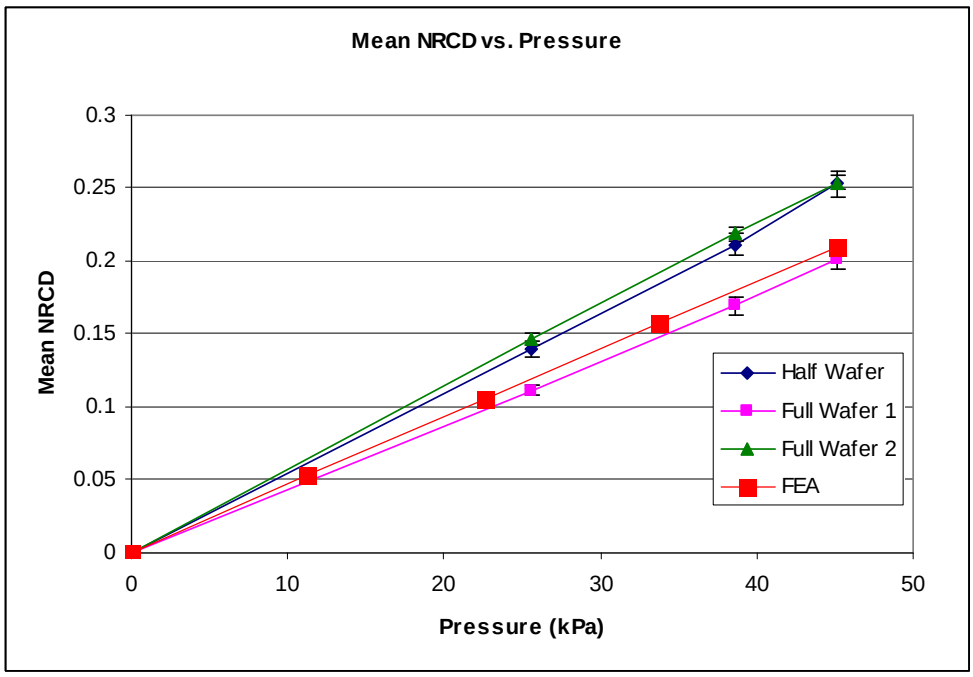


Figure 105: Wafer mean VDP NRCD vs. Pressure. FEA results are included.

The difference between HW/FW2 and FW1 is larger than expected, but is likely a result of differing bulk etch depth resulting in a differing diaphragm thickness. It also may be a result of differing piezoresistive constants due to possible doping inconsistency. Also, device misalignment with respect to the coordinate axes may be significant source of error.

The accuracy of the results with respect to FEA is more surprising, as the piezoresistive coefficients are unknown, and as such, quantitative conclusions should be avoided. The accuracy does indicate similar piezoresistive coefficients.

Examining the serpenting resistor data against the VDP device, the improvement is much larger than expected, as shown in Figure 106.

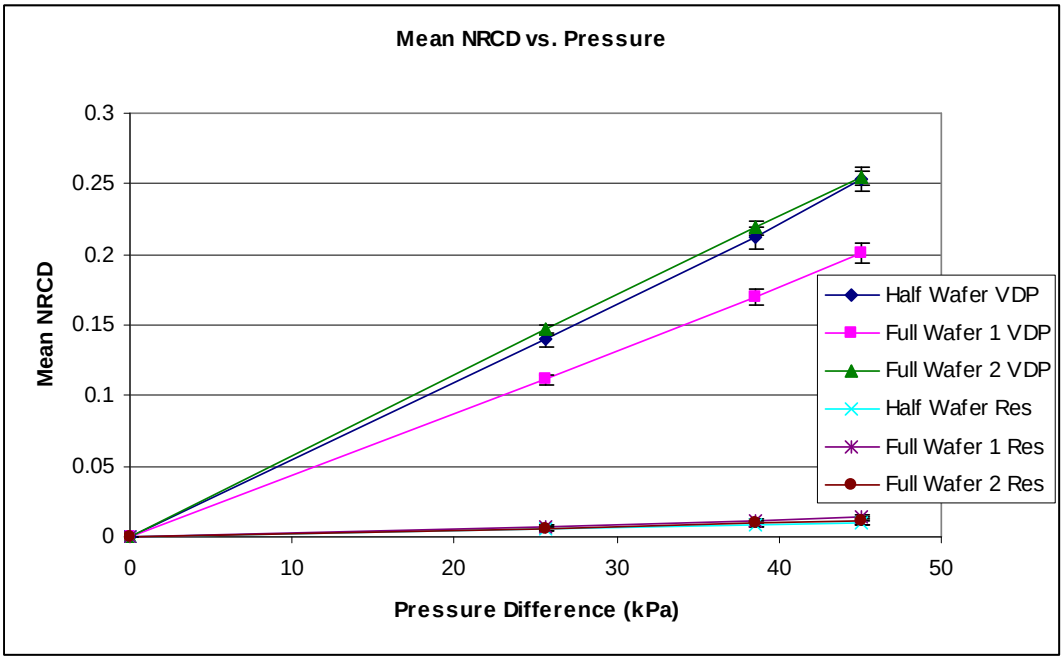


Figure 106: VDP NRCD and Resistor NRCD vs. Pressure

The sensitivity of the VDP device is much greater than 3.15 times the sensitivity of the resistor, as theory predicts. This can be explained primarily by the geometry of the device, and the stress state applied in the theoretical calculations. As shown in Figure 107, the 2D FE analysis of various shaped serpentine resistors is plotted against the mean resistor sensitivity.

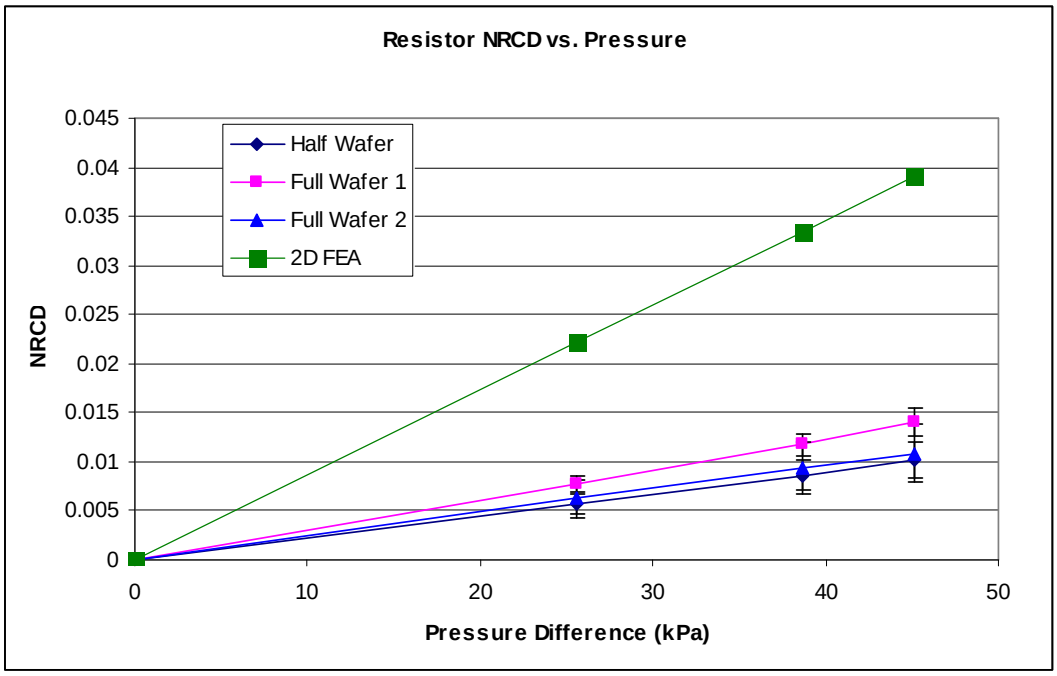


Figure 107: Fabricated resistor NRCD vs. pressure against 2D FEA resistor NRCD vs. pressure.

The 2D FE model done by Law was altered to more closely match the fabricated devices. The fabricated device is a 10 leg device, as is the 2D FE model. One major problem with the model is that a biaxial stress state must be applied to the FEA. Using plate theory calculations, the approximate biaxial stress states corresponding to the measured pressures was found, but this calculation is very susceptible to the large errors possible in the parameters. Wafer thickness, diaphragm size, and device position are not known accurately enough to provide a good estimate of biaxial stress. Another possible reason for the reduced sensitivity is the geometry of the device. It is not possible to determine the resistance of the vias, which may have a small effect on the overall sensitivity. Furthermore, the doped pads may include additional transverse effects reducing sensitivity.

VDP vs. Rotational Misalignment

Because the VDP sensitivity changes with angle from the [110] direction, rotational misalignment will also affect the sensitivity of the device. The angular dependence on the NRCD has been found previously to be given by the plot of Figure 108.

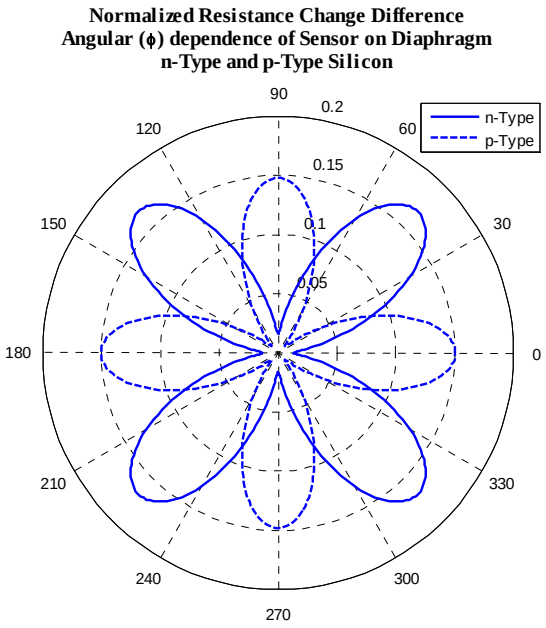


Figure 108: Angular dependence of NRCD

The diaphragms on the wafers which were designed to measure angular misalignment each contain four VDPs at 1° and 3° CW and CCW. Once again, because the piezoresistive coefficients are unknown for the fabricated devices, and because slight differences exist between the device model used by Law and the fabricated devices, this

discussion will also be limited to qualitative analysis. The results for angular dependence for both the fabricated devices, and the FE models are shown in Figure 109.

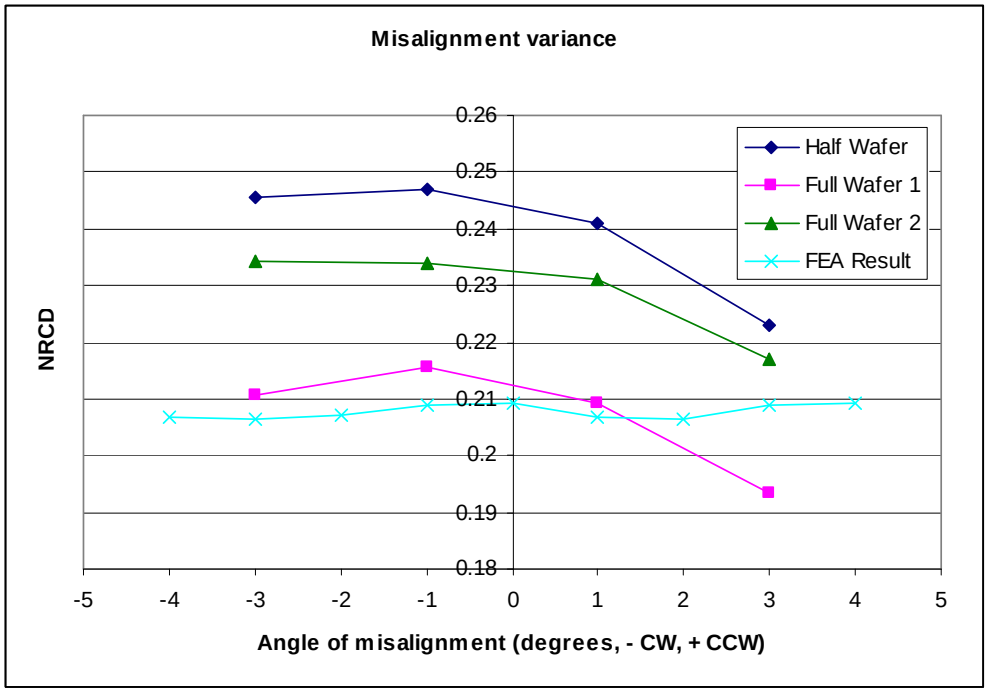


Figure 109: Angular misalignment variation of the NRCD. NRCD values are at 45.1kPa

The fabricated devices appear to be shifted towards the clockwise direction. This is hypothesized to be a result of misalignment during the application of the first photolithography mask, when alignment is done simply by attempting to line up the wafer flat with the mask coordinates. The differing scales should also be noted, as the fabricated resistors appear to be more sensitive to rotational misalignment. As stated, it is difficult to make a quantitative comparison of the two devices due to model differences, however, a clear trend downward with angular misalignment can be observed.

The effect of rotational misalignment on sensitivity can also be found analytically (see Appendix D). A plot of theoretical NRCD vs. angular misalignment is shown below in Figure 110.

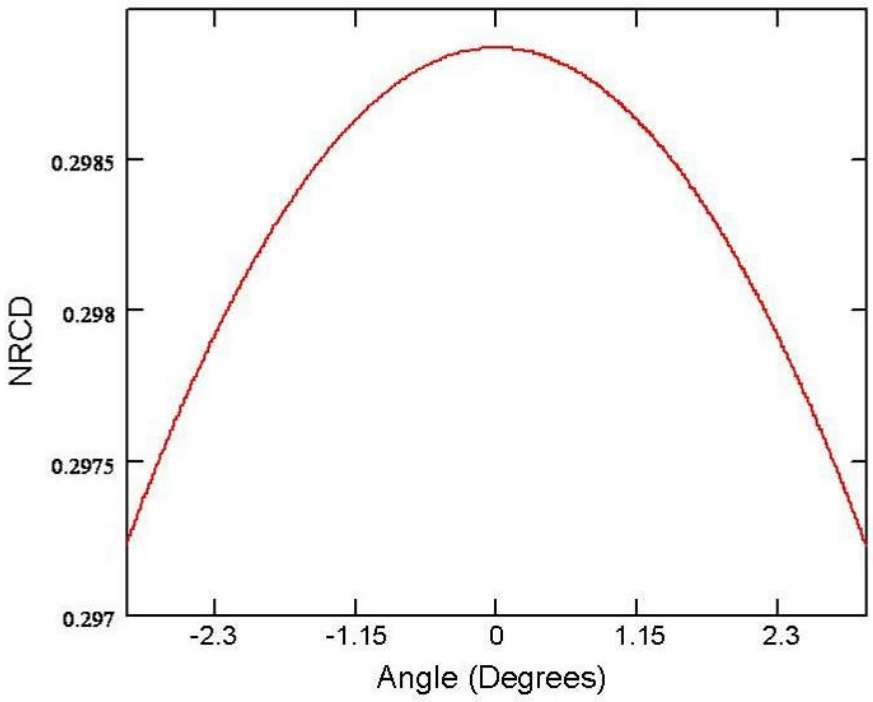


Figure 110: Theoretical NRCD vs. Angle under uniaxial stress of 100MPa.

Once again, the scales differ due to the lack of information regarding the piezoresistive coefficients, but qualitatively, theory matches the data.

VDP vs. Size

Theory indicates that sensitivity is independent of the size of the device, because for a square device, the lengths of the sides cancel out. The VDP device does depend on the stress state, which can vary over the area of the VDP. A larger VDP will be affected by

the average stress over its area. Because the curvature of the region over which the VDP lies is as shown in Figure 111, the result is a net reduction in stress felt as VDP size is increased.

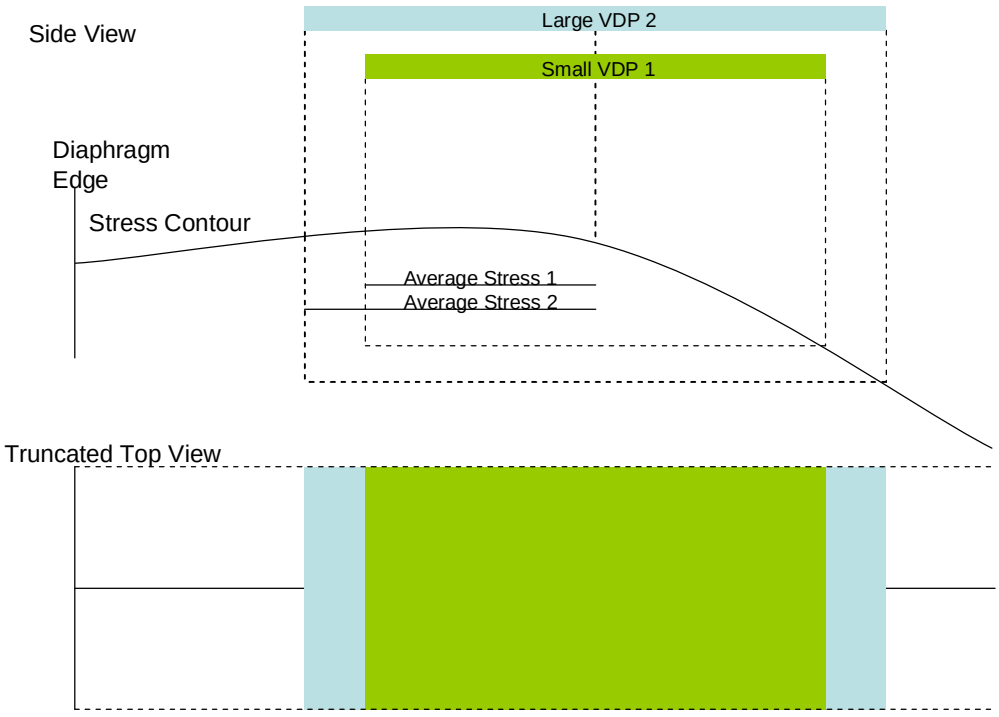


Figure 111: Illustration of theoretical decreasing sensitivity with size. The average stress seen by the smaller VDP is larger than that of the larger VDP.

The net reduction in stress leads to a reduction in sensitivity of the device as VDP area increases. Testing of the fabricated VDP devices yielded inconclusive data regarding the dependence of the VDP on size, as shown in Figure 112. Note that the data is for the maximum pressure difference of 45.1kPa.

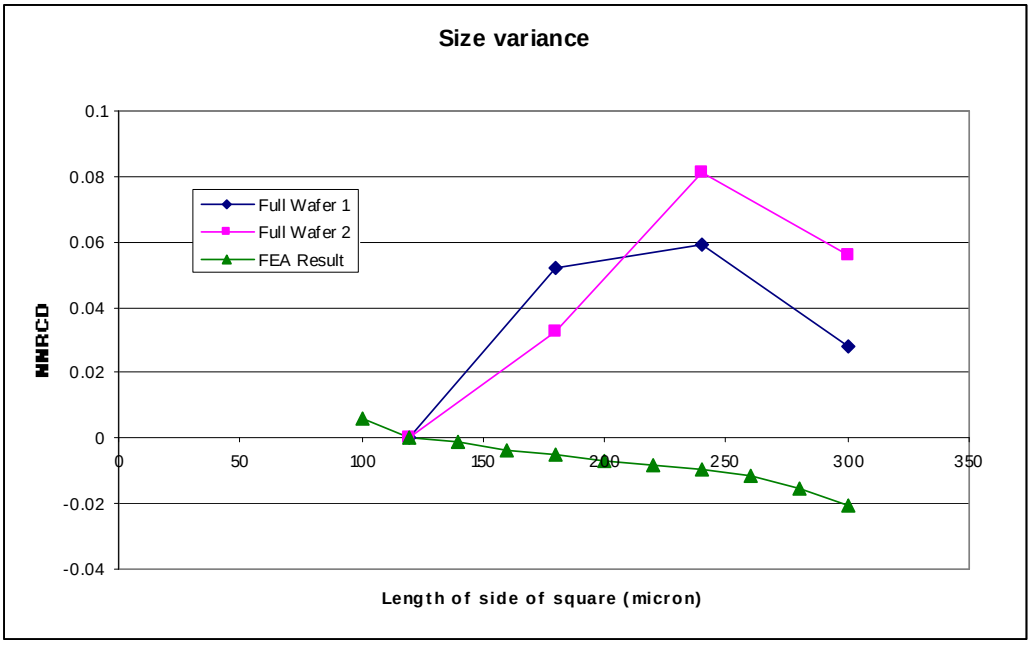


Figure 112: Normalized NRCD with respect to the length of a side of the VDP. Data is for 45.1kPa pressure difference.

Note that the plot in Figure 112 is of normalized NRCD, where the NRCD of both FEA and the data have been normalized to the NRCD of a 120µm VDP. Normalization was done due to data NRCD being in the range of approximately 0.25, while FEA was in the range of 0.20. NNRCD gives the percent change of the maximum NRCD as size changes. Notice that the percent change in NRCD from theory is only 2-3% while size triples. It's likely that measurement error has resulted in the larger percent change seen in the data, and because of this error, the trend cannot be seen.

VDP vs. Frame Device

The frame-shaped piezoresistive device [19] is an alternate form to the VDP, which is expected to be less sensitive based on the FEA results of Law. The relationship found by Law is shown in Figure 113.

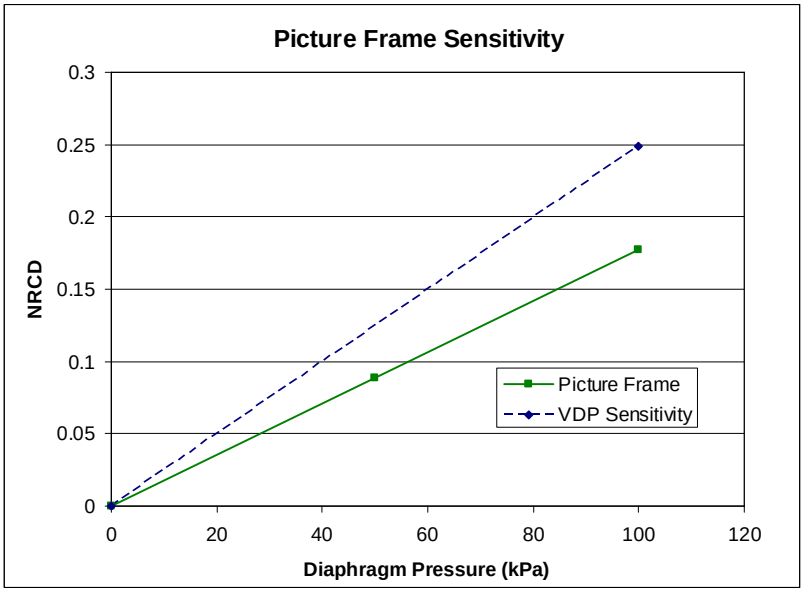


Figure 113: Law's FEA results for NRCD vs. pressure for the picture frame design and the VDP design. [9]

Two diaphragms of four frame devices each were tested to determine their NRCD. The results are shown in Figure 114.

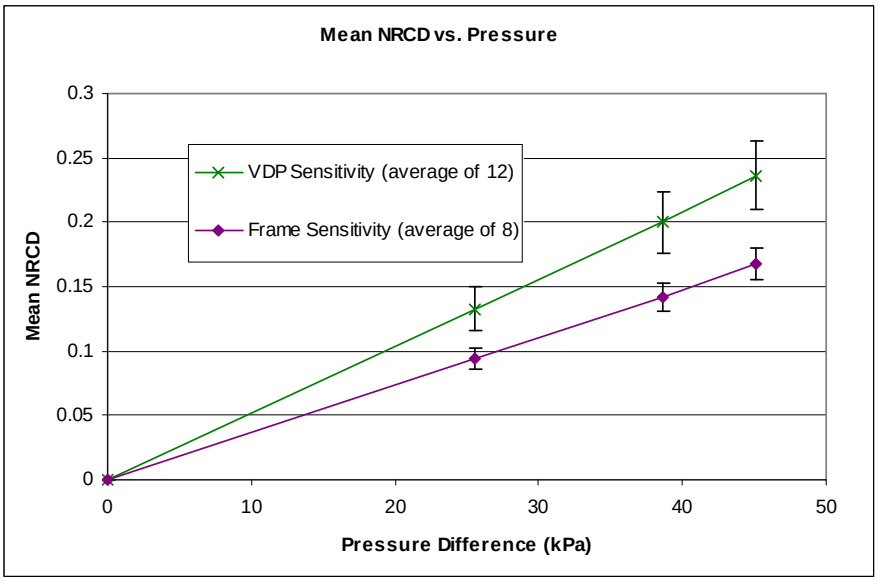


Figure 114: Average NRCD of 12 VDP devices across all three wafers vs. pressure compared with Average NRCD of 8 Frame devices. Error bars are standard deviations.

The frame device has a sensitivity of 3.72 MPa^{-1}, compared to 5.23 MPa^{-1} on average for the VDP devices. The result is as expected, with less piezoresistive area to produce resistance change, the sensitivity is reduced compared to the full VDP device.

CONCLUSIONS

In this thesis work, the VDP structure was fabricated and tested against a number of different parameters. The VDP devices, along with other piezoresistive structures, were designed to be fabricated onto a p-type Si wafer. Plate theory calculations, along with practical limitations dictated the design of the test wafer masks. During fabrication, the designed masks were used to create the micro-scale features using standard semiconductor lithography techniques. Finally, the wafers were tested and comparisons were made against the 3D FEA results performed previously by our group.

Beginning with the capabilities of the Montana Microfabrication Facility (MMF), a wafer type was chosen with the desired size, thickness, and dopant characteristics. Plate theory calculations, along with the piezoresistive properties of VDP sensors and characteristics of the required processing techniques determined the choice of wafer. The masks needed for the general process were created using standard mask making guidelines, while the initial process flow was finalized.

Creating the functioning pressure sensors was the next task, on which much of this thesis work was spent. While much of the processing worked properly, issues with thin photoresist layer remnants, pinholes due to oxide mask imperfections during bulk silicon etching, and large pressure differences in the sealed diaphragms processing under vacuum required additional processing to ensure functioning sensors. Due to these issues, only two complete wafers, and one partially damaged wafer were completed of nine wafers which began processing. A number of issues with initial and subsequent mask

misalignment, imprecise photolithography features, undercutting during oxide etch, etc. were unavoidable and may have resulted in degraded device sensitivity.

Testing of the sensors was done using a pressure chamber apparatus built by an undergraduate group, and calibrated using a factory calibrated vacuum gauge. While the data is qualitatively similar to the data obtained from FEA, no method for determining the exact piezoresistive coefficients obtained for the fabricated devices, making quantitative conclusions difficult to obtain.

It was found, however, that the VDP device has a clear advantage in sensitivity over both the serpentine resistor device and a frame-style piezoresistive device, while its simple geometry relative to these devices simplifies fabrication. In addition, the VDP device sensitivity is independent of line resistances, and appears to have little discernable dependence on VDP size. Both of these qualities allow for considerable miniaturization of both the device itself, and the lines which provide measurability, while maintaining the device performance.

ONGOING WORK

A primary issue in determining quantitative conclusions using the fabricated devices was the inability to determine the piezoresistive coefficients of the devices. A test strip was designed into the wafer for this purpose, however, obtaining measurements from the strip during testing would be difficult without an additional support apparatus for the micropositioners. While this is recommended for future work, only a single test strip remains largely undamaged, and only two may be testable. The reason for this is the strip's proximity to the wafer flat, where the wafer is typically handled from. It may be possible to use the existing test strips, but a more reliable approach would involve mask redesign to create strips which are less likely to be damaged during processing.

A number of additional structures have been designed into the wafer, and which were successfully fabricated, but were not tested for this thesis work. Additional testing of the VDP devices which have a different via design, the eight terminal VDP devices, and the large center diaphragm VDP array should be done. Also, the FTT devices were not measured and should be compared to the VDP devices. Lastly, the small diaphragms should be tested and compared to the large diaphragm devices.

RECOMMENDATIONS

During the design and fabrication of the sensors, a number of unexpected issues were discovered. It is recommended that certain amendments be made to the design and processing for certain scenarios.

A primary issue encountered during fabrication was the proximity of some devices to the wafer edge, particularly the test strip. In future designs, it is recommended that all devices which are necessarily functional be placed at least 1cm from the wafer edge. Additionally, contact pads should be placed at least 5mm from the edge of dicing lines to ensure chipping does not affect the pads.

Another issue encountered was the width of the alignment marks. The infrared light source does not cover the entire backside of the wafer, so alignment marks must be positioned properly. The marks used in the sensor fabrication were very near the outside edge of the light source, and should be moved inward in any future designs.

During oxide etching, it was often found that thin photoresist layers were not being entirely removed during development, possibly due to insufficient exposure dose. It was also found that the thin photoresist layer corresponded highly with damaged severely damaged devices after oxide etch. While increased exposure times may remove these remnants, this may cause a loss of pattern quality. It is recommended that a short (45s) plasma ash is done following photolithography of any pattern with feature sizes to be removed of greater than around 500µm, prior to oxide etching. This should be sufficient to remove the photoresist layer.

As described in the wafer processing section of this thesis, pinholes during bulk etching caused by imperfections in the masking frontside oxide layer caused issues that made photolithography of the affected wafer impossible, and also would have created large stress concentrations in the diaphragms, likely leading to failure, and certainly leading to incorrect results. To easily avoid these imperfections, simply bond a protective wafer to the frontside of the device wafer. The protective wafer should be oxidized, and it was found that bonding the frontsides of two device wafer worked well to protect both. High-temperature WaferGrip is recommended for bonding, as its softening point is 93°C, which allowed for TMAH etching at 75°C without any significant debonding or attacking of the WaferGrip beyond the edges of the wafers.

Also described in the wafer processing section is the difficulty of debonding wafers which have been bonded with high-temperature WaferGrip. Mechanical separation is not recommended, as it can crack the wafers, especially a fragile wafer that has been bulk etched. SVC-175 photoresist stripper is also not recommended for debonding. Though SVC-175 will attack the WaferGrip, its flash point is 104°C, only slightly above the softening point of the WaferGrip, and well below its melting point (115°C). With the WaferGrip below its melting point, the solution won't flow, dramatically increasing debonding time. A proprietary solution of StripAid from Dynatex, Inc, who produces WaferGrip, has a flash point of 212°C, and was found to give much better results. Also, the dimpling caused by the pressure difference in the diaphragms significantly increases the necessary time to debond the wafers, as the pressure difference acts to enhance the seal between the wafers, making it more difficult for the solution to attack the WaferGrip.

When debonding sensor wafers from handle wafers, agitation and an increased solution temperature of 180-185°C is recommended. Note that high-temp WaferGrip is not recommended above 190°C.

It is not recommended that diaphragms which cannot withstand a 1 atm pressure difference are fabricated using the process flow described in this thesis work. The vapor-prime oven and the aluminum PVD equipment apply vacuum to the sensor wafer/device wafer bonded combination, which contains air at approximately atmospheric pressure (slightly less due to bonding temperature) which was trapped during wafer bonding. The vacuum conditions can cause the diaphragms to burst under these conditions. If diaphragms which cannot withstand a 1 atm pressure difference are desired, the process flow should be modified. It may be possible to create such devices by applying the lines prior to bulk etching, protecting the backside oxide mask with a bonded wafer during BOE steps, then using dual-doped TMAH or a frontside bonded protective wafer to protect the lines and prevent pinhole formation during bulk etching. Dual-doping TMAH with silicic acid and ammonium peroxodisulphate (AP) has been shown to significantly reduce aluminum etch rate while maintaining a high silicon etch rate [30].

REFERENCES

1. W. G. Pfann, R.N.T., "Semiconducting Stress Transducers Utilizing the Transverse and Shear Piezoresistance Effects". *Journal of Applied Physics*, 1961. **32**(10): p. 2008-2019.

2. Smith, C.S., "Piezoresistance Effect in Germanium and Silicon," *Physical review*, 1954. **94**: p. 42-49.

3. P.J. French, A.G.R.e., "Polycrystalline Silicon as a Strain Gauge Material," *J. Phys. E: Sci. Instrum*, 1986. **19**: p. 1055-1058.

4. Jahsman, W.E., "Biaxial Gage Factor for Piezoresistive Strain Gages." *Experimental Mechanicas*, 1979. **19**(11): p. 411-415.

5. Mian, A., J.C. Suhling, and Richard C. Jaeger, "The van der Pauw Stress Sensor." *IEEE Sensors Journal*, 2006. **6**(2): p. 340-356.

6. "Silicon Crystal Structure and Growth." *Presentation accessed via:* www.usna.edu/EE/ee452/LectureNotes/05-Processing_Technology/18_Silicon .ppt

7. A. Mian, "Application of the van der Pauw Structure as a Piezoresistive Stress Sensor," Ph.D. dissertation, Dept. Mech. Eng., Auburn Univ., Auburn, AL, 2000.

8. D. A. Bittle, J.C.S., R.E. Beaty, R. C. Jaeger, R.W. Johnson, *Piezoresistive Stress Sensors for Structural Analysis of Electronic Packages.* Journal of Electronic Packaging, 1991. **113**: p. 203-214.

9. Law, Jesse T., "Application of the van der Pauw Structure as a Piezoresistive Pressure Sensor – A Numerical Study," MS Thesis, Dept Mech. Eng, Montana State University, MT, 2007.

10. Schmidt, R., "Universal intelligent pressure transducer for automotive applications," *Elektronic Praxis*, 2000. **No 20**: p. 62-64.

11. Schuster, J.P., "Automotive Silicon Based Pressure Transducers for Fluid Power Applications," in *Proceeding of the National Conference on Fluid Power,Annual Meeting*. 1986.

12. van der Pauw, L.J., "A Method of Measuring Specific Resistivity and Hall Effect of Discs of Arbitrary Shape," *Philips Research Reports*, 1958. **13**: p. 1-9.

13. van der Pauw, L.J., "Determination of Resistivity Tensor and Hall Tensor of Anisotropic Conductors," *Philips Research Reports*, 1961. **16**: p. 187-195.

14. Mian, A.K.M., J.C. Suhling, and R.C. Jaeger. "Sensitivity of (100) Silicon VDP Sensors to Uniaxial and Hydrostatic Loads," in *Proceedings of SECTAM-XX*. 2000. Callaway Gardens, Pine Mountain, GA.

15. W. L. V. Price, "Electric potential and current distribution in a rectangular sample of anisotropic material with application to measurement of the principal resistivities by an extension of van der Pauw's method," *Solid State Electron*, July 1973, vol.16, no.7, pp.753-62.

16. Skaguchi, Kiyofumi, Takao Yonehara, "SOI Wafers Based on Epitaxial Technology," *Solid State Technology*, June 2000, accessed via: http://sst.pennnet.com/display_article/75323/5/ARTCL/none/none/1/SOI-wafers-based-on-epitaxial-technology/

17. Petersen, Kurt E., "Silicon as a Mechanical Material," *Proceedings of the IEEE*, May1982, vol.70, no.5, pp. 421.

18. Urugal, A.C., *Stresses in Plates and Shells*, 1981, McGraw-Hill, Inc.

19. Senturia, Stephen D., *Microsystem Design*, 2001, New York: Springer Science+Business Media, LLC.

20. Morita, M., T. Ohmi, E. Hasegawa, M. Kawakami, and M. Ohwada, "Growth of native oxide on a silicon surface," *J. Appl. Phys.*, Vol. 68, No.3, August 1990,

21. Li, Yunqiang, Muthukumaran Packirisamy, Rama B. Bhat, "Shape optimizations and static/dynamic characterizations of deformable microplate structures with multiple electrostatic actuators," *Microsystem Technologies*, v14, n 2, Feb 2008, p255-256

22. Hendricks, Robert W., "Oxidation Theory," Sept 2002, Virginia Tech, accessed via: http://www.mse.vt.edu/faculty/hendricks/courses/mse2224/manual/oxidation_theory.htm.

23. "Thermal Oxidation," 2004, www.SiliconFarEast.com, accessed via: http://www.siliconfareast.com/oxidation2.htm

24. "Spin Coat Theory," Columbia Center for Integrated Science & Engineering, Cost Effective Equipment, accessed via: http://www.cise.columbia.edu/clean/process/-spintheory.pdf

25. SHIPLEY 1800 Series Photoresist Data Sheet, SHIPLEY

26. Kaiser, Todd, Andrew Lingley, Matt Leone, Brad Pierson, "MEMS fabrication as a multidisciplinary laboratory," *2007 ASEE Annual Conference and Exposition*, Conference Proceedings, 2007 8p.

27. Nanostrip, Cyantek Corporation, 3055 Osgood Court, Fremont, California 94539-5652, 510-651-3341

28. WaferGrip Adhesive, Dynatex, Inc., www.dynatex.com, 5577 Skylane Blvd, Santa Rosa, CA 95403, 1-707-542-4227

29. StripAid Debonding Solution, Dynatex, Inc., www.dynatex.com, 5577 Skylane Blvd, Santa Rosa, CA 95403, 1-707-542-4227

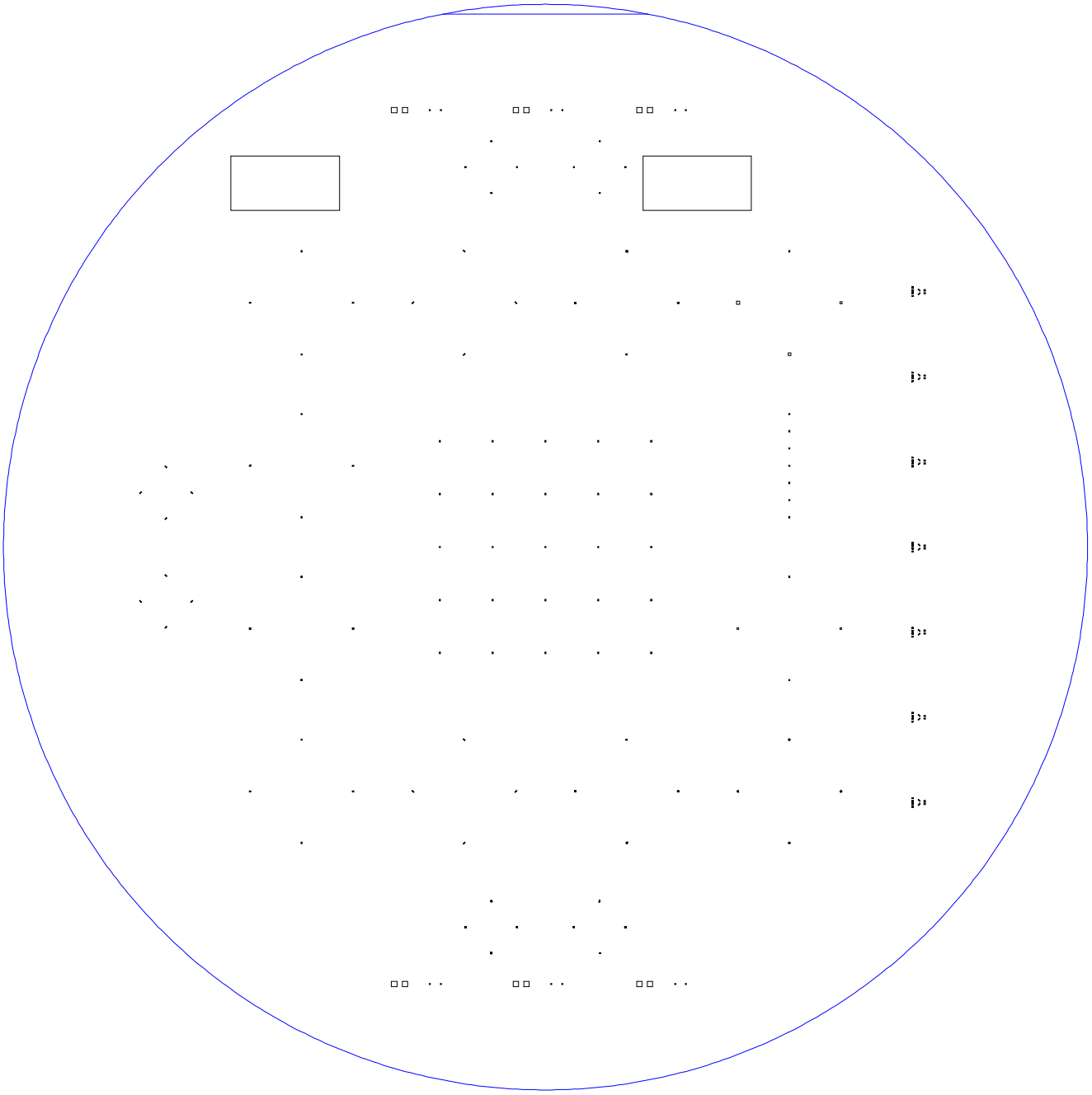
30. Biswas, K., S. Das, D.K. Maurya, S. Kal, and S.K. Lahiri, "Bulk Micromachining of Silicon in TMAH-based Etchants for Aluminum Passivation and Smooth Surface," *Microelectronics Journal*, v 37, n 6, June 2006, p. 519-525.

APPENDICES

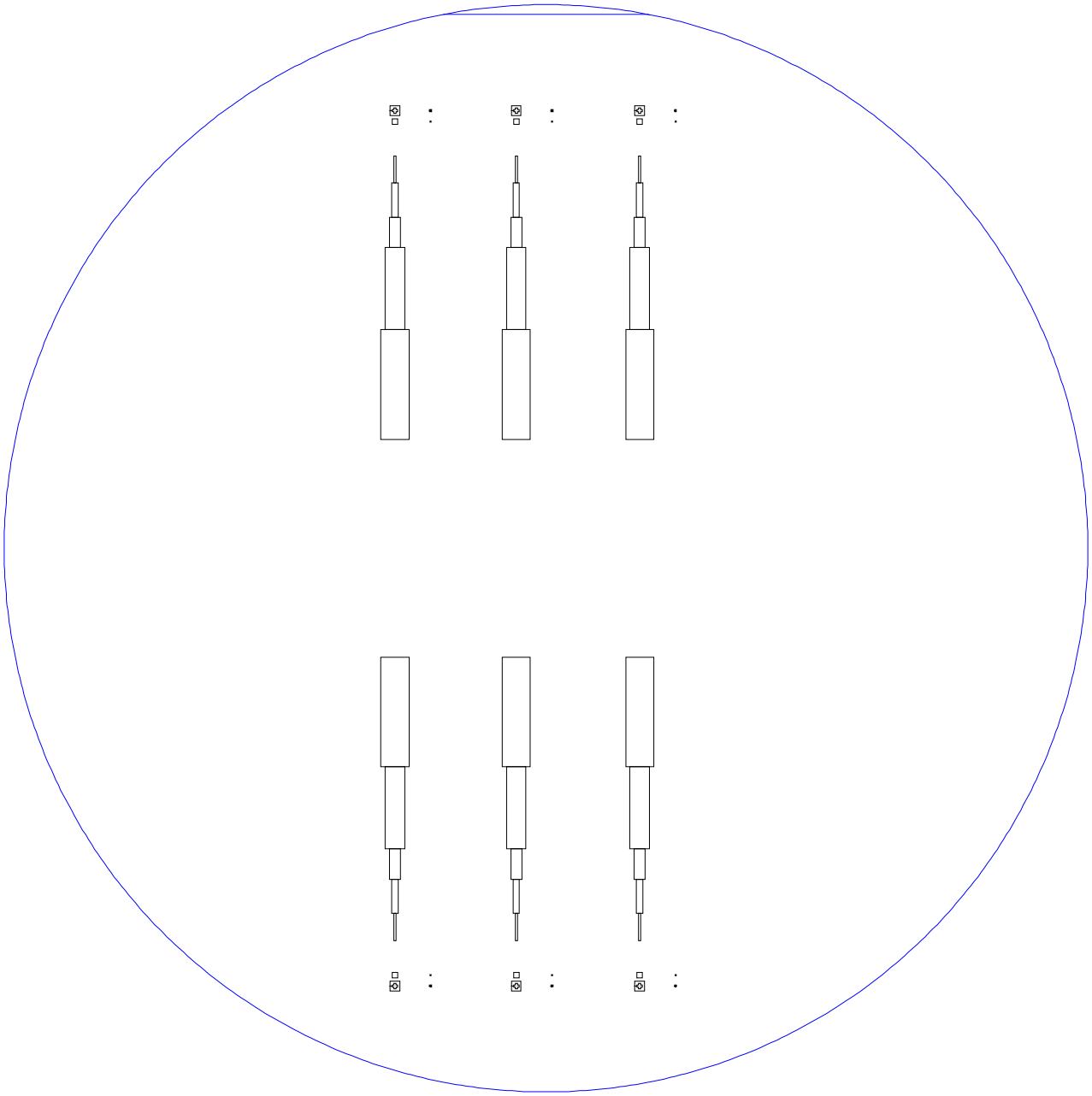
APPENDIX A

MASK IMAGES

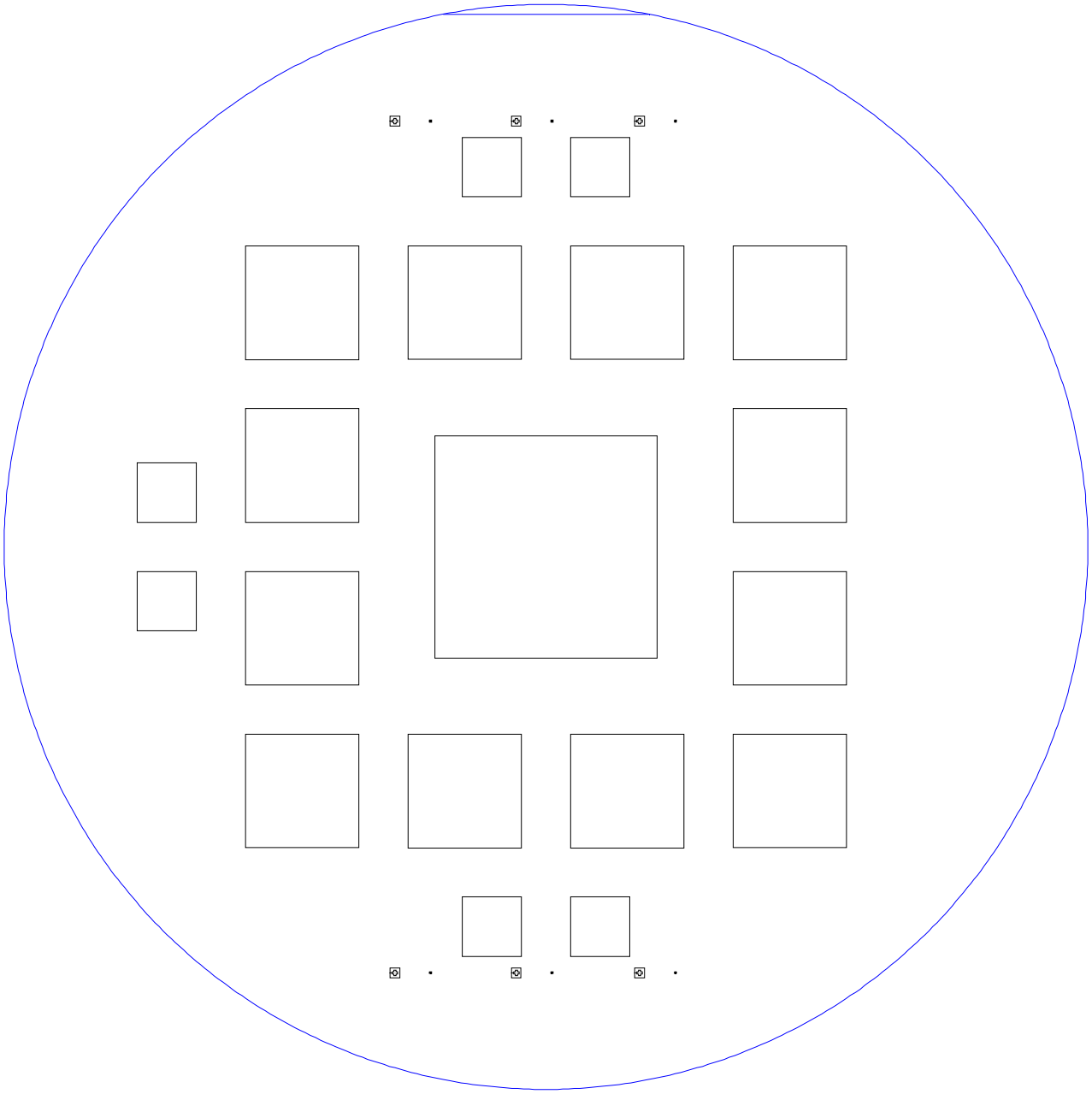
BORONDOPE



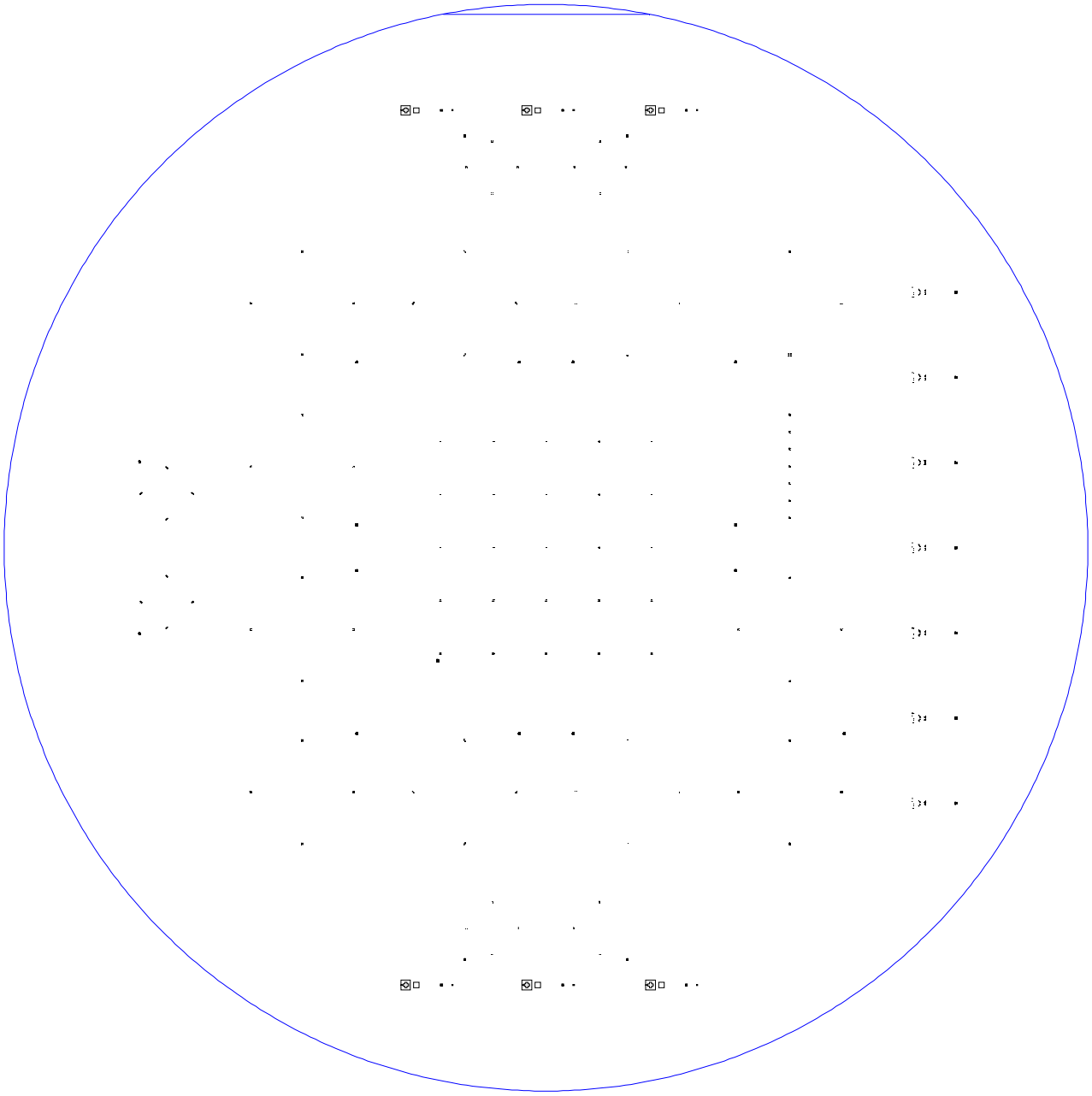
ALALIGN



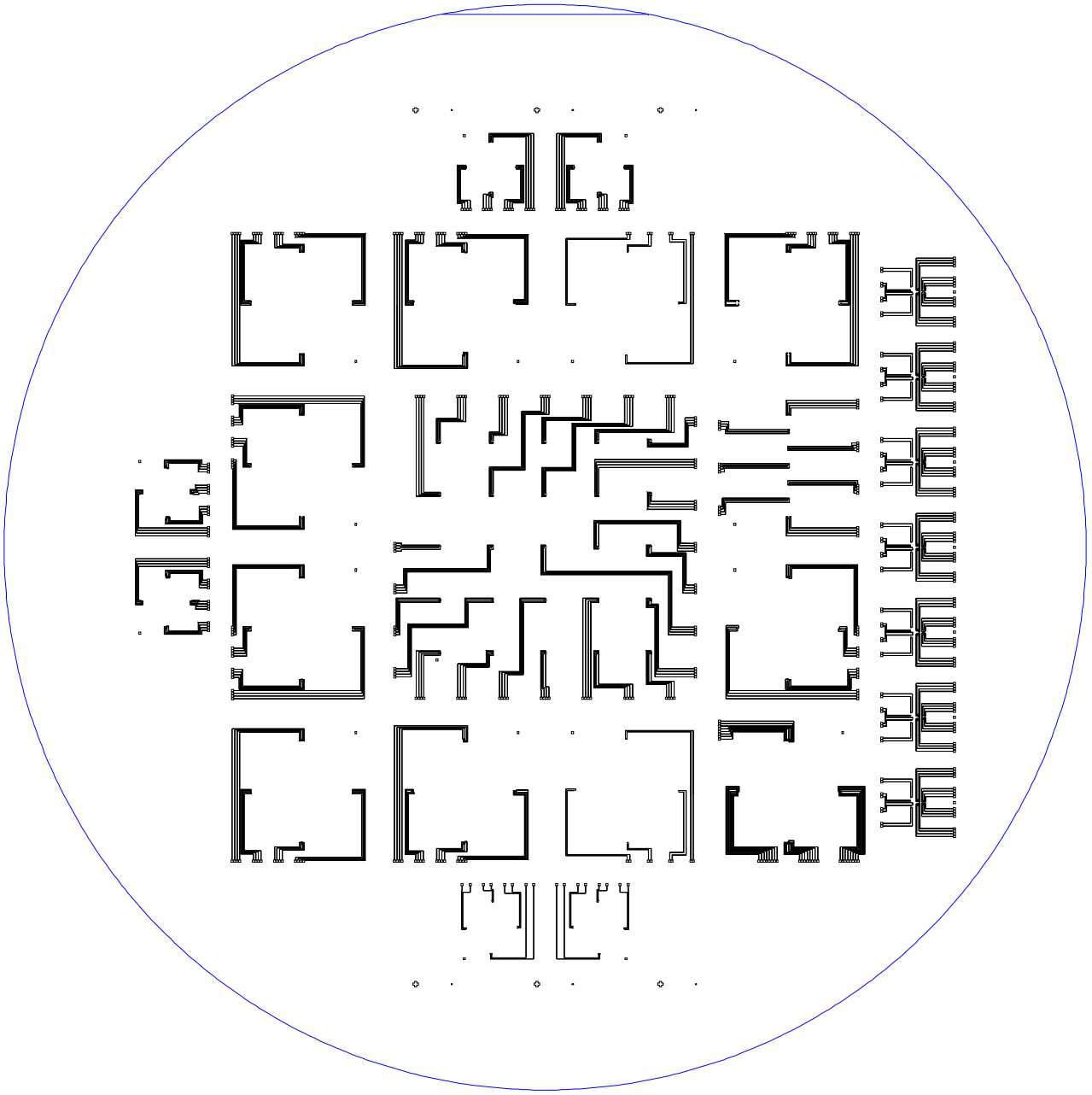
BACKETCH



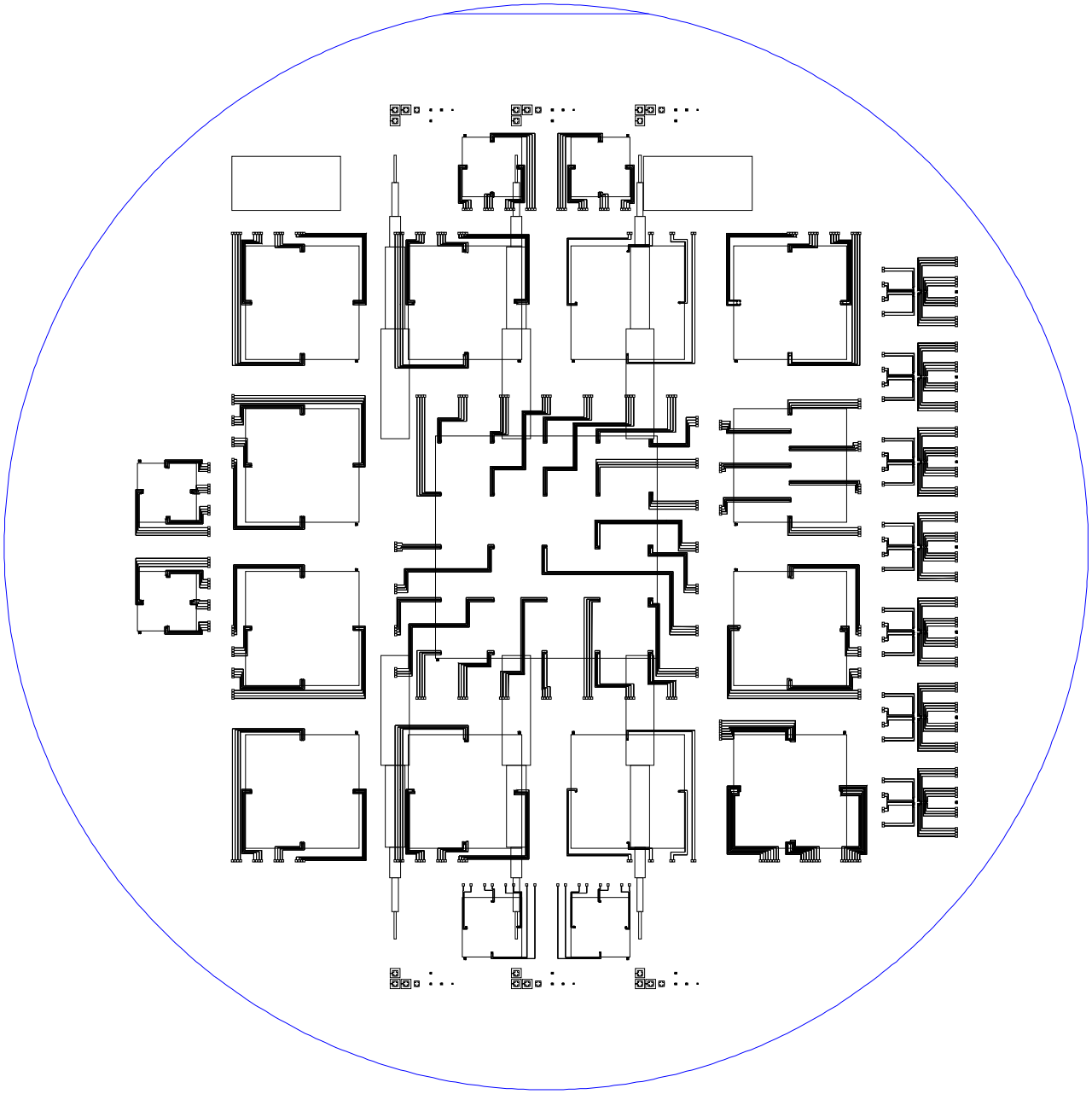
VIAS



ALCOMP



All masks superimposed



APPENDIX B

STRIPAID MSDS

dynatex™
INTERNATIONAL
semiconductor dicing equipment and materials

MATERIAL SAFETY DATA SHEET

DATE PREPARED: May 1, 2007

Dynatex International urges each customer or recipient of this MSDS to study it carefully to become aware of and understand the hazards associated with the product. The reader should consider consulting reference works or experts in ventilation, toxicology, and fire prevention, as necessary or appropriate to use and understand the data contained in this MSDS.

To promote safe handling, each customer or recipient should: (1) notify its employees, agents, contractors and others whom it knows or believes will use this material of the information in this MSDS and any other information regarding hazards or safety; (2) furnish this same information to each of its customers for the product; and (3) request customers to notify their employees, customers, and other users of the product of this information.

1. PRODUCT IDENTITY AND COMPANY CONTACT INFORMATION

Material Identity
Product Name: Strip Aid X Series
General or Generic ID: Phthalate Esters

Company
Dynatex International
5577 Skylane Blvd.
Santa Rosa, CA. 95403
707-542-4269

2. CHEMICAL COMPOSITION / INFORMATION ON INGREDIENTS

This product is hazardous as defined in 29 CFR1910.1200

3. HAZARDS IDENTIFICATION

Potential Health Effects

Eye:
Slightly irritating but does not injure eye tissue.

Skin:
Low order of toxicity. Prolonged or prolonged contact with skin my cause irritation.

Ingestion:
Minimal toxicity.

Inhalation:
Negligible hazard at ambient temperature (-18 to 38 Deg C; 0 to 100 Deg F).

4. FIRST AID MEASURES

Eyes:
For contact with eyes flush with water for 15 minutes, seek medical if any discomfort persists.

Skin:
Wash skin with soap and water.

Ingestion:
If a large quantity of material is swallowed, obtain medical attention.

Inhalation:
If irritation occurs proceed to a location where fresh air is readily available.

5. FIRE-FIGHTING MEASURES

Flash Point:
212 °C (Cleveland Open Cup)

Explosive Limit:
N/A

Autoignition Temperature:
N/A

General Hazard:
Low Hazard, liquid can burn upon heating to temperatures at or above the flashpoint.
Toxic gases will form upon combustion.
Static Discharge, material can accumulate static charges which can cause an incendiary electrical discharge.
"Empty" containers retain product residue (liquid and/or vapor) and can be dangerous.

Fire Fighting:
Use water spray to cool fire exposed surfaces and to protect personnel.
Isolate "fuel" supply from fire.
Use foam, dry chemical, or water spray to extinguish fire.
Respiratory and eye protection required for fire fighting personnel.

Decomposition Products Under Fire Conditions:
Fumes, smoke, carbon monoxide

6. ACCIDENTAL RELEASE MEASURES

Land Spill:
Eliminate sources of ignition. Prevent additional discharge of material, if possible to do so without hazard. For small spills implement cleanup procedures; for large spills implement cleanup procedures and, if in public area, keep public away and advise authorities. Prevent liquid from entering sewers, watercourses, or low areas. Contain spilled liquid with sand or earth. Recover by pumping or with a suitable absorbent. Consult an expert on disposal of recovered material and ensure conformity to local disposal regulations.

Water Spill:
Remove from surface by skimming or with suitable adsorbents. If allowed by local authorities and environmental agencies, sinking and/or suitable dispersants may be used in non-confined waters. Consult an expert on disposal of recovered material and ensure conformity to local disposal regulations.

7. HANDLING AND STORAGE

Storage Temperature:
Ambient 70-75 Deg. F

Loading/Unloading Temperature
Ambient 70-75 Deg. F

Storage & Handling:
Keep container closed. Handle and open containers with care. Store in a cool, well ventilated place away from incompatible materials. Do NOT handle or store near an open flame, heat or other sources of ignition. Protect material from direct sunlight. Material will accumulate static charges which may cause an electrical spark (ignition source). Use proper bonding and/or grounding procedures.
Do NOT pressurize, cut, heat, or weld containers. Empty product containers may contain product residue. Do NOT reuse empty containers without commercial cleaning or reconditioning.

8. EXPOSURE CONTROLS AND PERSONAL PROTECTION

Exposure Controls:
The use of local exhaust ventilation is recommended to control process emissions near the source. Laboratory samples should be handled in a lab hood. Provide mechanical ventilation of confined spaces. See respiratory protection recommendations.

Personal Protection:
For open systems where contact is likely, wear safety glasses with side shields, long sleeves, and chemical resistant gloves. Where contact may occur, wear safety glasses with side shields.
Where concentrations in air may exceed the limits given in this Section and engineering, work practice or other means of exposure reduction are not adequate, NIOSH approved respirators may be necessary to prevent overexposure by inhalation. Natural rubber, butyl rubber and PVC are not suitable protection; neoprene recommended.

Exposure Guidelines:
TWA of 5 mg/m3 for alkyl phthalates (C6-C13)

9. PHYSICAL AND CHEMICAL PROPERTIES

Boiling Point: Not Available	Density: 8.1 lbs/gallon at 68 F
Vapor Pressure: Negligible	Viscosity: 55 cSt at 68 F
Specific Gravity: 0.97 at 68 F	Percent Volatiles (wt %): 0.0034, by EPA Method 24
Evaporation Rate: Negligible	Appearance: Cloudy, oily
State: Liquid	Odor: Characteristic
PH: N/A	Solubility in Water: Negligible

10. STABILITY AND REACTIVITY

Hazardous Polymerization:
Product will not undergo hazardous polymerization.

Hazardous Decomposition:
None.

Chemical Stability:
Stable.

Chemical Incompatibility:
Avoid strong oxidizing agents

11. TOXICOLOGICAL INFORMATION

Please refer to Section 3 for available information on potential health effects.

12. ECOLOGICAL INFORMATION

No specific ecological data are available for this product. Please refer to Section 6 for information regarding accidental releases and Section 15 for regulatory reporting information.

13. DISPOSAL CONSIDERATIONS

Please refer to Sections 5, 6 and 15 for disposal and regulatory information.

Waste Management Information:
Dispose of waste in accordance with federal, state and local regulations. Incinerate in a licensed facility. So not discharge into waterways or sewer systems. Note: this material is not a hazardous waste under RCRA; it can be disposed of at a licensed facility.

14. TRANSPORT INFORMATION (NON-BULK)

D.O.T. PROPER SHIPPING NAME:
None

HAZARDOUS SUBSTANCE (CERCLA):
No

D.O.T. HAZARD CLASSIFICATION:

PRIMARY: None

SECONDARY: None

D.O.T. LABELS REQUIRED:
None

D.O.T. PLACARDS REQUIRED:
None

BILL OF LADING DESCRIPTION:
Non-Hazardous cleaner, stripper.

UN/NA CODE:
N/A

15. REGULATORY INFORMATION

TSCA:
This product is listed on the TSCA Inventory at CAS Registry Number 68515-45-7

CERCLA:
If this product is accidentally spilled, it is not subject to any special reporting under the requirements of the Comprehensive Environmental Response, Compensation and Liability Act. We recommend you contact local authorities to determine if there may be other local reporting requirements.

SARA TITLE III:
Under the provisions of Title III, Sections 311/312 of the Superfund Amendments and Reauthorization Act, this product is classified into the following hazard categories: Not Hazardous.

Hazard Ratings:

	Health	Fire	Reactivity	Special
HMIS	1	1	0	NA
NFPA	0	1	0	NA

16. OTHER INFORMATION

SA-103-99	Quart Sample
SA-103-00	1 Gallon
SA-103-05	5 Gallon
SA-103-55	55 Gallon

Shelf Life: 2 years

Although the information and recommendations set forth herein are presented in good faith and believed to be correct, Dynatex International makes no representations as to their completeness or accuracy. Information is supplied upon the condition that the persons receiving will make their own verification and determination as to its suitability for their purposes prior to use. In no event will Dynatex International be responsible for damages of any nature whatsoever resulting from the use of or reliance upon this information.

NO REPRESENTATION OR WARRANTIES, EITHER EXPRESSED OR IMPLIED, OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR ANY OTHER NATURE ARE MADE HEREUNDER WITH RESPECT TO INFORMATION OR PRODUCT TO WHICH INFORMATION REFERS.

EMERGENCY TELEPHONE NUMBER: (707) 542-4227

APPENDIX C

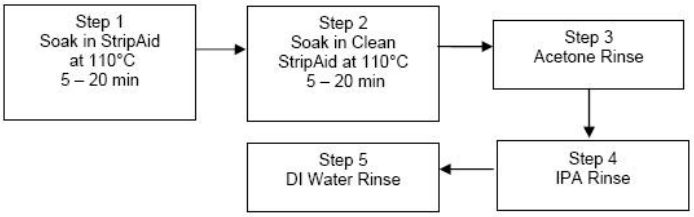
STRIPAID TECHNICAL DATA SHEET

StripAid™ X Series Specialty Solvent

Typical Physical Properties	*Value*
Specific Gravity @ 68°F	0.97
Density @ 68°F, lbs/gallon	8.1
Solubility in Water	Negligible
Water Solubility in Strip Aid @25°C, % by weight	0.2
Absolute Viscosity 68°F, cSt	55
Flash Point, °C	212
Vapor Pressure	Negligible
Color	Cloudy
Odor	Mild

Application

StripAid is specially formulated to remove WaferGrip Temporary adhesives. The following are recommended process steps.



Safety

Because StripAid has a low order of toxicity, it does not require special handling. Always use good industrial hygiene and safety practices. See the StripAid MSDS for complete safety, handling, storage and disposal information.

Storage

StripAid should be stored away from direct sunlight. Proper storage temperatures range from 20°C to 25°C. So not store under freezing conditions.

dynatex INTERNATIONAL
semiconductor dicing equipment and materials
5577 Skylane Boulevard
Santa Rosa, CA 95403
Phone: 707.542.4227
Fax: 707.579.8599
www.dynatex.com
sales@dynatex.com

DATA SHEET

StripAid Specialty Solvent Technical Data Sheet

APPENDIX D

ANALYTICAL MISALIGNMENT SENSITIVITY VARIATION CALCULATION

P-Type, phi

$p11 := 6.6 \cdot 10^{-11}$ $\quad \sigma 11 := 100 \cdot 10^{6}$ $\quad \rho := .078$

$p12 := -1.1 \cdot 10^{-11}$

$p44 := 138.1 \cdot 10^{-11}$

$B1 := \frac{p11 + p12 + p44}{2}$ $\quad B2 := \frac{p11 + 5p12 - p44}{6}$ $\quad 20 \cdot \frac{\pi}{180} = 0.349$

$\rho 11p(x) := \rho \cdot (1 + B1 \cdot \sigma 11)$

$\rho 22p(x) := \rho \cdot (1 + B2 \cdot \sigma 11)$

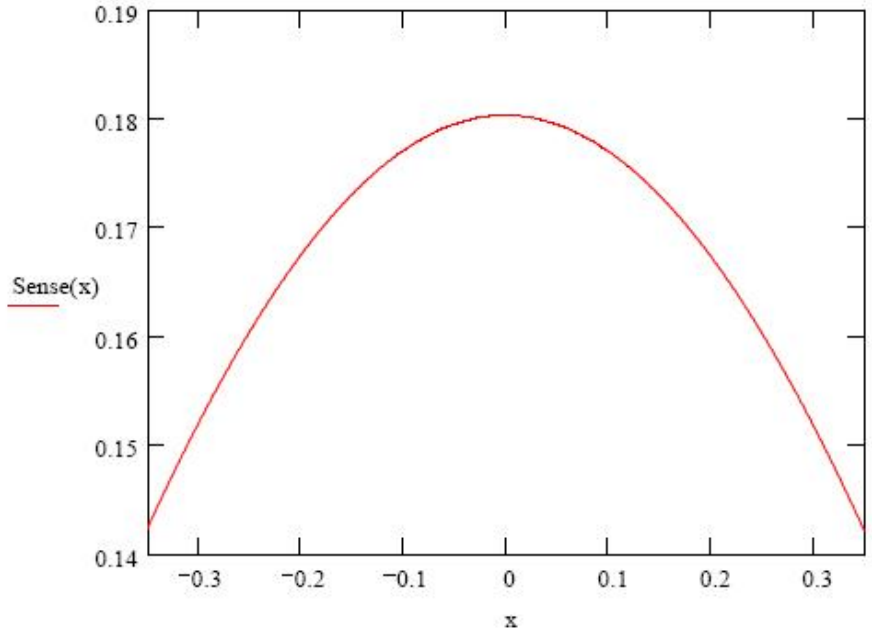
$\rho 12p(x) := 0$

$\rho 11pp(x) := \rho 11p(x) \cdot \cos(x)^2 + \rho 12p(x) \cdot \sin(2x) + \rho 22p(x) \cdot \sin(x)^2$

$\rho 22pp(x) := \rho 11p(x) \cdot \sin(x)^2 + \rho 12p(x) \cdot \sin(2x) + \rho 22p(x) \cdot \cos(x)^2$

$\rho 12pp(x) := \frac{\rho 11p(x) - \rho 22p(x)}{2} \cdot \sin(2x) + \rho 12p(x) \cdot \cos(2x)$

$$Sense(x) := \frac{\sqrt{\rho 11pp(x) \cdot \rho 22pp(x) - \rho 12pp(x)^2}}{\rho} \cdot \left(\frac{\ln\left(\tanh\left(\sqrt{\frac{\rho 22pp(x)}{\rho 11pp(x)}} \cdot \frac{\pi}{2} \right) \cdot \tanh\left(\sqrt{\frac{\rho 22pp(x)}{\rho 11pp(x)}} \cdot \frac{3 \cdot \pi}{2} \right) \right)}{\ln\left(\tanh\left(\frac{\pi}{2} \right) \cdot \tanh\left(\frac{3 \cdot \pi}{2} \right) \right)} \right) - 1$$



P-Type, phi+ 90 degrees

$p11 := 6.6 \cdot 10^{-11}$

$p12 := -1.1 \cdot 10^{-11}$

$p44 := 138.1 \cdot 10^{-11}$

$\sigma 11 := 100 \cdot 10^{6}$

$\rho := .078$

$B1 := \frac{p11 + p12 + p44}{2}$ $B2 := \frac{p11 + 5p12 - p44}{6}$

$\rho 11p(x) := \rho \cdot (1 + B1 \cdot \sigma 11)$

$\rho 22p(x) := \rho \cdot (1 + B2 \cdot \sigma 11)$

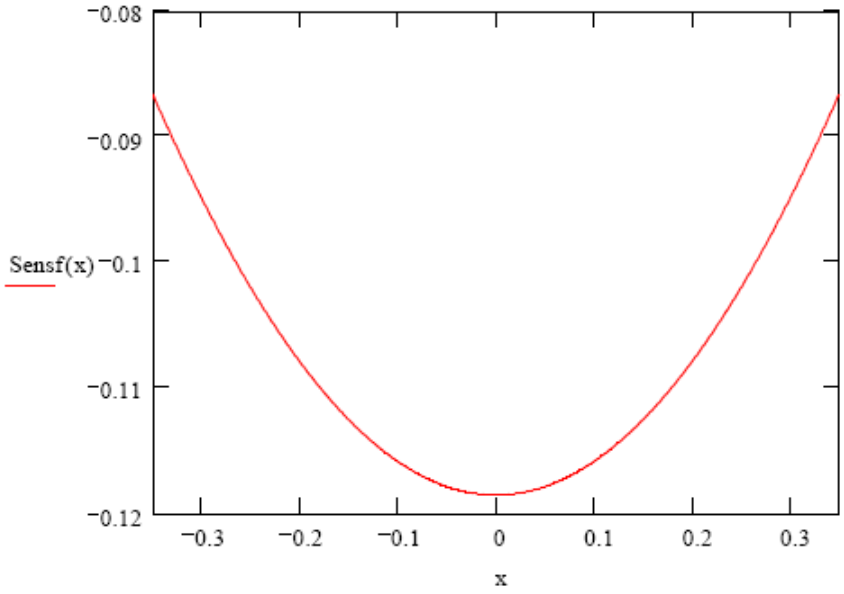
$\rho 12p(x) := 0$

$\rho 11pp(x) := \rho 11p(x) \cdot \cos(x)^2 + \rho 12p(x) \cdot \sin(2x) + \rho 22p(x) \cdot \sin(x)^2$

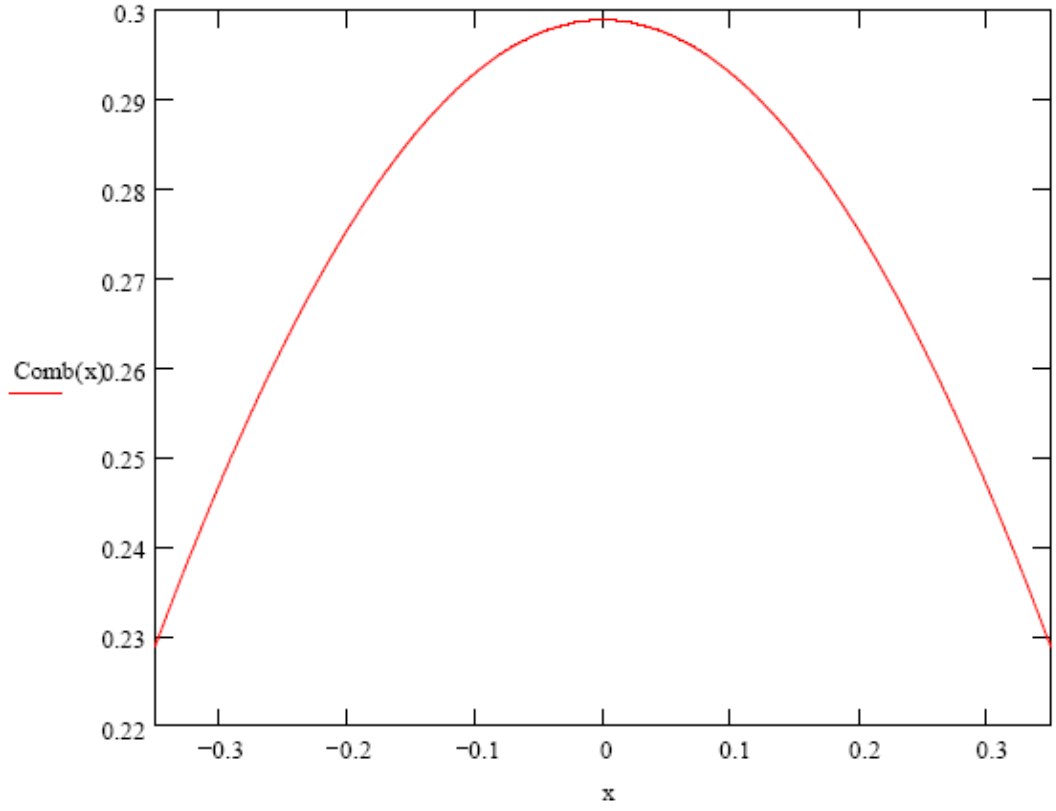
$\rho 22pp(x) := \rho 11p(x) \cdot \sin(x)^2 + \rho 12p(x) \cdot \sin(2x) + \rho 22p(x) \cdot \cos(x)^2$

$$\rho 12pp(x) := \frac{\rho 11p(x) - \rho 22p(x)}{2} \cdot \sin(2x) + \rho 12p(x) \cdot \cos(2x)$$

$$Sensf(x) := \frac{\sqrt{\rho 11pp(x) \cdot \rho 22pp(x) - \rho 12pp(x)^2}}{\rho} \cdot \left(\frac{\ln\left(\tanh\left(\sqrt{\frac{\rho 11pp(x)}{\rho 22pp(x)}} \cdot \frac{\pi}{2} \right) \cdot \tanh\left(\sqrt{\frac{\rho 11pp(x)}{\rho 22pp(x)}} \cdot \frac{3 \cdot \pi}{2} \right) \right)}{\ln\left(\tanh\left(\frac{\pi}{2} \right) \cdot \tanh\left(\frac{3 \cdot \pi}{2} \right) \right)} \right) - 1$$



$$Comb(x) := Sense(x) - Sensf(x)$$



Here, x is angle in radians, and Comb(x) is NRCD. For the plot in the figure, the x axis has simply been changed to degrees.