



Analysis, modeling and design of utility line current conditioner
by Kamalesh Chatterjee

A thesis submitted in partial fulfillment of the requirement for the degree of Master of Science in
Electrical Engineering
Montana State University
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Abstract:

Data processing devices such as a computer typically feature a diode bridge rectifier at the front end of the power circuit. The diode bridge rectifier, in conjunction with its capacitive filter is a nonlinear load. The device draws current with a high crest factor and rich in harmonics. These harmonic currents cause power quality problems. Such problems have prompted the development of unity power factor rectifiers, which use active current shaping techniques to draw sinusoidal current from the supply. However, such unity power factor rectifiers have not become popular in commercial data processing devices. Incorporating unity power factor rectifier in every device would lead to additional cost. Power quality problems become noticeable only in places where the loading by the data processing devices is substantial part of the total load. There is not enough incentive for the manufacturers to incorporate unity power factor rectifier with every device. Moreover, consumers usually place higher premium in processor speed, memory size, etc.

This thesis presents an alternative approach to solve power quality problems in such scenarios, only when the problems become severe and cause persistent malfunction. The proposed Utility Line Current Conditioner is based on a boost type ac to ac converter topology. The converter would act as an interface between the supply line and the non-linear load. The boost ac-ac converter is adapted to perform line current control in a single-phase line, loaded by a rectifier load. An inner average current control loop and an outer voltage control loop are used to perform the active wave shaping function.

This thesis presents detailed analysis of the basic converter topology, principle of operation, defining equations and design techniques. The dynamic models incorporate high frequency small signal model for the current control loop and a low frequency model for the voltage control loop. The modeling technique is versatile and could be directly applied to ac to dc unity power factor rectifiers as well. Dynamic performance characteristics of the overall system are discussed. Experimental results for a prototype 750 W converter are presented.

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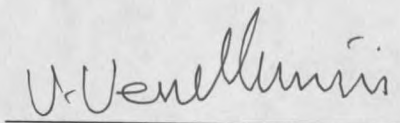
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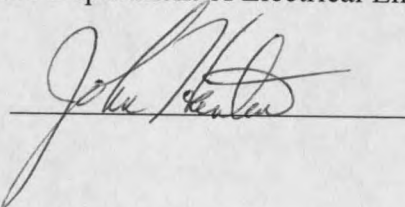
This thesis has been read by each member of the thesis committee and has been found to be satisfactory regarding content, English usage, format, citations, bibliographic style, and consistency, and is ready for submission to the College of Graduate Studies.

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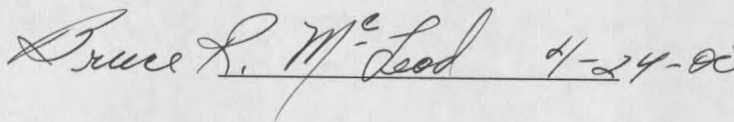
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ABSTRACT

Data processing devices such as a computer typically feature a diode bridge rectifier at the front end of the power circuit. The diode bridge rectifier, in conjunction with its capacitive filter is a nonlinear load. The device draws current with a high crest factor and rich in harmonics. These harmonic currents cause power quality problems. Such problems have prompted the development of unity power factor rectifiers, which use active current shaping techniques to draw sinusoidal current from the supply. However, such unity power factor rectifiers have not become popular in commercial data processing devices. Incorporating unity power factor rectifier in every device would lead to additional cost. Power quality problems become noticeable only in places where the loading by the data processing devices is substantial part of the total load. There is not enough incentive for the manufacturers to incorporate unity power factor rectifier with every device. Moreover, consumers usually place higher premium in processor speed, memory size, etc.

This thesis presents an alternative approach to solve power quality problems in such scenarios, only when the problems become severe and cause persistent malfunction. The proposed Utility Line Current Conditioner is based on a boost type ac to ac converter topology. The converter would act as an interface between the supply line and the non-linear load. The boost ac-ac converter is adapted to perform line current control in a single-phase line, loaded by a rectifier load. An inner average current control loop and an outer voltage control loop are used to perform the active wave shaping function.

This thesis presents detailed analysis of the basic converter topology, principle of operation, defining equations and design techniques. The dynamic models incorporate high frequency small signal model for the current control loop and a low frequency model for the voltage control loop. The modeling technique is versatile and could be directly applied to ac to dc unity power factor rectifiers as well. Dynamic performance characteristics of the overall system are discussed. Experimental results for a prototype 750 W converter are presented.

CHAPTER – 1

INTRODUCTION

Electrical power distribution systems almost universally operate as sinusoidal ac voltage sources. The properties of the load determine the amplitude and the waveform of the current drawn from the voltage source. Most lighting loads, heating loads and motor loads are linear loads. When supplied by a sinusoidal voltage source, the current drawn is also sinusoidal. Most data processing devices require dc power source. The dc power is derived from the ac supply by using a rectifier, terminated by a filter. The rectifier-filter is a non linear load. Current drawn from the supply by such loads is not sinusoidal and is rich in harmonics.

Harmonic currents generate electromagnetic interference and affect other devices connected to the same supply line. They also result in degradation of the supply voltage waveform quality. Harmonic currents also result in an increase of rms value of the line current without contributing to the power transfer, resulting in under-utilization of utility installations and increased transmission loss. These degrading effects of harmonic currents become noticeable only when the non-linear loads are a large part of the total load connected to the utility line. With the widespread use of computers and other data processing devices, the contribution of non-linear loads is steadily increasing.

In order to mitigate such problems caused by poor quality of input currents, technology of ac to dc harmonic free rectifiers has become widely available during the last decade. They are often called unity power factor rectifiers or power factor controllers. However, such unity power factor rectifiers have not become popular in commercial data processing devices. Incorporating unity power factor rectifier in every device would lead to additional cost. The power quality problems become noticeable only in places where the loading by the data processing devices is substantial part of the total load. There is not enough incentive for the manufacturers to incorporate unity power factor rectifier with every device. Moreover, consumers usually place higher premium in processor speed, memory size, etc. and not on the supply current waveform quality.

This thesis presents an alternative approach to solve power quality problems in such scenarios. The solution needs to be applied only when the problem becomes severe and causes persistent malfunction of equipment or other equipment connected to the same line. The proposed solution being named as ac to ac Utility Line Current Conditioner (ULCC), is an interface between the utility line and a data processing device such as a computer. The device is used as an add on device only in places where power quality problems demand the additional investment.

ULCC draws sinusoidal current from the supply and regulates the voltage being supplied to the load. It is based on pulse width modulated power converters. They have

been shown to be versatile to perform ac-ac power flow control in various applications [1,2]. The boost ac-ac converter is adapted to perform line current control in a single-phase line, loaded by a rectifier load. An inner average current control loop and an outer voltage control loop are used to perform the active wave shaping function.

Chapter 2 presents a detailed study of the rectifier type of load. Non linear loads such as rectifier loads are studied in detail and measures of harmonic distortion are reviewed. Typical measures of Total Harmonic Distortion (THD) of input current, harmonic currents and current crest factor are provided. Existing solutions to remove harmonic currents are discussed. The concept of the proposed ULCC is introduced.

Chapter 3 presents the power circuit topology of the ULCC. Equivalent circuits and defining equations for different switching intervals are presented. Simplified steady state analytical waveforms are given. During polarity reversal of input line voltage, the zero crossing spike of the input current has been identified as a bottleneck in control and a solution is proposed.

Chapter 4 presents design oriented analysis of the proposed ULCC. From a given set of converter specifications, it presents the equations to select the boost inductor and other circuit elements. Rms and average currents in different branches of the circuit are determined.

Classical circuit averaged model of the boost converter and the control transfer function presented in literature are used to model the average current control loop in Chapter 5. Loop stability and component selection is discussed using Bode plots. A simplified low frequency model of the current loop is introduced.

Chapter 6 presents the dynamic modeling and analysis of the complete system of utility line current conditioner supplying rectifier type of load. The voltage control scheme is discussed in detail. Models of different subsystems are shown separately. Voltage control loop stability is discussed using Bode plots. Closed loop output impedance and input susceptibility are discussed.

A 750 W prototype circuit built to verify the proposed concepts is presented in Chapter 7. Experimental waveforms of input current and other quantities are presented for different type of loads. THD of input current under different load conditions, individual harmonic percentages, line regulation, load regulation and efficiency of the converter are included.

CHAPTER – 2

POWER QUALITY PROBLEMS CAUSED BY RECTIFIER LOADS

Power factor for linear loads is reviewed. Operation of a rectifier type of load is studied in detail. Experimental results of input current waveform are presented. It is shown that input current waveform is rich in harmonics. Crest factor and Total Harmonic Distortion (THD) are defined as a measure of harmonic distortion. Input current harmonics are plotted.

Conventional solutions to improve power quality are discussed. These are: (a) passive filter at the input, (b) ferroresonant transformer, and (c) active power factor correction integrated to the input stage of the rectifier. As a solution to the power quality problems only where it is necessary, the utility line current conditioner is proposed.

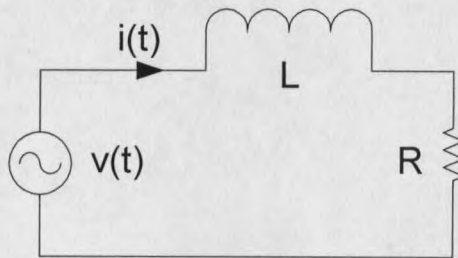
2.1 Linear Loads and Power Factor

Fig. 2.1: Schematic of an ac supply connected to R-L circuit.

Fig. 2.1 presents an ac supply connected to R-L circuit. R is the resistance of the circuit and L is the inductance. At any given instant the value of the supply voltage is $v(t)$ and the current drawn by the load is $i(t)$. The defining equation of the above circuit is

$$L \frac{di(t)}{dt} + R i(t) = v(t) \quad (2.1)$$

Eq. 2.1 represents a linear differential equation. So, the circuit is called a linear circuit and the R-L load is said to be a linear load. If the supply voltage is a sine wave of some given frequency the input current would also be a sine wave of the same frequency. Since the circuit is inductive the current drawn by the load $i(t)$ would lag the input voltage by an angle (say) θ . Typical voltage and current waveforms are presented in Fig. 2.2. This may also be illustrated in the form of a phasor diagram as shown in Fig. 2.3.

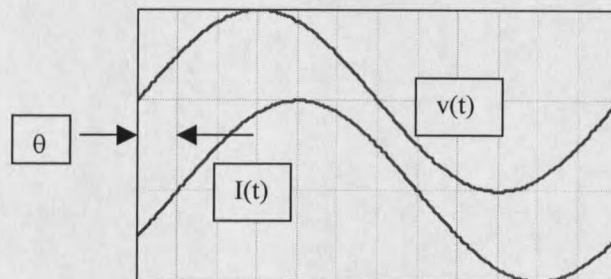


Fig. 2.2: Voltage and current waveforms of the R-L circuit.

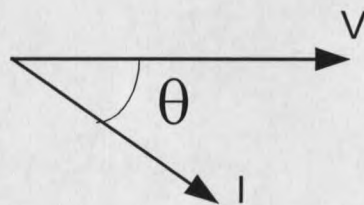


Fig. 2.3: Voltage and current phasor of the R-L circuit.

The average power P drawn by the load per cycle is given by

$$P = \frac{1}{2\pi} \int_0^{2\pi} v(t) i(t) d(\omega t) \quad (2.2)$$

Under such sinusoidal excitation and response conditions as with linear loads, it can be shown that the power P is related to the rms voltage, V_{rms} and the rms current, I_{rms}

$$P = V_{rms} I_{rms} \cos(\theta) \quad (2.3)$$

Power factor of the load may be defined as

$$\text{Power factor} = \frac{P}{V_{rms} I_{rms}} \quad (2.4)$$

Power factor becomes equal to $\cos(\theta)$ for such linear loads. However, when the load is such that it can not be expressed in terms of linear differential equations, then the load is called non linear. In such cases the current waveform will not be a pure sinusoidal waveform. Since the supply voltage is periodic the current would continue to be periodic and we can define the rms quantities of voltage and current. The definition of power factor as in Eq. 2.4 would be valid. But the power factor would not have a simple interpretation as in the case of linear loads. Rectifier loads are examples of such nonlinear loads and the following section presents a study of rectifier loads.

2.2 Rectifier Loads

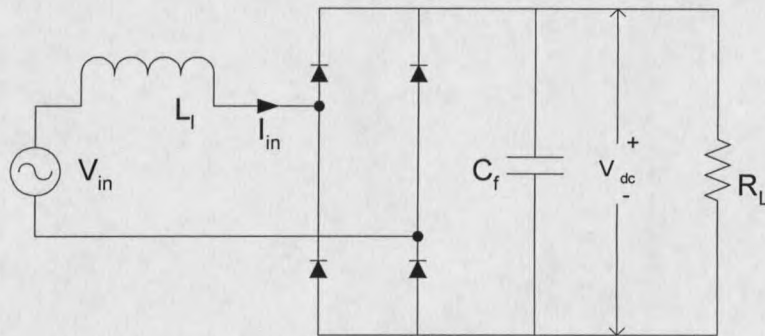


Fig. 2.4: Schematic of a rectifier load connected to ac supply

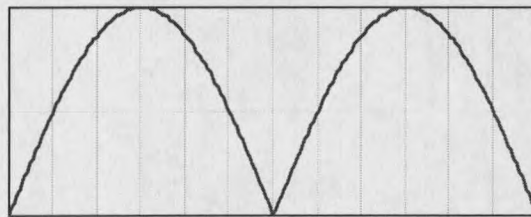


Fig. 2.5: Output voltage waveform of a bridge rectifier in absence of any other circuit at the output.

Fig. 2.4 shows an ac supply connected to a rectifier load. The four diodes connected in the above configuration form a full bridge rectifier. In absence of any other circuit at the output of the rectifier, the output voltage would look like a rectified sine wave as depicted in Fig. 2.5. This waveform, if decomposed into Fourier series, would have a dc component and higher harmonics. A filter is used to remove the harmonics. In Fig. 2.4,

C_f is the filter capacitor. The resistor R_L represents the load. The equivalent inductance of the supply line is shown as L_1 .

The current flows only when the rectifier diodes are forward biased. It is not possible to describe the system operation by linear differential equations as in Eq. 2.1, even if input voltage V_{in} is assumed to be sinusoidal. Fig. 2.6 presents the experimental input current I_{in} of such a rectifier type of load.

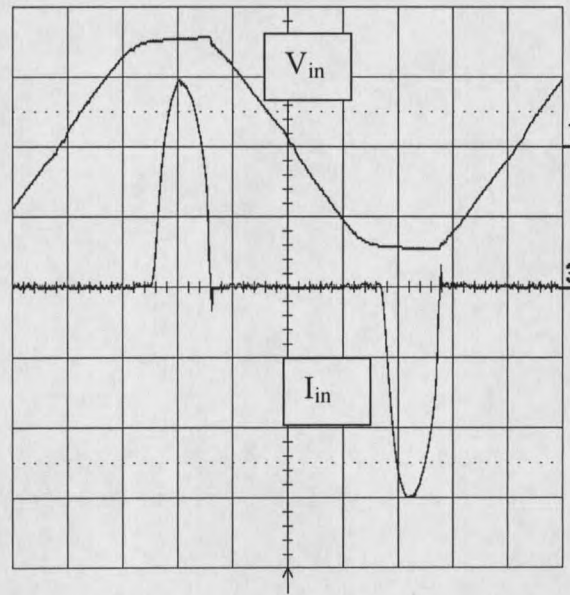


Fig. 2.6: Waveforms of input voltage and input current for a rectifier load.

As seen in Fig. 2.6, there are intervals when the input current is zero. Only when the supply voltage is more than the capacitor voltage, the rectifier diodes are forward biased and the input current builds up. The input current falls when the supply voltage goes below the capacitor voltage. The input current wave shape depends on the inductor L_1

and the loading. If the current waveform were decomposed into different frequency components there would be higher order harmonics along with the fundamental frequency component. It is often said that the current waveform is distorted by the harmonics. Large peak currents increase the rms current more than they contribute to average power. This will result in power factor as defined in Eq. 2.4 to be less than unity. However, following two performance indices better represent the extent of harmonic distortion.

Let the input current peak is denoted by I_p and the rms is denoted by I_{rms} ,

$$\text{Crest factor} = \frac{I_p}{I_{rms}} \quad (2.5)$$

If the current waveform is decomposed into different frequency components and rms value of the fundamental is $I_{rms}(f)$ the Total Harmonic Distortion (THD) as a percentage of fundamental is defined as follows

$$\text{THD} = \frac{\sqrt{I_{rms}^2 - I_{rms}(f)^2}}{I_{rms}(f)} \times 100\% \quad (2.6)$$

For the input current waveform of Fig. 2.6 it is expected that the crest factor and the THD would be large. Both the crest factor and the THD are better measures of harmonic distortion than power factor. As an example, a waveform with a 3% harmonic distortion alone has a power factor of 0.999. A current waveform with 30% total harmonic distortion still has a power factor of 0.95. On the other hand, a current with a 25° phase difference has a power factor of 0.90. Therefore, instead of referring to power

factor, crest factor and THD are often used to evaluate harmonic distortion of a waveform.

2.3 Experimental Results on Rectifier Loads

The circuit shown in Fig. 2.4 was assembled and the experimental results are given in Table 1.

Table - 1 Experimental results on rectifier load

Quantity	Symbol	Value
Circuit parameters/ input quantities		
Load resistor	R_L	140 ohm
Filter capacitor	C_f	2000 μ F
Input voltage	V_{in}	110 V
Test results		
Input power	P_i	158 W
Power factor	pf	0.634
Output dc voltage	V_{dc}	148 V
Input rms current	I_{in}	2.23 A
Input peak current	I_p	5.8 A
Input current crest factor		2.60
Input current THD		117.25%

As anticipated from the waveform, the input current has a large crest factor and a large THD. The individual harmonic currents are plotted in Fig. 2.7.

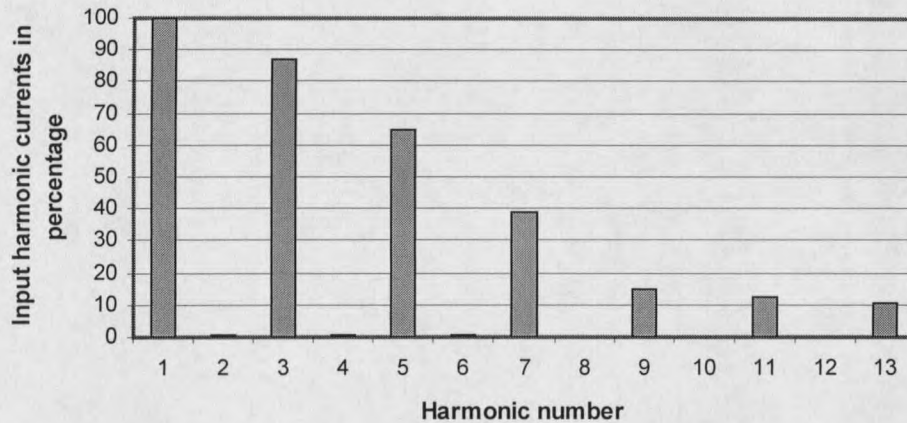


Fig. 2.7: Plot of harmonic currents as percentage of fundamental current.

Input current harmonics not only result in poor power factor but it also affects the other loads connected to the same supply. A typical consequence of high crest factor is that it distorts the voltage waveform and peak voltage gets reduced. High harmonic currents also produce electromagnetic interference. This may affect any sensing or measuring device in the immediate vicinity or connected to the same power line. Over the years, many solutions have been proposed to reduce the input current harmonics. Three such solutions are discussed next.

2.4 Possible Solutions to Input Current Harmonics

2.4 a) Passive Filter at the Input

A passive filter as shown in Fig. 2.8 is connected between the supply line and the rectifier load [3]. It is completely passive and its harmonic performance is good. But it is expensive and bulky. It removes the higher order harmonics but it may have very poor power factor, depending on the loading. This is due to the large series inductor as part of the filter.

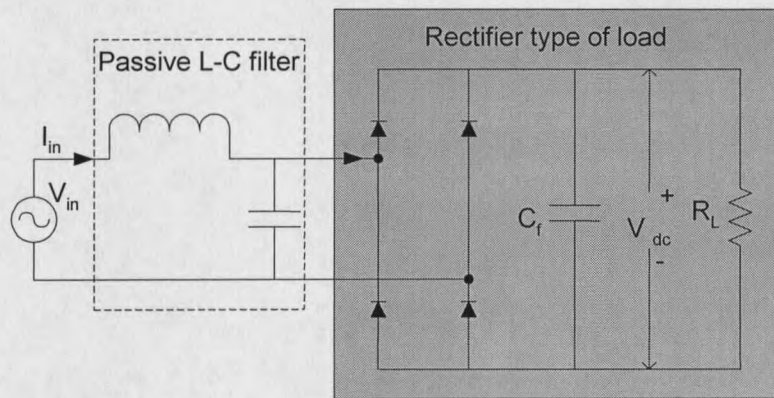


Fig. 2.8: Schematic of a passive filter used to improve harmonic performance.

2.4 b) Ferroresonant Transformer

Ferroresonant transformers are effective in removing higher order harmonics. Most ferroresonant transformers depend on the magnetic saturation and resonant circuits to

achieve this. They also regulate the amplitude of the output voltage. The rms value of the output voltage may change depending on input voltage. Ferroresonant transformers are most useful with rectifier loads in which the dc voltage depends on the amplitude voltage applied to it. Equivalent circuit of a ferroresonant transformer illustrated in Fig. 2.9 shows its basic principle of operation [4]. It differs from a conventional transformer by having a large leakage inductance L_s , a saturating shunt inductance L_p , and a large capacitor in parallel with the load. Fig. 2.10 presents the utilization of a ferroresonant transformer to correct power quality problems.

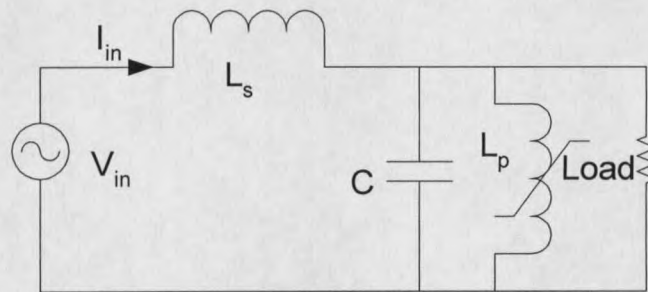


Fig. 2.9: Equivalent circuit of a ferroresonant transformer.

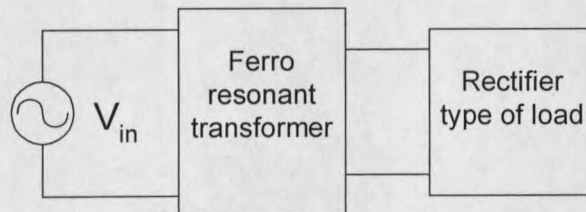


Fig. 2.10: Block diagram of a ferroresonant transformer with rectifier load.

Fig. 2.11 shows the experimental waveforms of a ferroresonant transformer supplying a rectifier load (one personal computer was used). The rectifier input current which is rich in harmonics has been shaped into spectrally cleaner supply line current by the ferroresonant voltage regulator. Because of the presence of large parallel capacitor C in Fig. 2.9 the supply current leads the supply voltage. This is not obvious from Fig. 2.11 because the voltage and current waveforms are taken separately and are at a different time scale. The rectifier input voltage waveform is distorted and it is close to a square wave. However, this does not degrade the performance of the rectifier load, because it is rectified and averaged into dc. Utility line current conditioner proposed later would have similar waveforms of the output voltage.

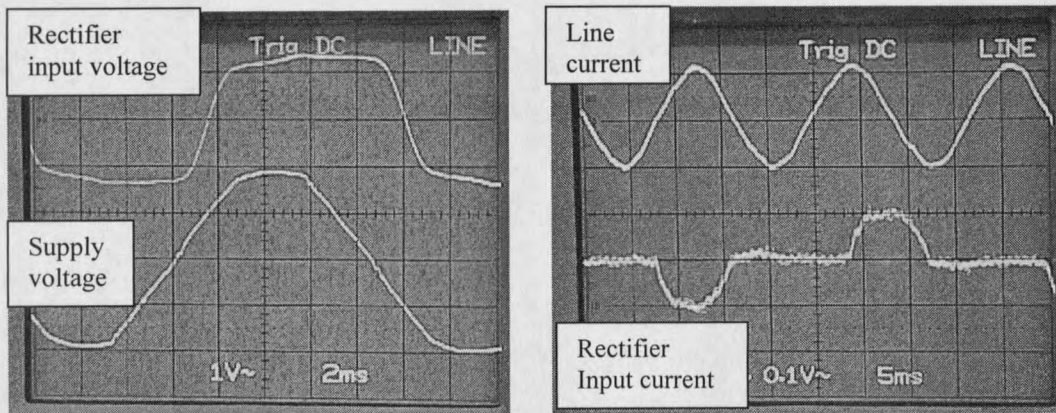


Fig. 2.11: Experimental waveforms of a ferroresonant transformer supplying a rectifier load.

2.4 c) Active Power Factor Correction Integrated to the Input Stage of the Rectifier

Over the last ten years this has become the most common scheme for harmonic free (unity power factor) rectification. Reference [5], [6] & [7] present some of the early works in its development. Fig. 2.12 presents the power circuit. It uses a boost converter topology. Supply line is rectified using a full bridge rectifier. High frequency switches S_1 and S_2 are used to control the boost inductor current I_L . S_1 and S_2 are operated as complementary switches. If S_1 and S_2 are used to denote the logic states of the respective switches then the following relation holds.

$$S_1 = \overline{S_2} \quad (2.7)$$

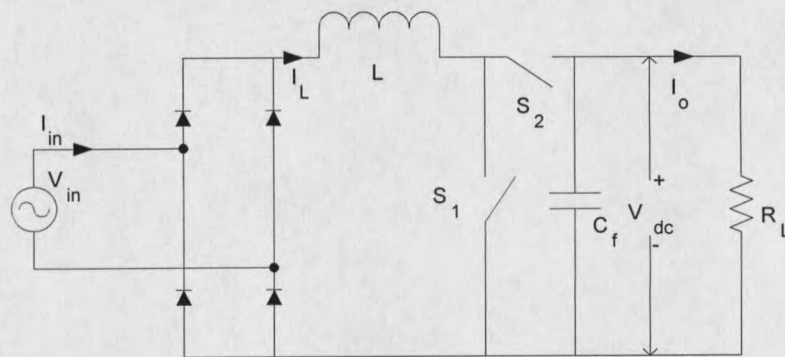


Fig. 2.12: Power circuit of ac to dc unity power factor converter.

Irrespective of the magnitude of supply voltage, when the switch S_1 is closed, the boost inductor L is applied across a positive voltage and current through it increases. After the controlled power switch S_1 is opened, as the complementary switch S_2 is closed, the boost inductor current finds its path through S_2 and charges the filter capacitor C . By controlling the ON-OFF intervals of the controlled switch it is possible to control the

waveform of the current drawn from the supply. This is the basic principle of the circuit operation. The average current mode control scheme is commonly used to control the input current [8]. In averaged current mode control, the inductor current is sensed and compared to the reference current signal to generate a duty ratio command. The current loop variables are continuous and high frequency component is filtered out. However, the filter corner frequency is selected so that it only removes high frequency components and does not interfere with the low frequency components. This in effect, enables the current loop design to use simple state space averaging tools yet gives control over the input current. The disadvantages are the increase in cost for every device and electromagnetic interference generated due to high frequency switching.

2.5 Proposed Ac to Ac Utility Line Current Conditioner

Although the technology of harmonic free unity power factor rectifier is known in the industry for over a decade such rectifiers have not been integrated in commercial data processing devices. Incorporating unity power factor rectifier in every device would lead to additional cost. The power quality problems become severe only in places where the nonlinear loads are a substantial part of the total loading. Moreover, the consumers usually place higher premium in processor speed, memory size, etc. And often the origin of power quality problem goes undetected and if the problem becomes severe isolating transformers or additional filters are installed. In this solution, transformers with delta connected primary windings and star connected four wire

secondary windings are used as isolating transformers. The third harmonic current gets internally circulated and does not enter the primary side. However, this results in overheating of the transformer and it needs to be a high K-factor transformer [9]. This solution is not only very expensive, but it does not address the problem. However, there is no incentive for the manufacturers to incorporate the ac to dc unity power factor rectifier in all data processing devices and not likely to happen in near future.

An alternative solution is proposed herein - ac to ac Utility Line Current Conditioner (ULCC). This device would act as an interface between the supply line and any rectifier load such as a computer. The device may be applied as add on equipment only in places where power quality problems demand the additional investment. The ULCC draws sinusoidal current from the supply and regulates the voltage being supplied to the load. It is based on pulse width modulated converters. They have been shown to be versatile to perform ac-ac power flow control in various applications. The boost ac-ac converter is adapted to perform line current control in a single-phase line, loaded by a rectifier load. The ac line conditioner utilizes an inner average current control loop with an outer voltage control loop to perform the active wave-shaping function. Although this solution would involve additional cost, unlike the unity power factor rectifier, the additional cost need not be added to every data processing device. This solution needs to be applied only when the power quality problem becomes severe and causes persistent malfunction of equipment.

In industry, power converters that provide harmonic free rectification are often called unity power factor converters. Similarly, utility line current conditioner may be called as ac to ac unity power factor converter. These names are commonly used in spite of the fact that power factor is not a good measure of harmonic distortion.

Conclusion

Behavior of linear and non linear loads with respect to input current quality has been studied. Rectifier loads used in most data processing devices have been identified as non linear loads. For such rectifier loads the input current has high crest factor and is rich in harmonics. Several existing solutions to reduce input current harmonics have been discussed. The proposed solution of utility line current conditioner as an add on equipment can be used only in places where power quality problems demand the additional investment. The operation, design and control of the proposed ULCC are presented further in subsequent chapters.

CHAPTER - 3

OPERATION OF UTILITY LINE CURRENT CONDITIONER

Power circuit of the proposed utility line current conditioner is introduced. Operation of the power circuit is explained. Basic design equations are presented. Control strategy based on average current control is proposed. Simplified design equations are solved analytically to produce the steady state waveforms. The chapter concludes with a discussion of zero crossing spike and possible solutions.

3.1 Power Circuit Topology and Principle of Operation

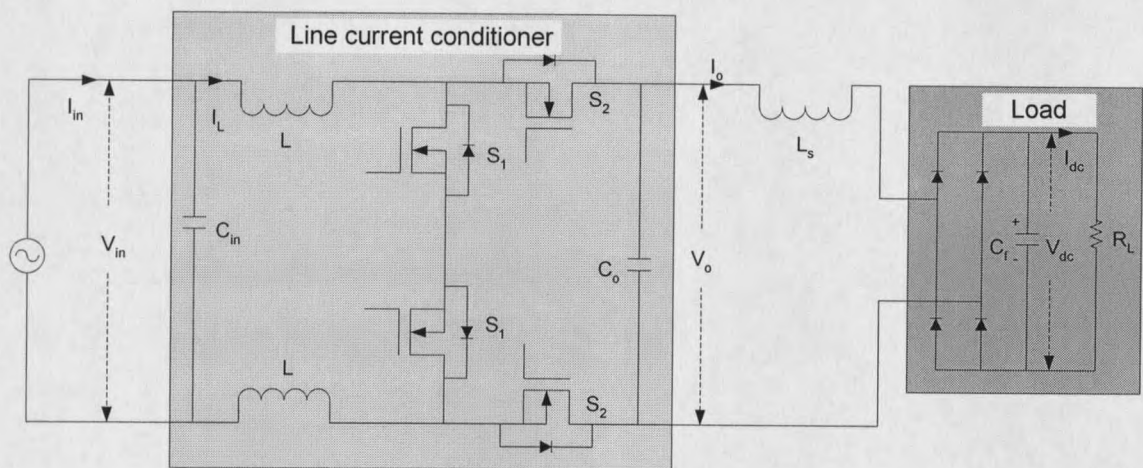


Fig. 3.1: Schematic of the power circuit of utility line current conditioner.

The power circuit of line current conditioner is presented in Fig. 3.1. It shows the line current conditioner, feeding a rectifier type of load. The lightly shaded area on the left is the line current conditioner. Darker shaded area in the right is the data-processing

device, load in this case. The stray inductance L_s accounts for any series inductance present between the output of the utility line current conditioner and the load. The inductors L represent the boost inductor, split into two sections for symmetry. C_f represents the filter capacitor internal to the rectifier. R_L is the equivalent resistance accounting for the loading of the rectifier. C_o and L_s form a second order filter to remove the high frequency component of the switching current. The values of C_o and L_s are selected so that the filter does not attenuate the supply frequency component of the current. The switching ripple in the output current does not affect the performance the utility current conditioner. So, a large switching ripple could be allowed in the output current. Input capacitor C_{in} supplies the high frequency component of the inductor current I_L . Supply frequency component the inductor current is the input current I_{in} . The input current may be controlled to be supply frequency sinusoidal current.

The switches S_1 and S_2 are operated as complementary switches. Their logic states are related by

$$S_2 = \overline{S_1} \quad (3.1)$$

When switches S_1 are closed, the boost inductors appear across the input ac line voltage V_{in} and the inductor current I_L increases in the direction of the input voltage. This current is forced to flow through the load when S_1 switches are opened, and S_2 switches are closed. During this period, the inductor transfers energy to the output capacitor C_o and the inductor current I_L decreases. By suitably controlling the duty ratio of the switches, the inductor current may be maintained at any desired value, as long as the

volt-second balance across the inductor is maintained. The constraint of controlling input current by controlling duty ratio is that the output voltage V_o should be greater in magnitude than the instantaneous value of the input voltage. This constraint is common to boost converter topology. The more stringent constraint is that the output voltage V_o should be of the same sign as the instantaneous value of the input voltage. The consequences of this constraint are discussed in Section 3.7. The relative magnitudes of the input voltage and the output voltage determine the instantaneous duty ratio.

$$V_o(t) = \frac{V_{in}(t)}{1 - D(t)} \quad (3.2)$$

$D(t)$ represents the switching signal, which takes the value of 1 when the switches S_1 are closed and 0 when the switches S_2 are closed. $V_o(t)$ is typically constant over one cycle of the supply frequency, but $V_{in}(t)$ is a sine wave at the supply frequency. So the high frequency averaged value of $D(t)$ is modulated at the supply frequency to maintain the relationship of Eq. 3.2. For simplicity of writing, the notation for time dependence is dropped, but it is to be remembered that all these quantities are modulated at the supply frequency.

The boost converter is operated to control the input current I_{in} to be sinusoidal, proportional to the input voltage so that load to the utility line will appear to be resistive, and hence feature high power factor. Average current control technique is used to achieve this. Average current mode control is most commonly used for a wide variety of converter topologies. In average current mode control, the current controller

does not directly generate the switching signal, instead it produces the average value of the switching signal which is used to generate a pulse width modulated gate drive waveform.

3.2 Control Strategy

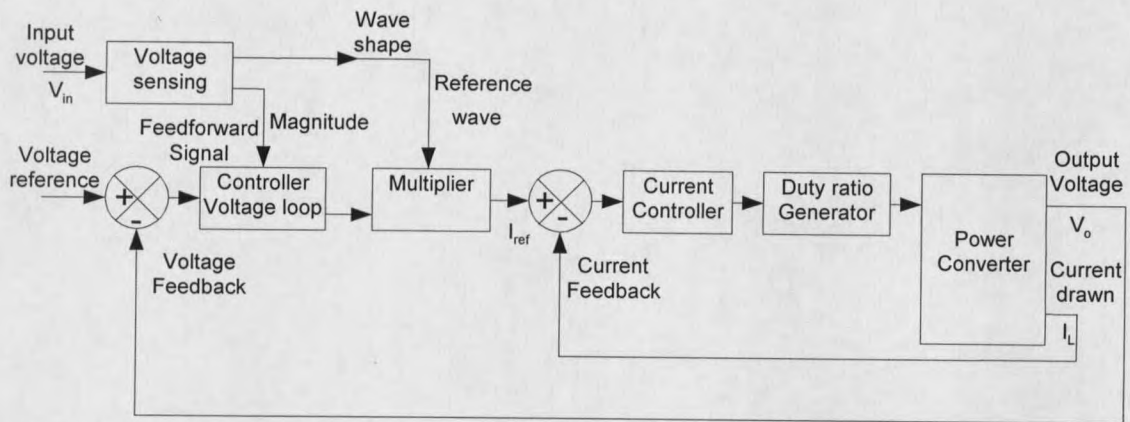


Fig. 3.2: Control circuit block diagram.

A block diagram of the control circuit is presented in Fig. 3.2. The inductor current I_L is sensed and compared to the reference current I_{ref} . The inner current control loop modifies the duty ratio of the boost converter to maintain the current through the boost inductor at the reference value.

The reference current is modulated to follow the input voltage waveform. If the current loop is fast enough, the current drawn by the converter will follow the reference current, and hence the input voltage, thereby providing unity power factor operation. The bandwidth of the current loop should be much larger than the supply frequency 60 Hz,

typically more than 1 kHz. If the current loop gain includes a pole at the zero frequency, this will act as an integrator and eliminate dc errors.

The output voltage feedback controller provides the magnitude command for the inner current control loop. A multiplier is used to generate the instantaneous value of the reference current command from the voltage error amplifier and the input voltage waveform. The voltage loop changes the magnitude of the reference current command depending on the loading and maintains the required output voltage. Voltage loop needs to be slow enough not to modulate the reference current waveform with second and third harmonic being fed back from the measured rectified waveform.

3.3 Defining Equations

S_1 and S_2 are controlled power switches, they can pass bi-directional current and block unidirectional voltage. S_1 and S_2 are complementary switches as in Eq. 3.1. S_1 ON or S_2 ON will result in two different equivalent circuits. The system alternates between these two equivalent circuits at switching frequency (50 kHz).

3.3 a) With S_1 ON S_2 OFF, Rectifier Conducting

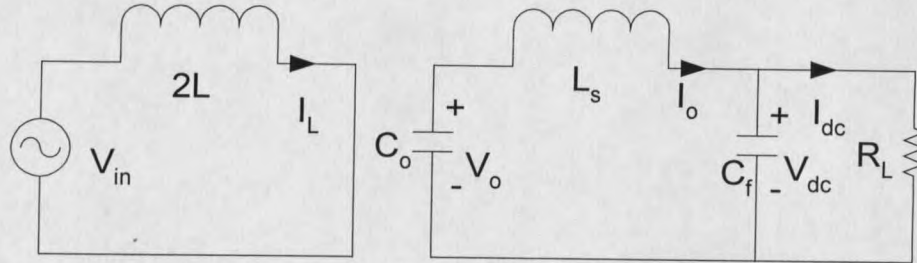


Fig. 3.3: Equivalent circuit with the S_1 ON S_2 OFF.

Equivalent circuit with S_1 ON and rectifier conducting is presented in Fig. 3.3. The switch and the diode drop and other non-idealities are neglected. In this interval the boost inductors are shorted and current through them increases in the direction of V_{in} . Output stage is disconnected from the input stage in this interval.

The defining equations for this interval are given below.

$$\frac{dI_L}{dt} = \frac{V_{in}}{2L} \quad (3.3a)$$

$$\frac{dV_o}{dt} = \frac{-I_o}{C_o} \quad (3.3b)$$

$$\frac{dI_o}{dt} = \frac{V_o - V_{dc}}{L_s} \quad (3.3c)$$

$$\frac{dV_{dc}}{dt} = \frac{I_o - I_{dc}}{C_f} \quad (3.3d)$$

3.3 b) With S_1 OFF S_2 ON, Rectifier Conducting

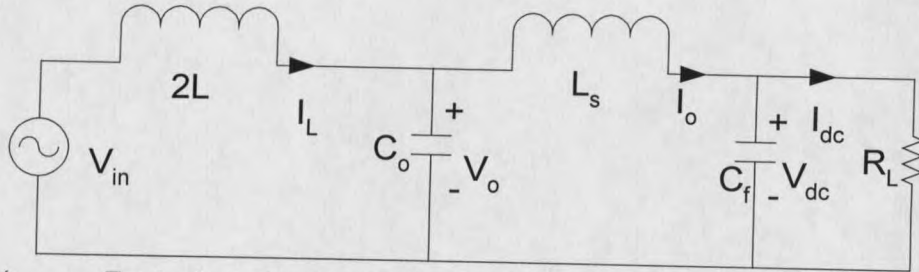


Fig. 3.4: *Equivalent circuit with the S_1 OFF S_2 ON.*

The equivalent circuit with S_2 ON and rectifier conducting is presented in Fig. 3.4. In this interval the boost inductors are charging the capacitor C_o .

The defining equations for this interval are given below.

$$\frac{dI_L}{dt} = \frac{V_{in} - V_o}{2L} \quad (3.4a)$$

$$\frac{dV_o}{dt} = \frac{I_L - I_o}{C_o} \quad (3.4b)$$

$$\frac{dI_o}{dt} = \frac{V_o - V_{dc}}{L_s} \quad (3.4c)$$

$$\frac{dV_{dc}}{dt} = \frac{I_o - I_{dc}}{C_f} \quad (3.4d)$$

3.4 Circuit Averaging and Steady State Solutions

The above equations describe the overall system. Assuming the switching frequency is much larger than the circuit time constants, the switching variable is replaced with a continuous variable D [10]. This is the duty ratio D as in Eq. 3.2. Time average of the switching variable is the duty ratio D . This is also called circuit averaging technique. Reference [11] provides a comprehensive treatment of the subject.

$$\frac{dI_L}{dt} = \frac{V_{in} - (1-D)V_o}{2L} \quad (3.5a)$$

$$\frac{dV_o}{dt} = \frac{I_L(1-D) - I_o}{C_o} \quad (3.5b)$$

$$\frac{dI_o}{dt} = \frac{V_o - V_{dc}}{L_s} \quad (3.5c)$$

$$\frac{dV_{dc}}{dt} = \frac{I_o - I_{dc}}{C_f} \quad (3.5d)$$

Neglecting the effects of the small intervals when the bridge rectifier is not conducting the steady state solutions could be found by equating these state variable derivatives to zero. Considering a small values of filter components L_s and C_o ,

$$V_o = \frac{V_{in}}{1-D} \quad (3.6a)$$

$$I_L = \frac{I_o}{1-D} \quad (3.6b)$$

$$V_o(\text{peak}) = V_{dc} \quad (3.6c)$$

$$I_o(\text{average}) = I_{dc} \quad (3.6d)$$

3.5 Simplified Equivalent Circuit and Steady State Solutions

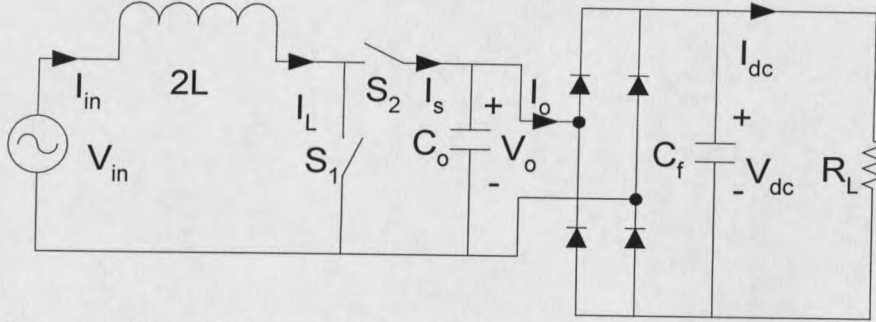


Fig. 3.5: Simplified equivalent circuit.

Fig. 3.5 presents the simplified equivalent circuit. Input filter capacitor and output stray inductor are ignored.

If V_{in} is a sine wave of frequency ω ,

$$V_{in}(t) = V_m \sin(\omega t) \quad (3.7)$$

and the boost ratio k is defined as,

$$k = \frac{V_m}{V_{dc}} \quad (3.8)$$

Then the average duty ratio $D(t)$ could be expressed as,

$$D(t) = \frac{V_o(t) - V_{in}(t)}{V_o(t)} \quad (3.9)$$

$$D(t) = 1 - k|\sin(\omega t)| \quad (3.10)$$

And the average switch current $I_s(t)$ is given by,

$$\text{Average } I_s(t) = I_{in}(t) \times \{1 - D(t)\} \quad (3.11)$$

$$\text{Average } I_s(t) = I_m k \sin(\omega t) |\sin(\omega t)| \quad (3.12)$$

The simplified waveforms are presented in Fig. 3.6. The time axis is indicated as normalized time, this means one complete supply frequency cycle is shown as 360° . If the current control loop of the boost stage works properly, I_{in} could be assumed to be a sine wave in phase with V_{in} as shown in Fig. 3.6. The third waveform is the average duty ratio $D(t)$ as described by Eq. 3.10. Next is average value of the switched current $I_s(t)$, this has the square of a sine wave shape as described in Eq. 3.12. Next is $V_o(t)$ having a peak equal to V_{dc} , when the rectifier is conducting this will be equal to V_{dc} . For simplicity V_{dc} is assumed to be constant here. For the first $1/6$ cycle time, the output voltage V_o changes sign and rectifier is not conducting. This mode starts whenever V_{in} changes polarity. During this time $I_o(t) = 0$. Input current charges the capacitor in the opposite polarity. This mode stops when $|V_o|$ becomes equal to V_{dc} . $I_o(t)$ becomes equal to $I_s(t)$ when the rectifier conducts.

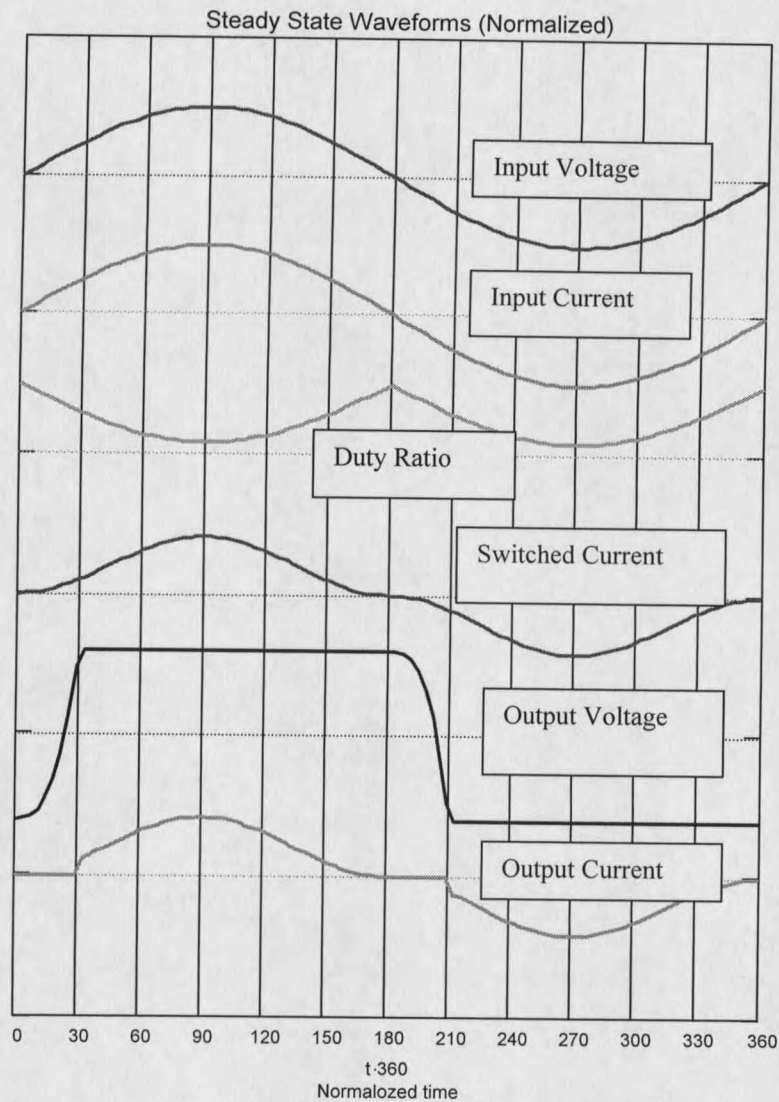


Fig. 3.6: Simplified steady state waveforms (one complete cycle is 360°).

These waveforms demonstrate the operation of the proposed circuit. These waveforms are solutions to the simplified equations developed herein. In Chapter 7 the experimental waveforms are presented that verify these results.

3.6 Equivalent Circuit during Zero Crossing

From the discussion of Section 3.4, when the input voltage V_{in} and output voltage V_o are of opposite polarity then Eq. 3.6a does not have a viable steady state solution. This is because D is limited between zero and one. So, during this interval the circuit loses control over the inductor current. This condition occurs whenever the input voltage changes polarity. When the input voltage changes polarity the output voltage also will change polarity and the bridge rectifier will not conduct until the capacitor C_o gets charged to V_{dc} of the opposite polarity. This is seen in Fig. 3.6 between 180° and 210° . However, since the control circuit has lost control over inductor current there will be resonance between the boost inductors and the output capacitor C_o and this will decide the input current. This will result in large current spike of the inductor current I_L and I_{in} .

The equivalent circuit from the output side during zero crossing resonance is presented in Fig. 3.7a and is simplified as shown in Fig 3.7b. The rectifiers are reverse biased so the load is disconnected. During zero crossing D is very close to unity, this makes the effective inductance very small. This results in a large current spike as will be discussed further.

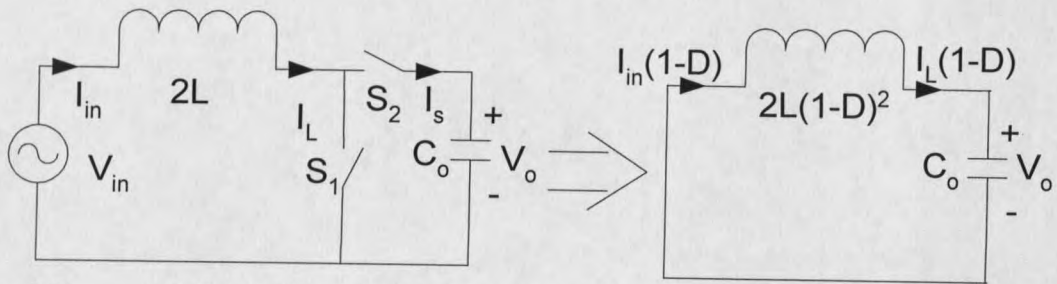


Fig. 3.7: a) Equivalent circuit at zero crossing. b) Simplified circuit.

3.7 Zero Crossing Spikes in Input Current

Fig. 3.7b is an L-C resonant circuit and at the end of the resonance the capacitor will have its charge reversed. In Fig. 3.8 the resonance interval is studied and it is observed that the capacitor voltage changes polarity at the end of the resonance interval when the control circuit resumes its control over the inductor current. The time scale of Fig. 3.8 is small compared to the total cycle time. The large current spike will distort the input current waveform as shown in Fig. 3.9.

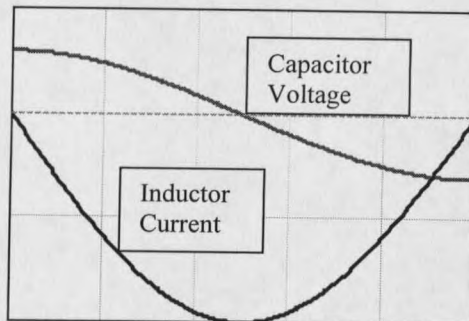


Fig. 3.8: Capacitor voltage and inductor current during resonance.

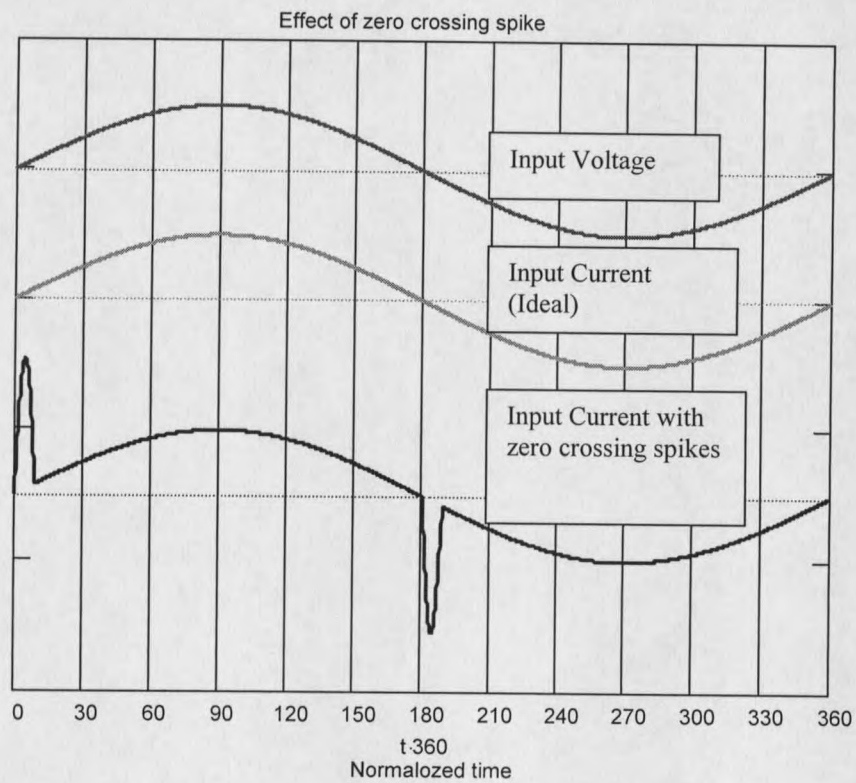


Fig. 3.9: Zero crossing spikes in input current (one complete cycle is 360°).

3.8 Proposed Solution to Zero Crossing Spikes

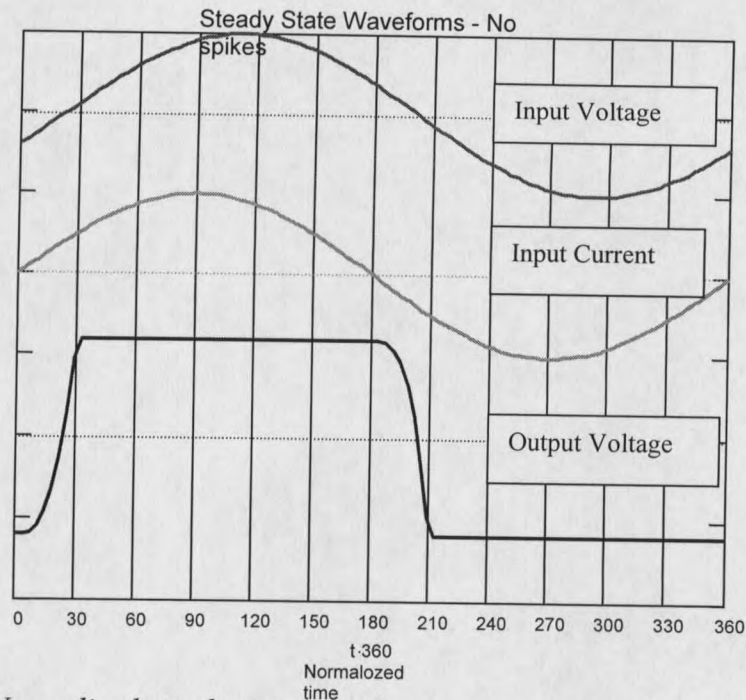


Fig. 3.10: Normalized steady state waveforms – no zero crossing spike.

In the simplified equivalent circuit of Fig. 3.5, direction of current can be controlled to any positive or negative values independent of input voltage polarity as long as duty ratio has control over input current. If a phase lead between the input voltage and the reference current signal is introduced, then the input current will become negative before the input voltage becomes negative. This negative current can change the polarity of the output capacitor. This is illustrated in Fig. 3.10. If the amount of phase lead is such that the input voltage and the capacitor voltage changes polarity at the same time, there will be no spikes in the input current as shown in Fig. 3.10.

The required phase difference will depend on the loading and the circuit parameters. This phase difference needs to be accurate over all loads to make zero crossing spikes disappear. It is possible to design simple analogue circuits, which can be tuned to operate under a given set of operating conditions. It is desirable to have digital controller and a dynamic phase lead adjustment algorithm, which adjusts the phase lead in real time to eliminate the spikes for better performance.

Conclusion

The power circuit operation for the proposed utility line current conditioner has been explained in this chapter. The defining equations have been developed from the equivalent circuits. The defining equations are solved analytically and simplified steady state waveforms have been presented. These will enable the design of the power circuit components of the prototype, which is presented in the next chapter.

CHAPTER – 4

DESIGN ORIENTED ANALYSIS

This chapter presents design oriented analysis of the ULCC. With the help of the steady state equations derived in the last chapter, design equations are presented here. Selection of the boost inductor and the switch average and rms currents are presented. The ideal power switches are realized with the available power MOSFETs. A complete circuit diagram of the power circuit is given.

4.1 Specifications of the Prototype Converter

Table 2 presents the specifications of the prototype converter built to verify the concepts. The rectified dc voltage, V_{dc} , has to be higher than the peak of the maximum input voltage. V_{dc} is chosen to be 200 V to provide a reasonable amount of margin under overvoltage conditions. Selection of the boost inductor and the power semiconductor switches are explained for the following specifications.

Table - 2 The specifications of the prototype converter

Quantity	Symbol	Value
Output power	P_o	750 W
Input voltage	V_{in}	100-130 V
Dc bus voltage	V_{dc}	200 V
Switching frequency		50 kHz
Supply frequency		60 Hz

4.2 Boost Inductor Selection

When supply voltage is at its minimum, the amount of boosting necessary is maximum and the current stress on the inductor is maximum. Thus, the minimum rms supply voltage is the condition used for developing the inductor selection methodology.

$$V_{in} = V_{in}(\min) = 100V \quad (4.1)$$

The input power is determined assuming some efficiency (say) $\eta = 90\%$

$$P_{in} = P_o / \eta \quad (4.2)$$

The rms input current may be determined as

$$I_{in} = P_{in} / V_{in} \quad (4.3)$$

And the peak input current is given by

$$I_{pk} = \sqrt{2} I_{in} \quad (4.4)$$

The duty ratio can be determined from the input and output voltages. The duty ratio D at the peak of the input voltage is

$$D = \frac{V_{dc} - \sqrt{2} V_{in}}{V_{dc}} \quad (4.5)$$

At the peak of the input voltage a certain ripple current, $\Delta I =$ (say) 20% is assumed.

The boost inductor may be calculated from the ripple current specifications as [11].

$$L = \frac{1}{2} \frac{\sqrt{2} V_{in} \times D}{f_s \times \Delta I} \quad (4.6)$$

The boost inductor selection is presented in detail. Selection of other power circuit components is presented in Appendix A as a Microsoft Excel® design sheet. Appendix B presents the Mathcad® sheet for inductor design. The formulas of determining the worst case rms and average currents in the switches S_1 and S_2 are presented below.

4.3 Derivation of Power Switch Currents

4.3 a) Average and Rms Current through S_1

Half cycle average current of the switch S_1 is given by

$$I_{s1}(av) = \frac{1}{\pi} \int_0^{\pi} I_{s1}(t) dt \quad (4.7)$$

where $I_{s1}(t)$ is the instantaneous current through S_1 . $I_{s1}(t)$ could be expressed as

$$I_{s1}(t) = I_{in}(t) D(t) \quad (4.8)$$

Combining the above two equations and substituting $D(t)$ from Eq. 3.9c,

$$I_{s1}(av) = \frac{1}{\pi} \int_0^{\pi} I_m \sin(\omega t) \{1 - k \sin(\omega t)\} d(\omega t) \quad (4.9)$$

where I_m is the peak of the input current and the boost ratio k is defined by

$$k = \frac{\sqrt{2} V_{in}}{V_o} \quad (4.10)$$

Performing the integral in Eq. 4.9 the average switch current may be obtained to be

$$I_{s1}(av) = I_m \left\{ \frac{2}{\pi} - \frac{k}{2} \right\} \quad (4.11)$$

This may be expressed in terms of input average current $I_{in}(av)$ as

$$I_s(av) = I_{in}(av) \left(1 - k \frac{\pi}{4} \right) \quad (4.12)$$

It is straightforward to modify Eq. 4.9 to get the rms current $I_{s1}(rms)$.

$$I_{s1}(rms)^2 = \frac{1}{\pi} \int_0^{\pi} \{I_m \sin(\omega t)\}^2 \{1 - k \sin(\omega t)\} d(\omega t) \quad (4.13)$$

Evaluation of the integral results in

$$I_{s1}(rms) = I_m \sqrt{\frac{1}{2} - \frac{4k}{3\pi}} \quad (4.14)$$

This result is expressed in terms of input rms current.

$$I_{s1}(rms) = I_{in}(rms) \sqrt{1 - k \frac{8}{3\pi}} \quad (4.15)$$

4.3 b) Average and Rms Current through S_2

The average current through S_2 , $I_{s2}(av)$ could be calculated following the same procedure as above and modifying Eq. 4.8 and Eq. 4.9. However, the average the

current through the capacitors C_o or C_f has to be zero in steady state. This leads to direct answer for $I_{s2(av)}$

$$I_{s2(av)} = I_o \quad (4.16)$$

Eq. 4.8 is modified for switch S2 as

$$I_{s2}(t) = I_{in}(t) \{1 - D(t)\} \quad (4.17)$$

The expression for rms current is given by

$$I_{s2}(rms)^2 = \frac{1}{\pi} \int_0^{\pi} \{I_m \sin(\omega t)\}^2 \{k \sin(\omega t)\} d(\omega t) \quad (4.18)$$

Evaluation of the integral and simplification results in

$$I_s(rms) = I_{in}(rms) \sqrt{k \frac{8}{3\pi}} \quad (4.19)$$

4.4 Determination of Blocking Voltages of the Power Switches

With reference to the ideal power circuit as shown Fig. 3.1, S_1 blocks when the switch S_2 conducts. So the blocking voltage for switch S_1 , $V_1(OFF)$ is the output voltage V_o . Peak value of V_o could be considered as approximately equal to V_{dc} if the rectifier diode drops are neglected.

$$V_1(\text{OFF}) = V_{dc}(\text{peak}) \quad (4.20)$$

Similarly blocking voltage for switch S_2 , $V_2(\text{OFF})$ is approximately equal to V_{dc} .

$$V_2(\text{OFF}) = V_{dc}(\text{peak}) \quad (4.21)$$

Equations 4.20 and 4.21 are valid only in ideal cases. In practice the switches are not ideal, so the dead time considerations and the voltage spike due to stray inductance would necessitate the selection of power switches of much higher voltage rating. The necessity of the dead time when both the switches S_1 and S_2 are OFF is explained in the next section. It is also shown that a turn OFF snubber is necessary to provide an alternate path for the inductor current during the dead time.

4.5 Semiconductor Switch Selection and other Practical Considerations

Each power switch in Fig. 3.1 needs to block unidirectional voltage and pass bi-directional current. The relevant power switches for this application are IGBT and MOSFET. For low power applications MOSFET is recommended and for high power applications use of IGBT is recommended. For the specifications given, the above power MOSFET could be used. To select the MOSFET one needs to know the peak rms current stress and the voltage stress. Equations (4.12-4.19) present the formulas for calculating average and the rms currents.

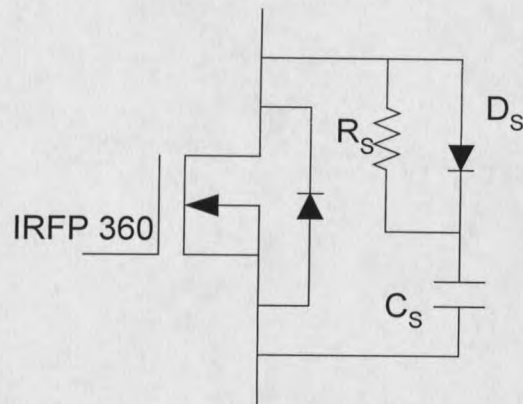


Fig. 4.1: Schematic of the snubber circuit for each mosfet.

Peak voltage stress considerations are explained above. In this application the MOSFET IRFP360 is selected. It has a blocking voltage rating of 400 V and continuous drain current of 23 A.

Eq. 3.1 shows that the switches S_1 and S_2 are complementary switches. Since both the switches can not be ON simultaneously (This would create a short circuit across the output capacitor C_o), a dead time is typically provided, when both S_1 and S_2 are OFF. During this time the boost inductor current flows through the snubber capacitor C_s . The snubber circuit is shown in Fig. 4.1. This is a typical turn OFF Snubber. Capacitor C_s is designed such that the inductor current charges this capacitor to the allowable voltage during the dead time [11]. The resistor R_s limits the turn ON current.

The complete power circuit is presented in Fig. 4.2. The switches S_1 and S_2 are realized with power MOSFET and snubber circuits as described in Fig. 4.1 are added.

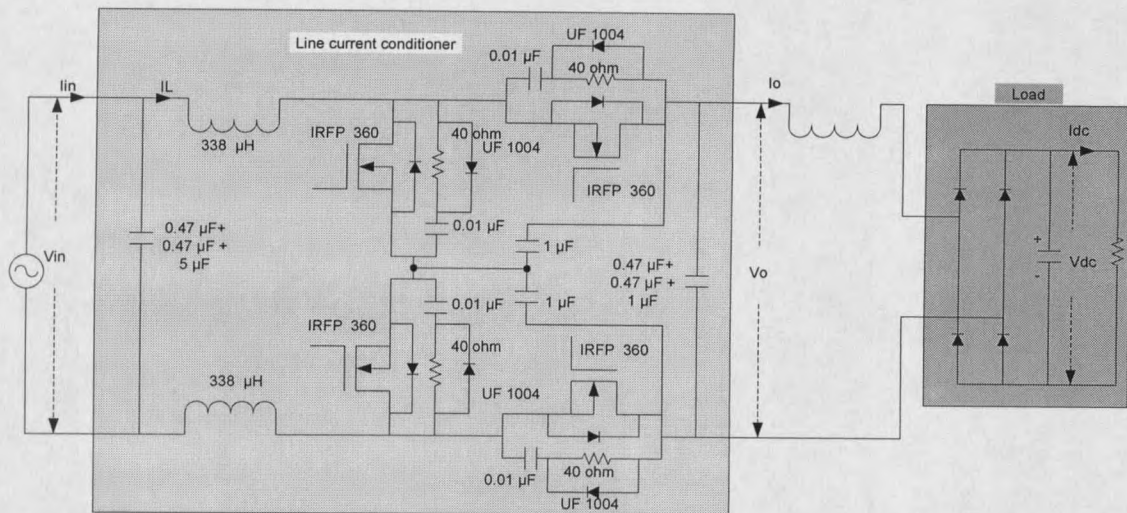


Fig. 4.2: Schematic diagram of complete power circuit.

Conclusion

This chapter concludes the steady state analysis and design. The basic design equations for the boost inductor and equations for determining the rms and average currents through the switches have been provided. The various appendices referred to in this section are useful for developing any similar converter. The next chapter presents the high frequency modeling and dynamic analysis of the converter.

CHAPTER - 5

HIGH FREQUENCY SMALL SIGNAL MODELING AND ANALYSIS

This chapter introduces to the high frequency small signal model of the proposed supply line current conditioner. It is seen that supply voltage is almost constant over a switching cycle so that it could be considered a dc voltage. The model of the averaged current controller is used and suitably modified to represent the circuit used in the implementation of the utility line current conditioner. From the block diagram, the overall loop gain may be computed and used for small signal stability analysis. By using the Bode plot technique, the parameters for the controller may be chosen.

5.1 Model of the Basic Boost Converter

The circuit illustrated in Fig. 3.6 operates from the supply voltage. The switching frequency is 50 kHz whereas the supply frequency is 60 Hz., so that over one or even a few switching cycles the input voltage can be considered as constant and so dc. With these considerations the simplified circuit given in Fig. 3.5 reduces to a simple boost converter as drawn in Fig. 5.1.

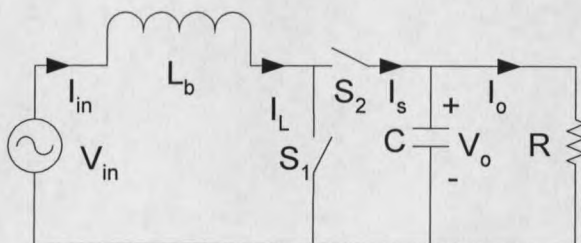


Fig. 5.1: Schematic of the boost converter.

If switching cycle time is T_s , for $0 < t < DT_s$ the switch S1 ON & S2 OFF, for $DT_s < t < T_s$ the switch S1 OFF & S2 ON.

The boost converter is a nonlinear system with respect to the control variable, namely the duty ratio. But in each of the switching intervals DT_s and $(1-D)T_s$ the equivalent circuits are linear. To obtain the equivalent description for the entire switching cycle the defining equations are averaged. From this, it is possible to derive transfer functions for small perturbations around the operating point. The averaging technique and small signal dynamic analysis for switching converters are widely presented in literature. Reference [11] presents a very systematic description of modeling dc to dc power converters. Reference [12] and [13] also provide additional information.

The converter inputs and outputs are shown in Fig. 5.2. V_{in} , I_o and D are inputs and V_o and I_{in} are considered as outputs. Note that I_{in} is considered as an output because the loading and the circuit and its dynamics decide the input current.

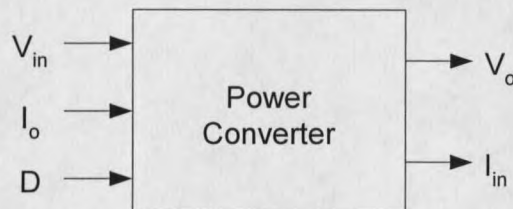


Fig. 5.2: *Input and output variables of the boost converter.*

For small signal analysis we consider small perturbations around the operating point. The small signals are denoted by lower case letters as shown in Fig. 5.3. The operating point is denoted by the corresponding symbols in capital letter.

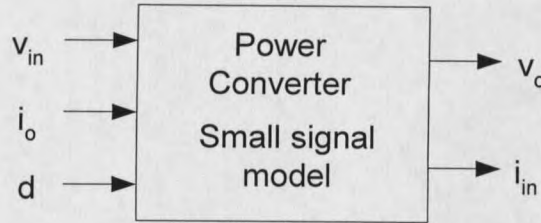


Fig. 5.3: Small signal inputs and outputs of the boost converter.

From Reference [11], the control transfer function of the inductor current may be determined to be,

$$G_b(s) = \frac{i_{in}(s)}{d(s)} = \frac{V_{dc}}{R(1-D)^2} \frac{2 + sCR}{1 + s\frac{L_e}{R} + s^2 L_e C} \quad (5.1)$$

where the parameter L_e is given by

$$L_e = \frac{L_b}{(1-D)^2} \quad (5.2)$$

5.2 Average Current Mode Control

Average current mode control is common in different types of switching power converters and is widely discussed in literature. Reference [8] presents a good summary of the subject. Fig. 5.4 illustrates a common implementation of the scheme. The current controller gives an average signal proportional to the difference between the actual current and the reference current. The current is sensed by measuring the voltage drop across a current sense resistor. Output of the current controller is compared to the saw-tooth wave to generate the duty ratio signal.

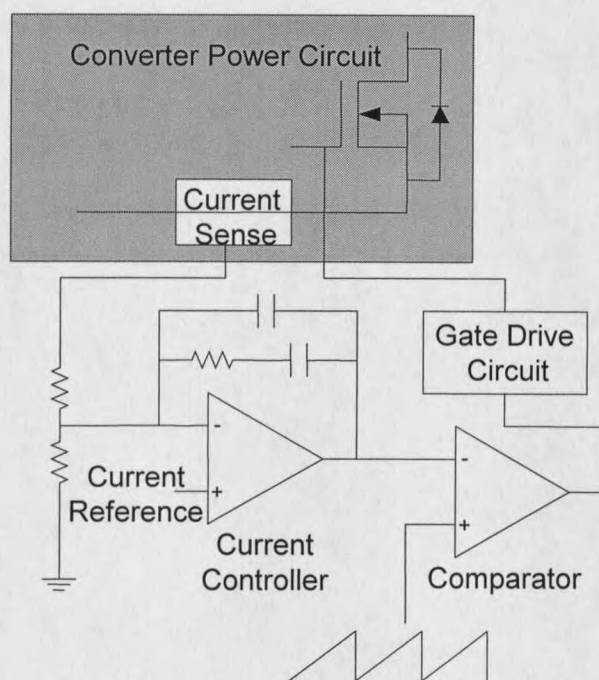


Fig. 5.4: A general scheme of average current mode control.

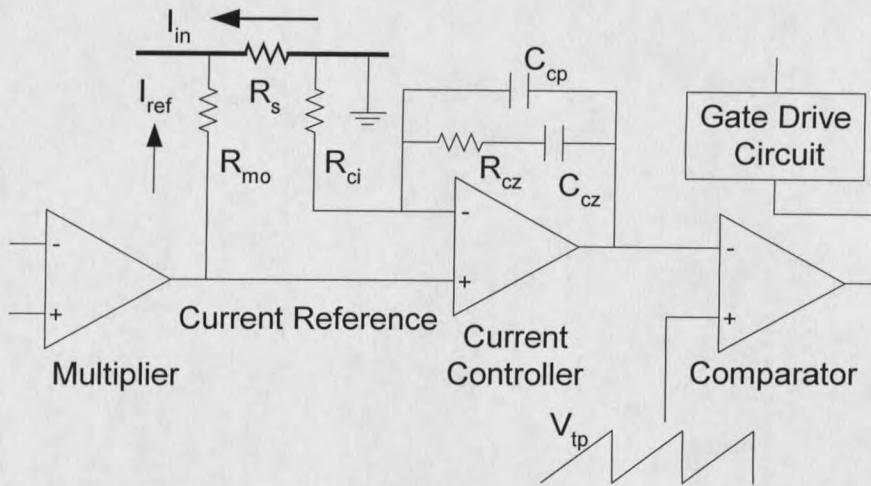


Fig. 5.5: Current controller using UC3854A.

Such a controller may be implemented using the IC UC3854A. The schematic of the current loop of the control circuit is shown in Fig. 5.5. Output of the voltage loop is a multiplier, which gives the reference current to the current loop. The multiplier output is a current source and this current flows through R_{mo} . The load current flows through the sense resistor R_s and generates a negative voltage, which is balanced by the voltage drop in R_{mo} . The current controller amplifier operates with both the inputs near zero voltage. The PI controller produces the signal used to generate the duty ratio.

5.3 Modeling the Current Loop

The current loop consists of the converter, the controller, and the feedback path. The proposed model of the current loop is presented in Fig. 5.6. G_b is the converter transfer function as given in Eq. 5.1.

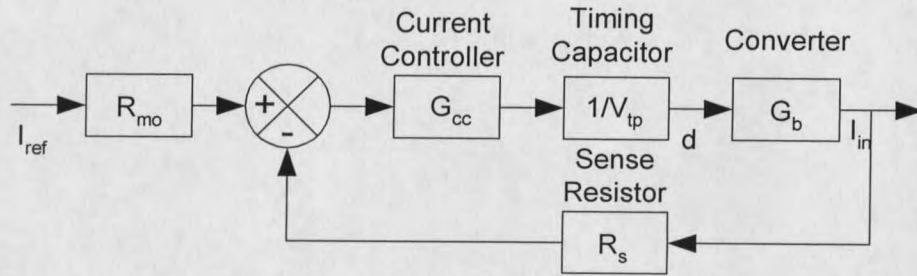


Fig. 5.6: The block diagram of the current loop.

G_{cc} is the transfer function of the PI controller and is given by Eq. 5.3. V_{tp} is the voltage to which the timing capacitor gets charged.

$$G_{cc}(s) = \frac{1 + \frac{s}{\omega_{cz}}}{\frac{s}{\omega_{cpz}} \left(1 + \frac{s}{\omega_{cp}} \right)} \quad (5.3)$$

Where ω_{cz} , ω_{cp} and ω_{cpz} are given by

$$\omega_{cz} = \frac{1}{R_{cz} C_{cz}} \quad (5.4)$$

$$\omega_{cp} = \frac{1}{R_{cz} \frac{C_{cz} C_{cp}}{C_{cz} + C_{cp}}} \quad (5.5)$$

$$\omega_{cpz} = \frac{1}{R_{cz} (C_{cz} + C_{cp})} \quad (5.6)$$

5.4 Loop Stability and Component Selection

With reference to the block diagram of Fig. 5.6 the loop gain function is given by

$$G_{\text{loop}}(s) = G_{\text{cc}}(s) \frac{1}{V_{\text{tp}}} G_{\text{b}}(s) R_{\text{s}} \quad (5.7)$$

It is possible to design the components of the current loop using the loop gain. Bode plot technique has been used for this. Appendix C provides the Mathcad® code of the current loop design. Reference [15] provides a detailed step by step discussion for designing ac to dc unity power factor rectifier. For ac to ac application, this approach needs to be modified suitably and the component values could be fine-tuned by using Bode plot technique.

In this application the reference current is modulated at the supply frequency. The current loop response should be fast enough so that the input current tracks the reference current with little error. This requires that the low frequency gain of the current loop should be large and the loop should have a large bandwidth. It should be noted that the operating duty ratio is modulated at double the supply frequency. The loop transfer function is dependent on the operating duty ratio. The stability and performance conditions need to be satisfied ideally for all duty ratios. The following Bode plots are for a duty ratio of 0.8 and 0.2. The steady state gain differs with duty ratio but the stability performances are not affected.

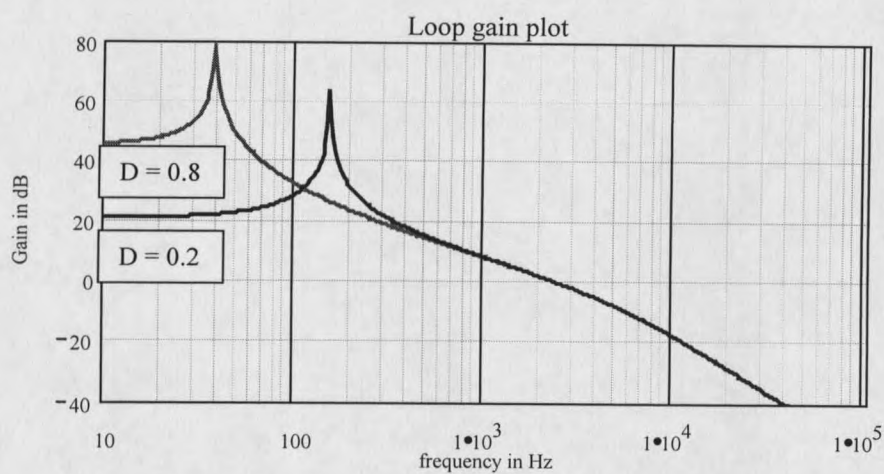


Fig. 5.7: Gain plot of the current loop.

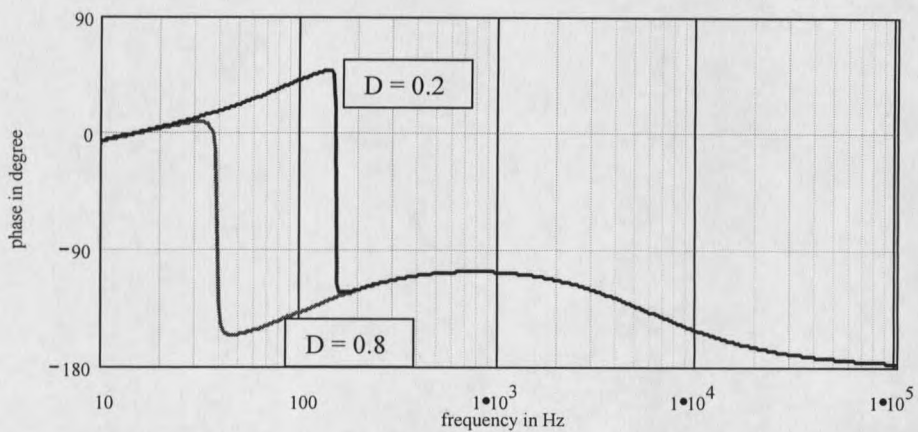


Fig. 5.8: Phase plot of the current loop.

With reference to Fig. 5.5, the above plots are for the following components.

Table – 3 Current controller component values

Symbol	Value
$R_{mo} = R_{ci}$	10 k
R_{cz}	33 k
C_{cz}	0.047 μ F
C_{cp}	880 pF

As seen from the plots that the bandwidth is 2 kHz and the steady low frequency gain is around 46 dB and the phase margin is above 45°. But for duty ratio of 0.8 the phase plot goes close to 180° at a lesser frequency (40 Hz) before the gain cross over frequency. So at that frequency phase stability margin is not very good. However, for a lower duty ratio (0.2) the effect of this phenomenon is less severe.

5.5 Simplified Low Frequency Model of the Current Loop

The block diagram of the current loop could be reduced to find the transfer function between the input current and the reference current. As seen from the Bode plots, the bandwidth of the current loop is around 2 kHz. The dynamics of the whole loop could be neglected and the loop could be considered as a simple gain, for frequencies order of magnitude less than the bandwidth. This is verified by studying the transfer function.

$$G_{cl} = \frac{I_{in}}{I_{ref}} \quad (5.8)$$

With reference to Fig. 5.6 and Eq. 5.7, the transfer function is given by

$$G_{cl}(s) = R_{mo} \frac{G_{cc}(s) \frac{1}{V_{tp}} G_b(s)}{1 + G_{cc}(s) \frac{1}{V_{tp}} G_b(s) R_s} \quad (5.9)$$

Fig. 5.9 presents the gain plot of the overall transfer function of the current loop.

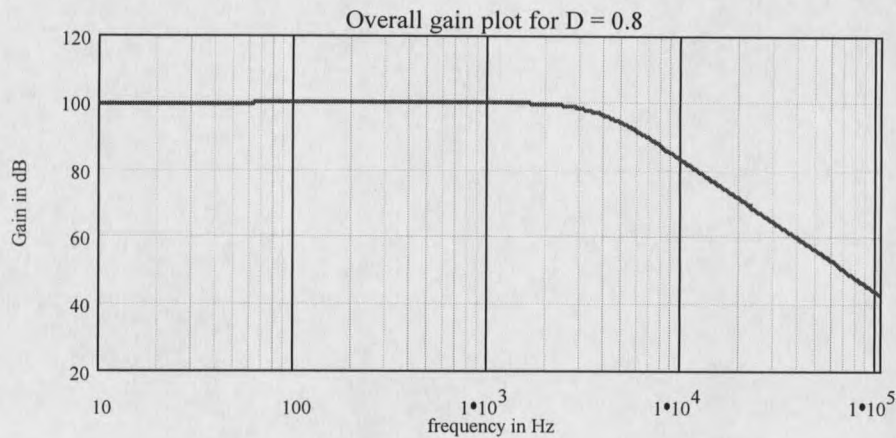


Fig. 5.9: Overall gain plot of the current loop.

Fig. 5.10 presents the corresponding phase plot. As seen from the plots that up to the bandwidth frequency (2 kHz) the overall transfer function could be considered as a simple gain as shown in Fig. 5.11

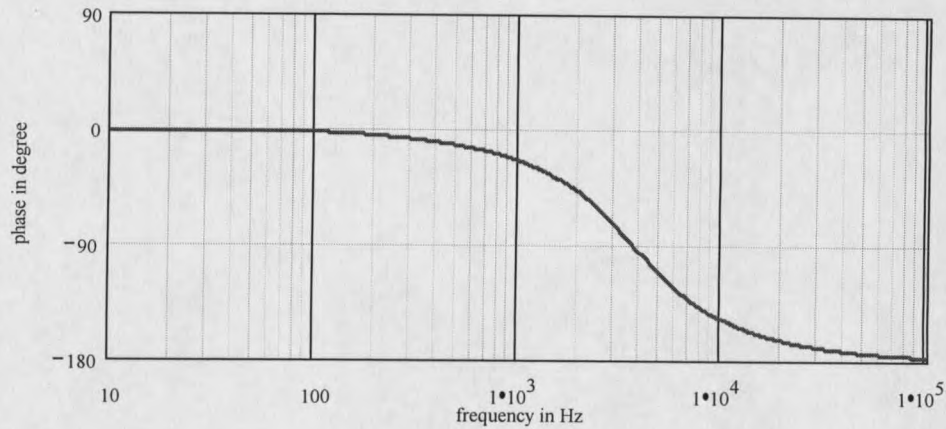


Fig. 5.10: Phase plot of the overall transfer function.

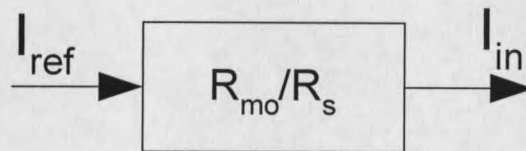


Fig. 5.11: Simplified block diagram of the current loop.

Conclusion

Simplification of the actual circuit to that of a simple boost converter for high frequency analysis has been illustrated. The general scheme of average current mode control has been briefed. Using the small signal model of a boost converter a model of the current loop has been illustrated. Dynamic analysis has been performed using Bode plot

technique. For frequencies much less than the loop bandwidth the loop could be simplified as a simple gain. In the next chapter this simplified model of the current loop is used for modeling and analysis of the voltage loop.

CHAPTER - 6

LOW FREQUENCY DYNAMIC MODELING AND ANALYSIS

Utility line current conditioner supplies rectifier type of load and draws sinusoidal current from the supply. The rectified dc voltage is regulated by the outer voltage loop. Modeling the voltage-regulating loop is necessary to design the system to meet the desired performance. Utility line current conditioner supplying a rectifier type of load forms a non-linear system. Supply current and voltage of the line conditioner could be considered as sinusoidal, however the output current is not sinusoidal and the output voltage is trapezoidal. This makes the modeling challenging. It is not straightforward to apply the modeling techniques to the overall system consisting of the utility line current conditioner and the load. This chapter presents a simple approach to modeling the overall system.

6.1 Control Scheme for Output Voltage Regulation

Section 3.2 introduces to the control scheme of the utility line current conditioner. The multiplier block in the voltage loop of Fig. 3.2 has been shown in detail in Fig. 6.1. The output of the voltage controller is multiplied with the sine-wave shape I_{sine} and divided by the square of feed-forward voltage V_{ff} . The feed forward voltage V_{ff} is proportional to the average input voltage. The gain of the voltage loop would change with the square of the input voltage without the feed-forward circuit. However, the voltage loop gain will be independent of the input voltage if the voltage controller output is divided by the square of feed-forward voltage as shown in Fig. 6.1.

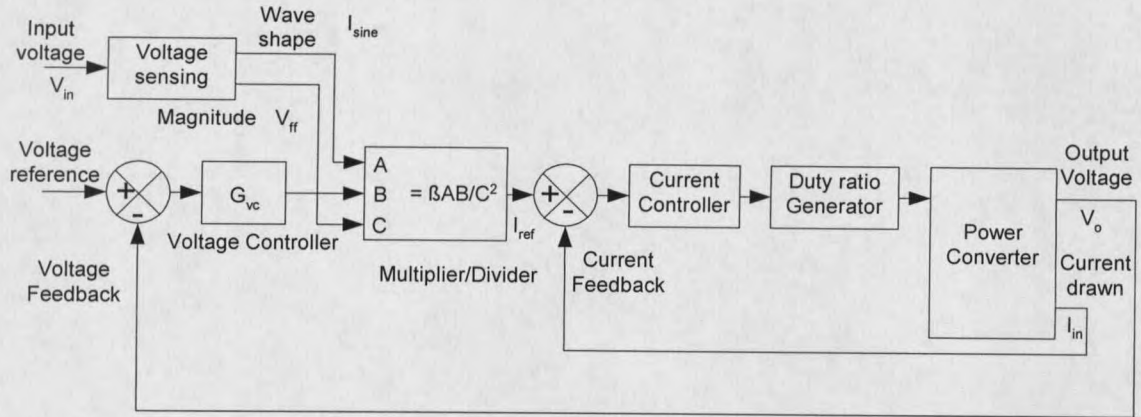


Fig. 6.1: Block diagram of the control circuit.

6.2 The Overall System including the Rectifier Load.

Modeling of ac to dc unity power factor rectifiers is presented in Reference [16,17,18]. Study of these modeling approaches is instructive, but extension of these concepts towards modeling ac to ac utility line current conditioner is not straightforward. The objective here is to get an accurate low frequency model of the complete system in order to design the parameters of the voltage control loop.

With reference to Fig. 3.5, the rectifier dc voltage V_{dc} is not directly measured to regulate it. The output voltage V_o , which is measured is a direct reflection of the dc voltage V_{dc} . Through this, the load parameters enter into the dynamics of the system.

The load has filter capacitance C_L and load resistance R_L . A simplified block diagram of the system is shown in Fig. 6.2.

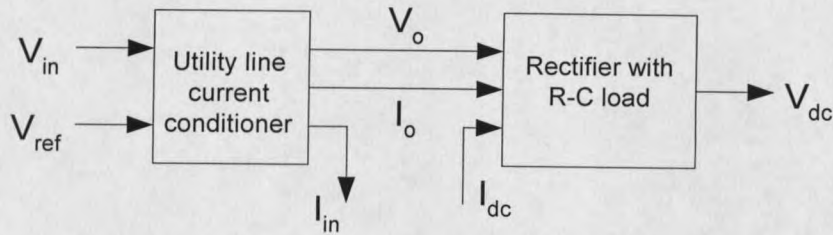


Fig. 6.2: Utility line current conditioner supplying a rectifier type of load.

As seen in Fig. 3.6, output voltage of the utility line current conditioner is close to a square wave with peak value V_{dc} . So for modeling purposes, V_{dc} may be considered as the output instead of V_o . I_o is “sine-squared” waveform as shown in Fig. 3.6. Its average value may be defined as I_o . V_{in} refers to the rms input voltage.

6.3 Averaged Low Frequency Model

Considering the half cycle average value for I_o and V_{dc} , the system could be modeled as shown in Fig. 6.3. This model will faithfully represent the system dynamics for frequencies below the supply frequency. For the voltage loop design we are interested in frequencies below 20 Hz, where this model could be used to analyze and design the system. Each block is inspected in detail below.

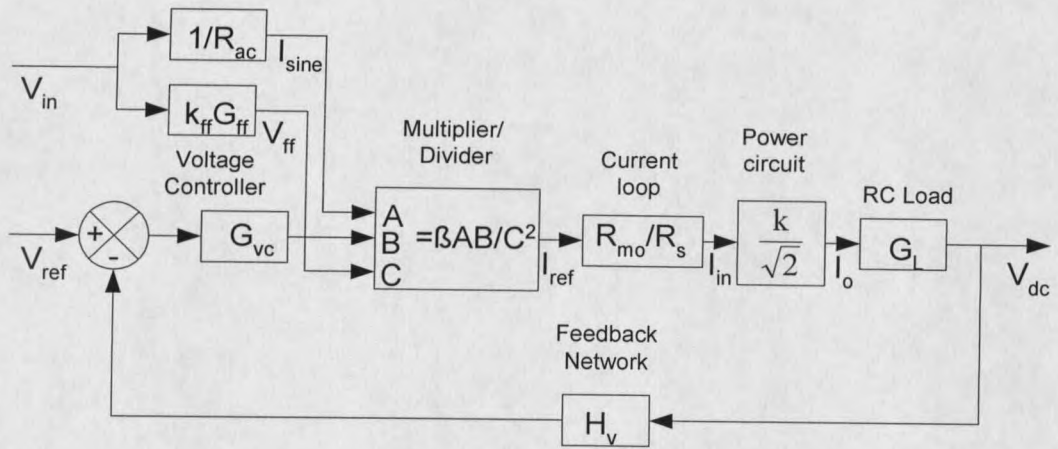


Fig. 6.3: Low frequency dynamic model of the utility line current conditioner.

6.3 a) R-C Load

The equivalent circuit for this part could be drawn as in Fig. 6.4. V_{dc} is a dc voltage and I_o is the average current

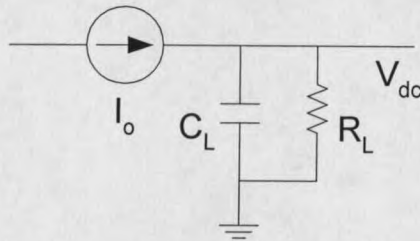


Fig. 6.4: Equivalent circuit of the load.

From the circuit above it is straightforward to write the transfer function as

$$G_L(s) = \frac{V_{dc}(s)}{I_o(s)} = \frac{R_L}{1 + sC_LR_L} \quad (6.1)$$

6.3 b) Power Circuit of the Line Current Conditioner

The equivalent circuit of the boost power stage is shown in Fig. 6.5. The relationship between the average value of the output current I_o and the input current I_{in} is of interest.

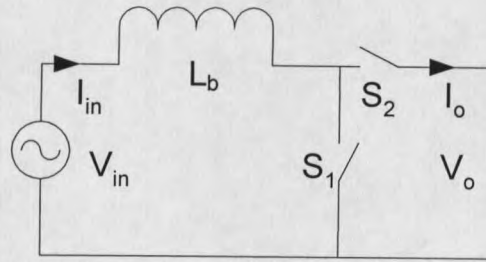


Fig. 6.5: Equivalent circuit of the boost power stage.

V_{in} and I_{in} are supply frequency sine waves

$$V_{in}(t) = V_m \sin(\omega t) \quad I_{in}(t) = I_m \sin(\omega t) \quad (6.2)$$

Using power balance

$$V_o(t)I_o(t) = V_{in}(t)I_{in}(t) \quad (6.3)$$

Where $V_o(t)$ is V_{dc} multiplied by a sgn function

$$V_o(t) = V_{dc} \text{sgn}[\sin(\omega t)] \quad (6.4)$$

Using (6.2), (6.3) and (6.4)

$$I_o(t) = \frac{V_m}{V_{dc}} I_m \sin^2(\omega t) \text{sgn}[\sin(\omega t)] \quad (6.5)$$

Denoting average of $I_o(t)$ as I_o

$$\frac{I_o}{I_m} = \frac{k}{2} \quad (6.6)$$

Denoting I_{in} as the input rms current

$$G_{pc} = \frac{I_o}{I_{in}} = \frac{k}{\sqrt{2}} \quad (6.7)$$

6.3 c) Current Loop

The simplified block diagram of the current loop was developed in Chapter 5. The transfer function is given by

$$G_{cl} = \frac{I_{in}}{I_{ref}} = \frac{R_{mo}}{R_s} \quad (6.8)$$

6.3 d) Voltage Controller

Voltage control loop maintains constant dc voltage at the load. If the bandwidth of the voltage loop were large it would undesirably modulate the input current. This requires that the voltage loop bandwidth is less than the supply frequency. From the transient response consideration loop bandwidth should be large as possible. A bandwidth of around 20 Hz is a good compromise between the two conflicting requirements. A dominant pole controller gives good result for this application. The schematic of the voltage controller is given in Fig. 6.6.

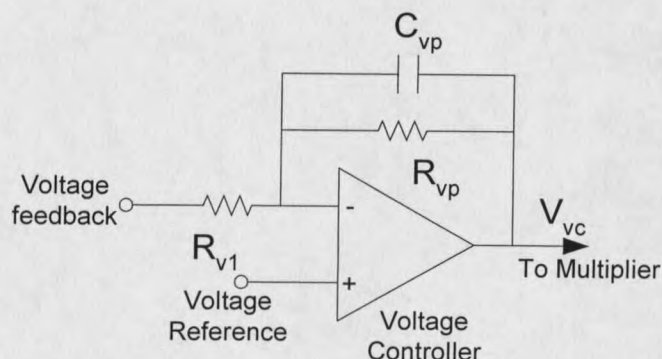


Fig. 6.6: Schematic of the voltage controller.

The transfer function of the controller is given by

$$G_{vc}(s) = \frac{R_{vp}}{R_{v1}} \frac{1}{1 + s C_{vp} R_{vp}} \quad (6.9)$$

6.3 e) Feedforward Section

As explained in Section 6.1 feed forward voltage V_{ff} is squared and fed into the divider to keep the loop gain independent of the input voltage. The feed forward signal V_{ff} is proportional to the average input voltage. Any supply frequency noise present in V_{ff} distorts the input current waveform. Adequate filtering needs to be done to remove the supply frequency components of the input voltage V_{in} . A second order filter with poles at ω_{ff1} and ω_{ff2} has been used, The dc gain k_{ff} is the ratio of the feed forward voltage V_{ff} to the rms input voltage V_{in} . With these parameters the transfer function is given by

$$\frac{V_{ff}(s)}{V_{in}(s)} = K_{ff} G_{ff}(s) \quad (6.10)$$

$$G_{ff}(s) = \frac{1}{\left(1 + \frac{s}{\omega_{ff1}}\right) \left(1 + \frac{s}{\omega_{ff2}}\right)} \quad (6.11)$$

6.3 f) The Sine Wave Modulator Signal

Inside the multiplier, the output of the voltage controller is modulated by the waveform derived from the input voltage. This is the input sine wave current I_{sine} .

$$\frac{I_{\text{sine}}}{V_{in}} = \frac{1}{R_{ac}} \quad (6.12)$$

6.3 g) The Multiplier

From Fig. 6.3 it is straightforward to write down the multiplier gain. The constant β has units of voltage but it's magnitude is unity.

$$G_m = \beta \frac{I_{\text{sine}}}{V_{ff}^2} \quad (6.13)$$

6.3 h) The Feedback Network

There are two ways to determine the feedback path transfer function. One is to follow the circuits in the feedback path and determine the gain or attenuation of each section and multiply. The other approximate way is to say that the feedback path gain H_v has to equal to the ratio of V_{ref} to V_{dc} .

$$H_v = \frac{V_{ref}}{V_{dc}} \quad (6.14)$$

6.4 Loop Stability of the Voltage Control Loop

With reference to the block diagram of Fig. 6.3 for a constant input voltage, the system is linear with respect to V_{ref} . The simplified block diagram is presented in Fig. 6.7.

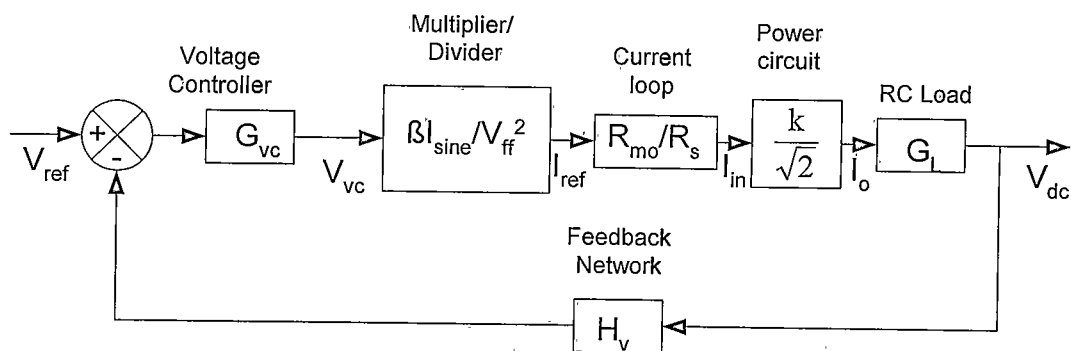


Fig. 6.7: Simplified block diagram of voltage control loop for stability analysis.

With all the blocks known it is possible to perform stability analysis by studying the bode plot of the loop gain.

$$G_{\text{loop}}(s) = G_{\text{vc}}(s) G_{\text{m}} G_{\text{cl}} G_{\text{pc}} G_{\text{L}}(s) H_{\text{v}} \quad (6.15)$$

It should be noted that the loop dynamics depends on the loading R_{L} . The circuit has to operate for any load including no load. The system is a simple second order system. Since the reference voltage is not likely to have any dynamics, transient response of output voltage for any change in the reference voltage is not important. However, voltage loop needs to be stable. Following are the Bode plots under rated conditions.

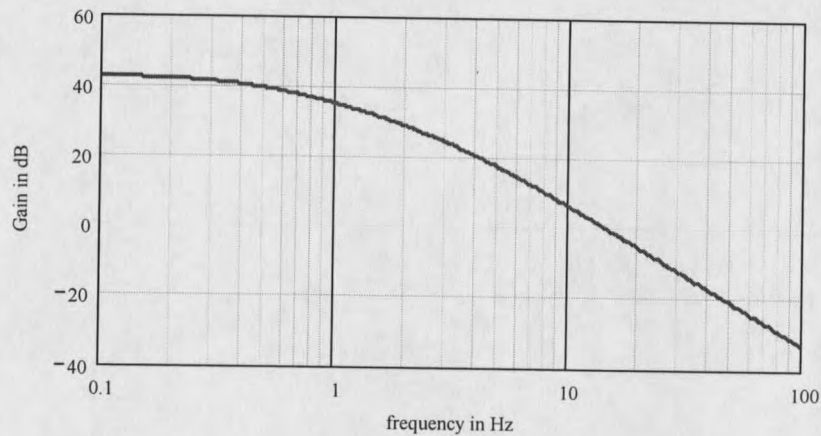


Fig. 6.8: Gain plot of the voltage loop.

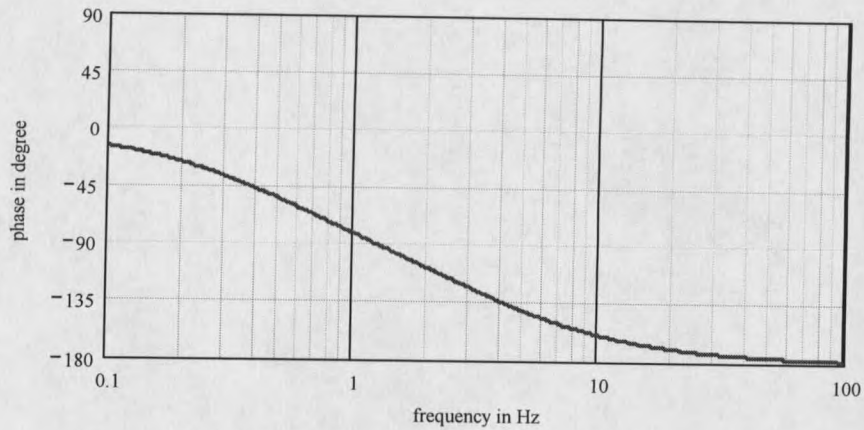


Fig. 6.9: Phase plot of the voltage loop.

It is seen that the bandwidth is around 15 Hz and the dc gain is 42 dB. The phase margin is very poor, about 15° . Different types of voltage controllers could be investigated to improve the phase margin. In practice, large slow start capacitor is used to reduce the transient overshoot associated with poor phase margin. With reference to Fig. 6.6 the above plots are for the following control circuit parameters.

Table – 4 Voltage controller component values

Symbol	Value
R_{v1}	5.6 k
R_{vp}	22 k
C_{vp}	2.2 μ F

6.5 Closed Loop Output Impedance

The utility line current conditioner supplying a rectifier type of load should be able to regulate the dc voltage against load variations. This performance could be studied by considering the closed loop output impedance. Ideally, the closed loop output impedance should be zero for steady state. To study this, we modify the block diagram of Fig. 6.7 to as shown in Fig. 6.10.

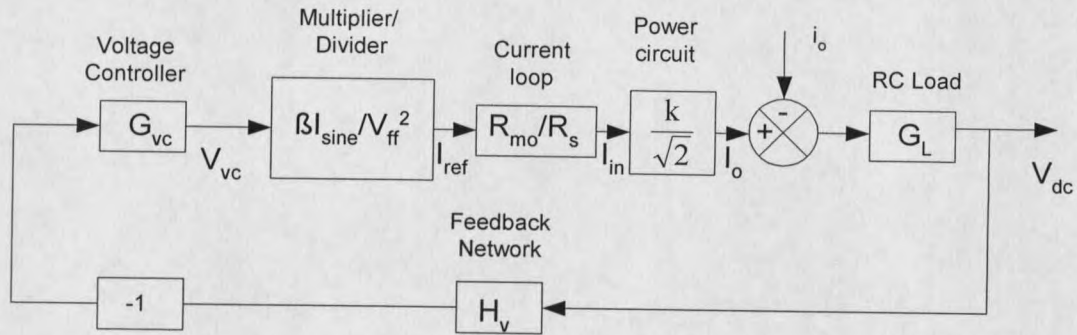


Fig. 6.10: Block diagram to determine output admittance.

The output impedance is given by

$$Z(s) = \frac{G_L(s)}{1 + G_{loop}(s)} \quad (6.16)$$

Plot of output impedance is presented in Fig. 6.11. The output impedance is normalized with respect to 1Ω and the ratio is plotted on a dB scale.

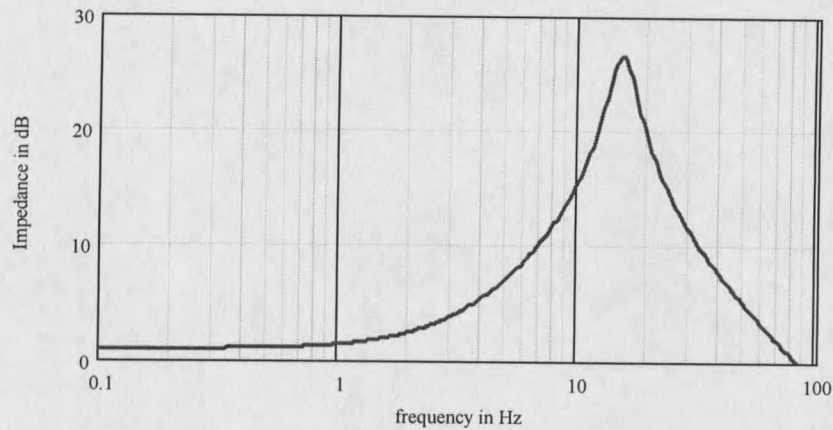


Fig. 6.11: Plot of closed loop output impedance.

Dc output impedance is about 1.2Ω . Impedance increases at higher frequencies and at the gain crossover frequency it goes to a very large value. This is because the denominator in Eq. 6.16 becomes close to zero at gain crossover frequency. This is also a consequence of poor phase margin of the voltage loop.

6.6 Small Signal Model and Input Susceptibility

The utility line current conditioner supplying a rectifier type of load should be able to regulate the dc voltage against variations of input voltage. This could be studied by examining the transfer function between the input voltage and the output voltage. Due to the presence of the multiplier block, the model is not linear with respect to input voltage. However, by introducing small perturbations around the steady state operating

point it is possible to develop a small signal linear model. The resulting small signal linear model is presented in Fig. 6.12.

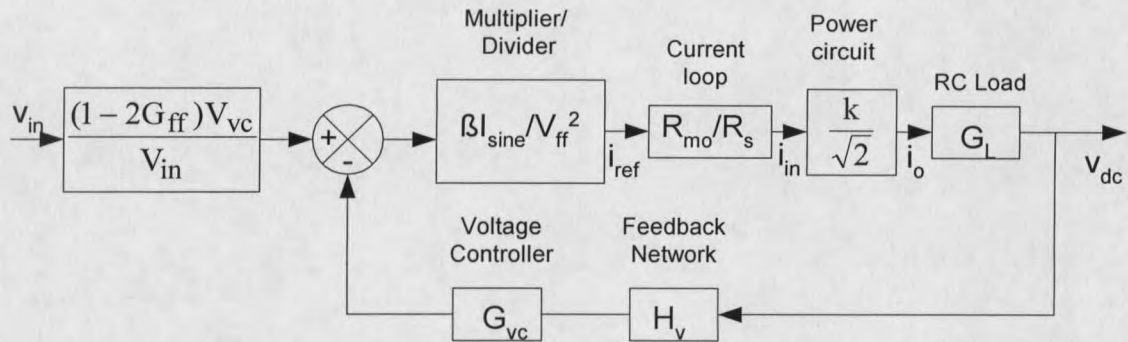


Fig. 6.12: Small signal model to determine input susceptibility.

The small signal quantities are denoted by lower case letters and the operating point is represented by quantities in capital letters. Input susceptibility could be calculated as

$$\frac{v_{dc}(s)}{v_{in}(s)} = \left(\frac{(1 - 2G_{ff}(s))V_{vc}}{V_{in}} \right) \left(\frac{G_m G_{cl} G_{pc} G_L(s)}{1 + G_{loop}(s)} \right) \quad (6.17)$$

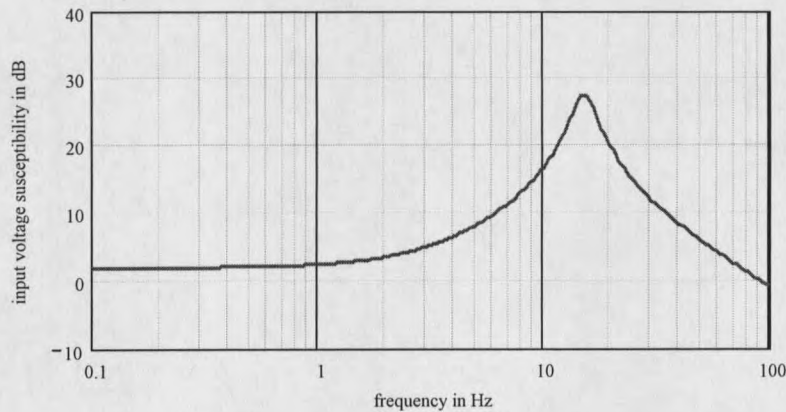


Fig. 6.13: Plot of small signal input susceptibility.

Plot of input susceptibility is presented in Fig. 6.13. In steady state, input susceptibility is about 2 dB. This is large if we consider large variations of input voltage. However, large variations of input voltage are compensated for by the feed forward technique. This input susceptibility is valid for small signal response only. Input susceptibility increases to a very high value if the noise frequency of the input voltage becomes close to gain crossover frequency. This is because the denominator in Eq. 6.17 becomes close to zero at gain crossover frequency. This is also a consequence of poor phase margin of the voltage loop.

6.7 Loop Design

From the above discussion it is straightforward to complete the closed loop design. The voltage controller used is a dominant pole controller. However, a PI controller could be used for improved phase margin. The Mathcad[®] program for the voltage loop analysis and design is presented in Appendix –D. With the Mathcad[®] program it is possible to decide the gain and the pole position of the voltage controller. But it is desirable to have some simpler technique to start a design. Reference [15] presents step by step design procedure for ac to dc unity power factor converter and could be extended to ac to ac application.

Conclusion

A straightforward technique to model the line current conditioner has been presented. The diode rectifier is a non-linear system. However, there are definite relationships between the supply frequency rms input quantities and the dc output quantities that enables development of such a model. The boost stage is modeled starting from the basic principle of power balance. A block diagram of the overall system is presented. From the block diagram it is possible to perform the stability analysis and determine the components of the voltage controller. The Bode plots of the loop gain are presented. Other quantities of interest for this problem are the input susceptibility and the output admittance. Block diagram for determining the output impedance is presented. Small signal linear model for determining input susceptibility is also given.

So far all the necessary tools and analysis techniques have been presented. Next chapter focuses on some details of the circuits used in the prototype converter that was assembled to demonstrate the concept. The next chapter also presents some experimental results on the prototype converter.

CHAPTER- 7

EXPERIMENTAL RESULTS

This chapter presents the details of the hardware implementation of the utility line current conditioner. The circuit diagrams of the power circuit and the drive circuit are presented. The pictures of the assembled prototype are presented. Waveforms of input current under different operating conditions are presented. By incorporating differentiator circuit in the current reference the zero crossing spike has been improved. Further improvement of the zero crossing spikes by reactive reference current injection is proposed. The experimental results of the line and the load regulation are presented. The harmonic spectrum of the input current is presented.

7.1 Power Circuit and Drive Circuit

The complete power circuit is presented in Fig. 4.2. The power switches used are MOSFET IRP360 400V, 23A, TO – 247 package. Other than the basic switches, the circuit incorporates snubber circuit and additional capacitors directly across each leg of the power switches to reduce the switching spikes. Current is being sensed with the current sensing resistor R_s . The current is rectified through a bridge rectifier (MBR-1645) and then passed through the resistor R_s .

The drive circuit is presented in Appendix E. In the drive circuit opto-isolator HP 4503 has been used to provide isolation between the power and the control circuit. IR2111

high and low side driver has been used to drive the MOSFETs. The floating channel of IR2111 can be used in bootstrap mode to drive the high side MOSFET.

7.2 Control Circuit

The schematic of the control circuit is presented in Appendix F. UC3854A has been used to realize the control requirements. A supply frequency transformer is used for sensing the input voltage V_{in} . The transformer output is passed through a half bridge rectifier and connected to the current reference (pin - 6) through a resistor. The output of the half bridge rectifier is passed through a two pole RC filter, which gives the feed forward signal V_{ff} .

The PI controller for the current loop has been described in Section 5.2. The voltage controller has been described in Section 6.3d.

Next discussed are some important parts of the control circuit.

7.2 a) Peak Detector Circuit Used to Sense the Output Voltage

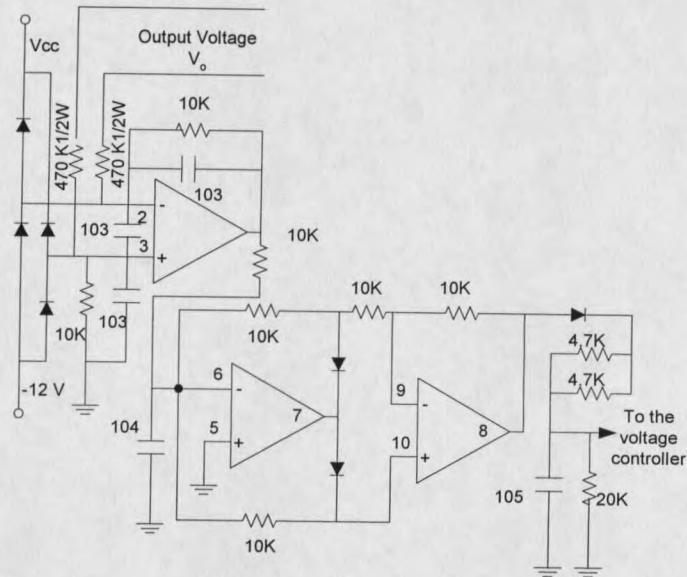


Fig. 7.1: The peak detector circuit used in sensing the output voltage.

Utility line current conditioner should be able to control the dc voltage of the rectifier load, V_{dc} . The rectifier is not directly accessible, the output voltage of the line current conditioner, V_o is sensed and used as sense voltage. The peak of V_o is the same as V_{dc} . As seen in Fig. 3.7, V_o is a trapezoidal waveform. Hence it is necessary to sense only the peak of V_o . The peak detector circuit is presented in Fig. 7.1.

7.2 b) The Differentiator Circuit

Section 3.8 illustrates how a phase lead in reference current with respect to the input voltage would reduce the zero crossing spikes in the input current. The control circuit can not in principle implement this feature because this circuit does not treat the ac

signals directly, instead it uses the rectified ac signal. However, due to circuit delays and other non-idealities a simple differentiator circuit in the reference current signal reduces the zero-crossing spikes of the input current. Fig. 7.2 illustrates the differentiator circuit used in the prototype. The resistance R_{ac} has been split into two and across one of them a capacitor is connected. It has been demonstrated that introduction of phase lead in reference current signal improves zero crossing spikes.

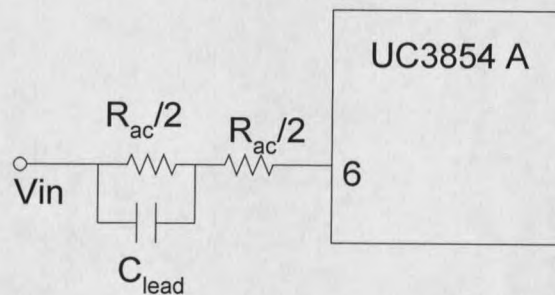


Fig. 7.2: *Differentiator circuit in the reference current path.*

7.2 c) Reactive Current Injection Circuit

As seen in Fig. 3.1 the capacitor C_o is connected across the output. The capacitor is a reactive component and appropriate reactive current needs to be supplied. This reactive current signal should not come through the voltage loop because this current magnitude is dependent on the output voltage and not on the input voltage. The reactive current could be added after the multiplier/divider block in Fig. 6.1. This modification is illustrated in Fig. 7.3.

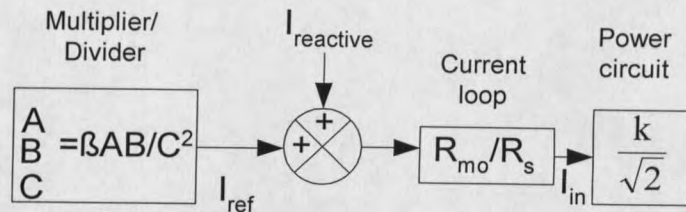


Fig. 7.3: Reactive current injection scheme.

In Section 3.8 it was proposed that a phase lead between the input voltage and the reference current signal would eliminate zero crossing spikes. The reactive current injection scheme in principle provides the necessary phase lead. The approach of reactive current injection scheme is better suited for practical implementation. In the phase lead approach, the required phase lead needs to be changed dynamically depending on the loading. But in the reactive current injection scheme, the required reactive current depends on the input voltage and the circuit parameters, and hence it is easier to tune.

7.3 Prototype Assembly

Two prototypes of utility line current conditioner have been built and tested extensively. Fig. 7.4 shows the power circuit of the first prototype. Picture of the second prototype is presented in Fig. 7.5. All the waveforms and the results to be presented next are taken on the second prototype.

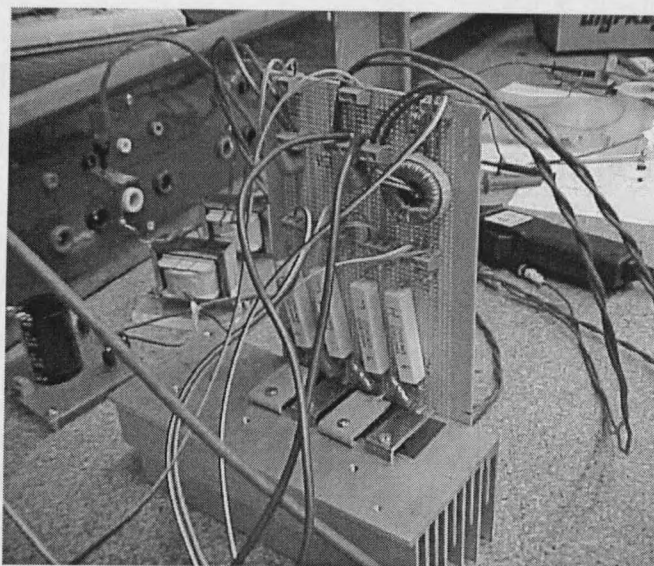


Fig. 7.4: The power circuit of the first prototype.

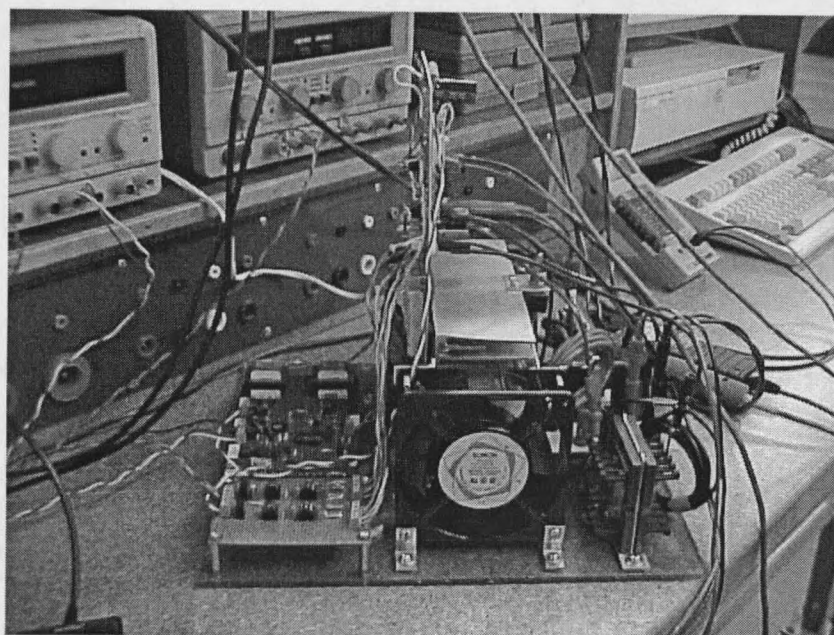


Fig. 7.5: The second prototype set up.

7.4 Experimental Results - Waveforms

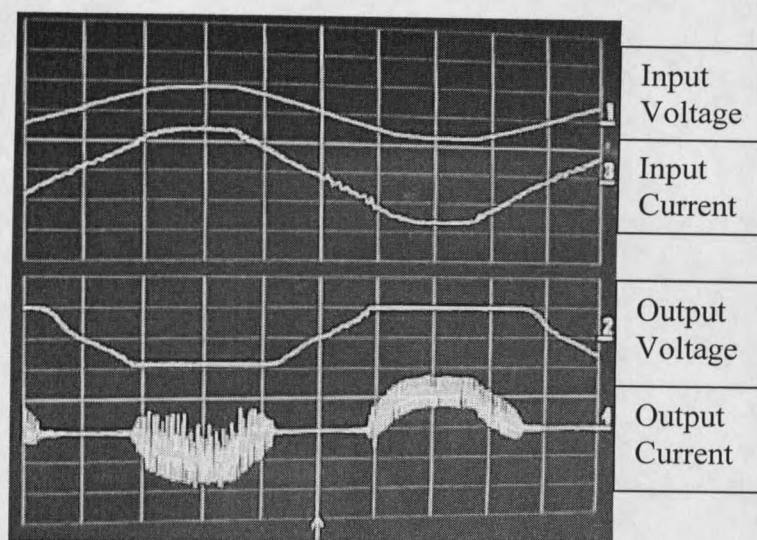


Fig. 7.6: Experimental waveforms for input voltage – 110 V, input power – 424 W, output power – 267 W, rectifier type of load with load resistance 140 Ω .

Fig. 7.6 presents a representative early waveform. It is seen that the input current is a very clean waveform and closely resembles the input voltage without any zero crossing spikes. The output voltage is a trapezoidal wave as has been analytically shown in Fig. 3.6. The output current is of sine-square wave except that the current stays at zero when the output capacitor changes polarity. The output current also contains significant switching frequency ripple. This ripple is not necessarily a negative feature because the output current is only an intermediate variable. Large L-C filter in the output will reduce the output current ripple but it will deteriorate the input current waveform. So a compromise between the two conflicting requirements has to be made. Some more waveforms for different type of load are presented.

7.4 a) Computer Load

A Micron personal computer (Model no- AL440LX-PII300-CR) was used as a load. The waveforms are presented in Fig. 7.7. Zero crossing spike in input current is present and is more than with the rectifier load shown in Fig. 7.6. Increased zero crossing spike is the effect of series inductance likely to be present in the input of the computer.

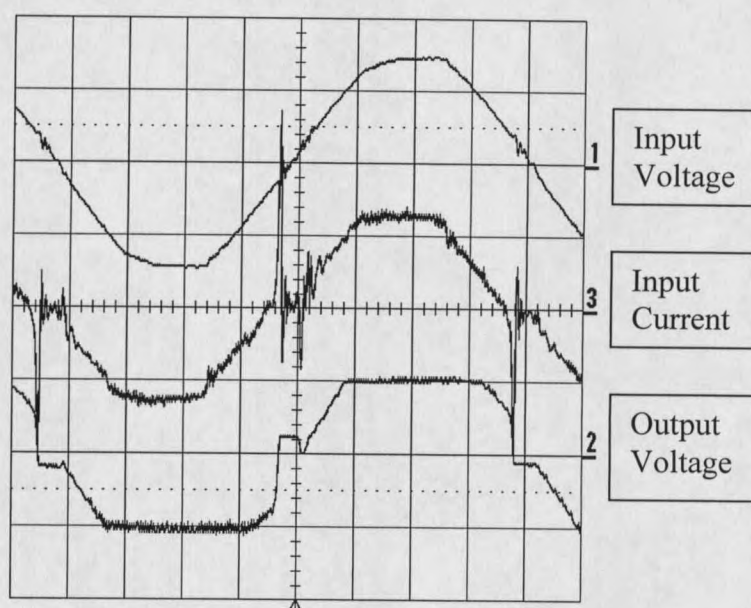


Fig. 7.7: Experimental waveforms for input voltage – 110 V, input power - 210 W, output power – 121 W, computer load.

7.4 b) Rectifier Load

A full bridge rectifier was built in the lab. Filter capacitor was 2000 μF . Fig. 7.8 presents the waveforms with load resistor of 73 Ω .

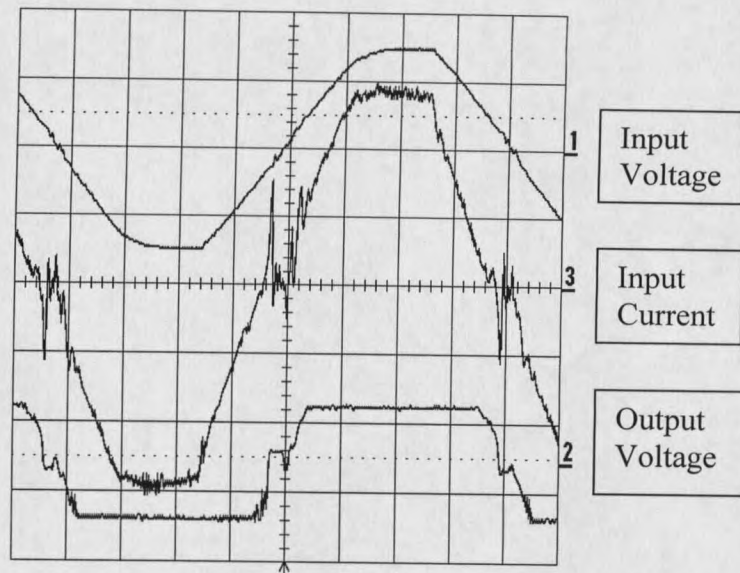


Fig. 7.8: *Experimental waveforms for input voltage – 110 V, input power - 445 W, output power – 359 W, rectifier load with 73 Ω resistance.*

7.4 c) Resistive Load without the Diode Bridge Rectifier

It may be of interest to operate the line current conditioner without the rectifier. Fig. 7.9 presents the waveform for this case. Important thing to note is the output voltage waveform is perfectly sinusoidal instead of trapezoidal. In this mode the system works as a boost regulator.

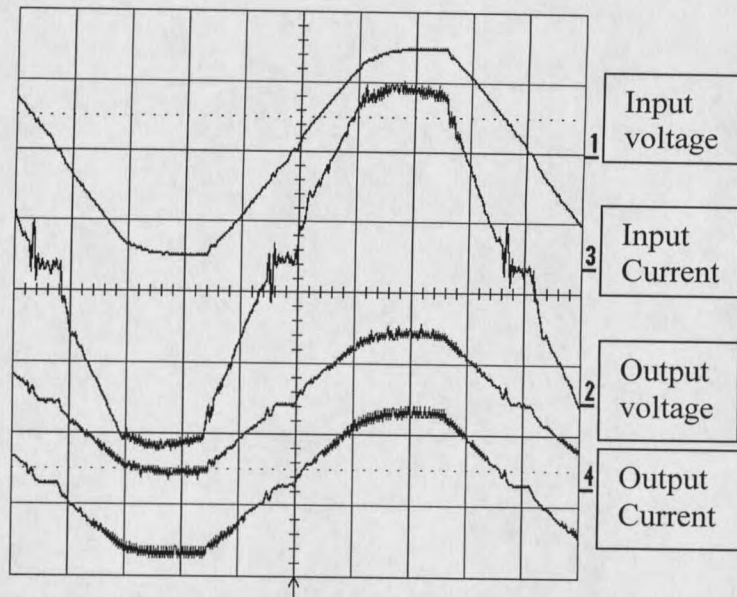


Fig. 7.9: Experimental waveforms for input voltage – 110 V, input power - 391 W, output power – 336 W, resistive load without the rectifier.

7.5 Experimental Results - Performance Analysis

The desired performances expected from a utility line current conditioner are that the harmonics in the input current should be very small, the dc voltage of the rectifier load should be well regulated against line and load variations and it should be energy efficient. The performance analysis results are tabulated in Appendix G. The following performance indices are studied below.

7.5 a) THD in Input Current

Input current total harmonic distortion (THD) as a percentage of the fundamental is presented in Fig. 7.10. These results are for 110 V input voltage, rectifier type of load, the load resistance was changed from 300 to 70 Ω . For 166 W output power the total harmonic distortion is 16.2 %. However, for computer load THD is more. For two Micron computers as load, THD is 26.7%. This result could be compared against a THD of 117% of the same computer without the line current conditioner.

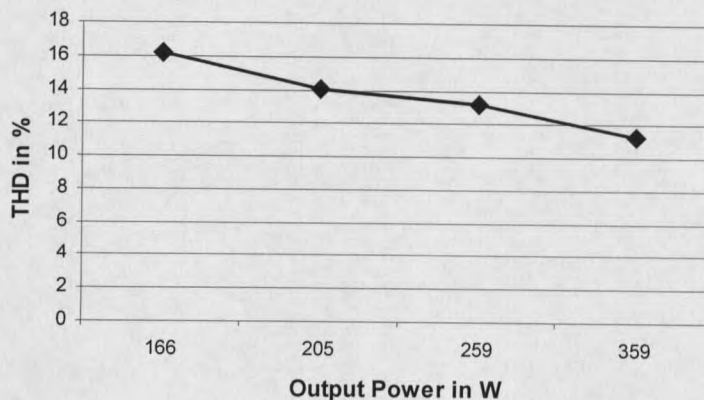


Fig. 7.10: *Percentage total harmonic distortion of the input current of the prototype converter as a function of output power.*

7.4 b) Individual Harmonic Contents

Individual harmonics of the input current as a percentage of the fundamental is presented in Fig. 7.11. Input voltage is 110 V and two personal computers are used as load. Individual harmonics as well as the THD is well within the IEC specifications.

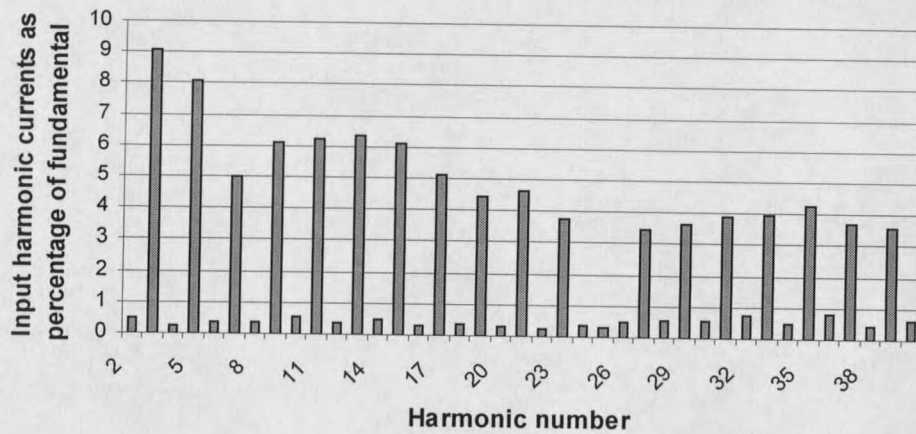


Fig. 7.11: Individual harmonics of the input current of the prototype converter.

7.5 c) Line Regulation

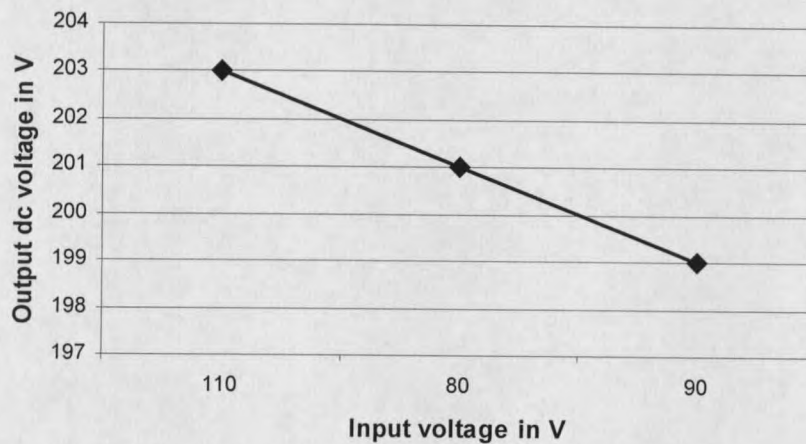


Fig. 7.12: Line regulation of the rectified dc voltage of the prototype converter.

Line regulation of the rectified dc voltage V_{dc} is presented in Fig. 7.12 as the line voltage changes from 90 to 110 V. The line regulation is excellent even beyond this voltage range. The converter operates with the good line regulation from 70 to 130 V. The price of operating at low input voltage is the consequential increase in input current.

7.5 d) Load Regulation

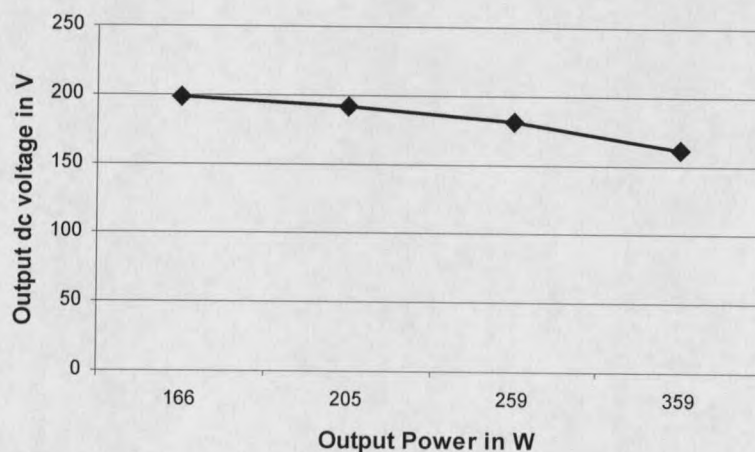


Fig. 7.13: Load regulation of the rectified dc voltage of the prototype converter.

Load regulation of the rectified dc voltage, V_{dc} is presented in Fig. 7.13. These results are for 110 V input voltage, rectifier type of load, the load resistance was changed from 300 to 70 Ω . The load regulation is not so satisfactory. The voltage being regulated is the output voltage of the rectifier. This voltage is not available for sensing. This

information is derived by sensing the output voltage of the utility line current conditioner. The poor load regulation is attributed to the inherent errors in voltage sensing with the present circuit. In principle, it is possible to achieve very good output voltage regulation.

7.5 e) Efficiency

Efficiency of the line current conditioner is presented in Fig. 7.14. These results are for 110 V input voltage, rectifier type of load, the load resistance was changed from 300 to 70 Ω .

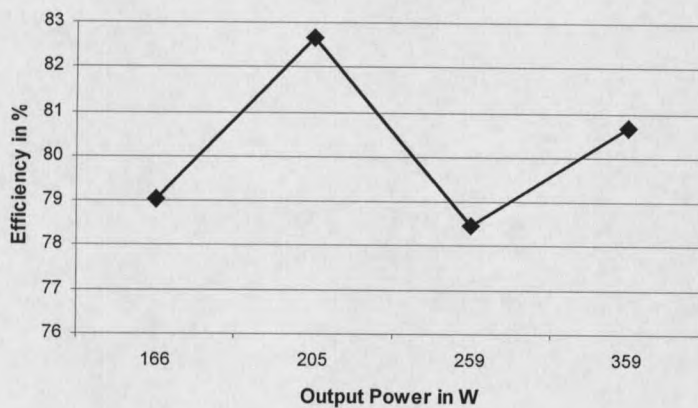


Fig. 7.14: Efficiency of the prototype converter as a function of output power.

The converter was designed for 750 W. It has been tested up to 359 W. The present circuits used to implement the converter could be modified to go up to the full power. However, at full power, the efficiency is estimated to be better, around 85%. By

incorporating more intelligent DSP based control circuit and thereby reducing the snubber power losses it would be possible to increase the efficiency beyond this limit.

Conclusion

The experimental results to demonstrate the basic principle of the utility line current conditioner has been presented. Different parts of the control circuit have been explained. Reactive current injection scheme to improve the zero crossing spikes has been proposed and the scheme has been explained in block diagram. The waveforms of the utility line current conditioner have been presented for three different types of loads- computer load, rectifier load and resistive load. The performance curves of the prototype converter has been presented. Total harmonic distortion and individual harmonics have been plotted. Line regulation and load regulation of the output dc voltage and the efficiency of the utility line current conditioner have been presented.

The objective of demonstrating utility line current conditioner has been realized. Experimental verification of the modeling techniques described in Chapter 5 and 6 will represent logical continuation of the work. The next chapter proposes a few areas for further investigation.

CHAPTER – 8

CONCLUSIONS

A different approach to solve power quality problems caused by non-linear loads has been presented. With the increase of the use of data processing devices these non-linear loads are becoming a large part of the total load from the supply line. The proposed utility line current conditioner can be used as an interface between the supply line and the non-linear load. The solution needs to be applied only when the problem becomes severe and causes persistent malfunction of the device or other devices connected to the same line. The boost ac-ac converter has been adapted to perform line current control in a single-phase line, loaded by a rectifier load. The utility line current conditioner utilizes an inner average current control loop with an outer voltage control loop to perform the active wave-shaping function.

A detailed analysis of the basic converter and its principle of operation have been presented. Equivalent circuits and defining equations for different switching intervals have been given. The defining equations are essential for any further analysis and modeling. The zero crossing spike of the input current has been analyzed. It is demonstrated that appropriate phase lead in the reference current with respect to the supply voltage could potentially eliminate zero crossing current spikes. Simple formulas

to determine rms and average current in different branches have been presented. Complete power circuit has been presented and design of power circuit components has been outlined.

The model of average current controller available in literature has been modified to represent the circuit in context. It has been shown that the inner current loop has high bandwidth, which is necessary to achieve wave shaping of the input current. It has been shown how current loop may be simplified and modeled as a simple gain for low frequency applications. Dynamic modeling and analysis of the complete system of utility line current conditioner supplying rectifier type of load have been presented. The rectifier has been modeled by using the linear relationship between the input rms voltage and the output dc voltage. Models of different subsystems have been shown separately. Loop stability, output impedance and input susceptibility have been discussed.

Experimental results on a 750 W prototype have been presented. Reactive current injection to improve zero crossing spikes has been discussed. The input current waveform has been presented for different types of loads, computer load, rectifier load assembled in the laboratory, and resistive load. Line regulation and load regulation of the rectifier output voltage have been presented. Harmonic performance of the input current has also been analyzed quantitatively.

The application of the modeling technique to the complete system of utility line current conditioner supplying rectifier type of load is versatile and could be applied to many power converter circuits. In particular, it is directly applicable to ac to dc unity power factor rectifiers. The modeling technique is elegant, and directly useful for design.

The objective of demonstrating utility line current conditioner has been realized. However, there are several avenues open for future investigations as outlined further.

The concept of reactive current injection scheme of Sec. 7.2c could be verified experimentally. It has been demonstrated that this has the potential to eliminate the zero crossing spikes in input current.

Inadequate voltage regulation is attributed to the error in determining the rectifier output voltage from the available output voltage of utility line current conditioner. This was explained in Sec. 7.5d. DSP based control scheme with adaptive gain scheduling to track the operating conditions would improve voltage regulation. It would also improve dynamic performances of the voltage loop.

It is possible to devise an alternative switching strategy to reduce the power loss in the snubber. With reference to Fig. 4.2, in the positive half of the supply voltage upper S_2 could be kept OFF and lower S_2 could be kept ON. This will avoid high frequency switching of S_2 . S_1 could be operated as per the duty ratio command but there will be no

need of any dead time. If dead time is eliminated, the power loss in snubber components gets reduced by orders of magnitude. This will result in increase in efficiency.

The modeling techniques described in Chapter 5 and 6 could be verified experimentally. This would involve frequency response measurement and suitable instrumentation techniques. It will be an important continuation of the present work, due to its potential for application to a wide range of power converters, specifically ac to dc unity power factor rectifiers.

Ac to ac power converters have only recently been identified for various power control functions and their application potential have not been completely investigated. The studies presented in this thesis represents one small step in widening the application scope of pulse width modulated ac to ac converters.

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APPENDICES

APPENDIX - A

POWER CIRCUIT DESIGN

Specifications**Symbol Value**

Output power	Po	750	W
Maximum input Voltage	Vinmax	126	V
Minimum input Voltage	Vinmin	108	V
Target Efficiency	Ef	0.98	
Worst case efficiency for power Calculation	Efw	0.92	
Inductor ripple current factor in CCM (Peak to Peak)	rfccm	0.1	
Dc bus voltage	Vdc	200	V
Switching frequency	fs	5.00E+04	Hz
Supply frequency	f	60	Hz

Derived quantities**Symbol Formula****Value**

Input Power	Pin	Po/Efw	815.217	W
Peak Max input Voltage	Vinpkmax	Vinmax*sqrt(2)	178.191	V
Peak Min input Voltage	Vinpkmin	Vinmin*sqrt(2)	152.735	V
Min input current	Imin	Pin/vinmax	6.46998	A
Max input Current	Imax	Pin/vinmin	7.54831	A
Min input current Peak	Ipkmmin	Imin*sqrt(2)	9.14993	A
Max input Current Peak	Ipkmmax	Imax*sqrt(2)	10.6749	A
Cycle time for switching frequency	Ts	1/fs	0.00002	s
Dc side ouput current	Idc	Po/Vdc	3.75	A

Inductor Design

Ratio of Vinpkmin to Vdc	k	Vinpkmin/Vdc	0.76368	
max. Pk-Pk ripple current	Irp	Ipkmmax*rfccm	1.06749	A
Input current average at min voltage	Iinav	Imax*2*sqrt(2)/PI()	6.79587	A
Duty ratio at min Voltage peak	dpk	(Vdc-Vinpkmin)/Vdc	0.23632	
Boost inductor	Lb	Vinpkmin*dpk/(fs*Irp)*100	0.67626	mH
Inductor peak current	ILpk	Ipkmmax*(1+rfccm/2)	11.2087	A

Mosfet selection

Switch peak current	Isp	ILpk	11.2087	
Boost switch average current	Isav1	Iinav*(1-k*PI()/4)	2.71978	A
Freewheel switch average current	Isav2	Idc	3.75	A
Mosfet peak voltage	Vspk	Vdc*1.2	240	V**

** from simulation

Selected Mosfet IRFP360 from international rectifier, 400 V, 23 A, TO - 247 package

· APPENDIX - B

INDUCTOR DESIGN

$L := 0.4 \cdot 10^{-3}$	Inductor value L
Peak Current through the inductor	$I_p := 12$
Rms inductor current	$I_{rms} := 8$
Assume J in A/sq.m	$J := 2 \cdot 10^6$
Assume kw	$kw := 0.5$
Assume max. flux density Bm	$B_m := 0.3$
Compute Area Product in sq. cm	$A_p := \frac{L \cdot I_p \cdot I_{rms}}{kw \cdot J \cdot B_m} \cdot 10^8$
	$A_p = 12.8$

Select Core EC/70/34/17 Siemens ferrite pot core

Core Area in sq m	$A_c := 2.79 \cdot 10^{-4}$
Window area in sq m	$A_w := 4.69 \cdot 10^{-4}$
Select wire area	$AW := \frac{I_{rms}}{J}$
	$AW = 4 \cdot 10^{-6}$
Select wire area in sq.cmX1000	$AW \cdot 10^4 \cdot 10^3 = 40$

Select wire gauge 11 AWG

Turns per sq cm of the selected wire = 13.5	
Max. possible No. of turns	$N_{max} := 13.5 \cdot AW \cdot 10^4$
	$N_{max} = 63.315$
	$N := 62$

Select number of turns as 62

Compute air gap lg in mm	$l_g := \frac{N^2 \cdot A_c \cdot 4 \cdot \pi \cdot 10^{-7}}{L}$
	$l_g = 3.369 \cdot 10^{-3}$

Total air gap = 3.4 mm

Mean length of turn = 9.7 cm	
Coil ESR in ohm	$R_s := 41.3 \cdot 10^{-6} \cdot N \cdot 9.7$

$$R_s = 0.025$$

ESR = 0.025 ohm

Copper loss = 1.6 W

Copper loss Pcl	$P_{cl} := I_{rms}^2 \cdot R_s$
	$P_{cl} = 1.59$

Check for max. flux density	$B_{ma} := \frac{4 \cdot \pi \cdot 10^{-7} \cdot N \cdot I_p}{l_g}$	$B_{ma} = 0.277$
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APPENDIX - C

ANALYSIS AND DESIGN OF THE CURRENT LOOP

Inputs

$V_{rms} := 110$	Input rms voltage
$W := 200$	Define Operating output power
$V_{dc} := 180$	Output voltage (dc)
$L := 700 \cdot 10^{-6}$	Total boost inductance
$C := 1000 \cdot 10^{-6}$	Output (dc side) filter capacitance
$D := 0.8$	Duty ratio

Derived quantities

$V_{in} := \sqrt{2} \cdot V_{rms}$	Peak input voltage
$R := \frac{V_{dc}^2}{W}$	calculate load resistance
$L_e := \frac{L}{(1 - D)^2}$	

Transfer function of the power stage

$w(f) := 2 \cdot \pi \cdot f$	Generalized frequency in rad/sec
$s(f) := i \cdot w(f)$	define parameter s

$$G_b(f) := \frac{V_{dc}}{R \cdot (1 - D)^2} \cdot \frac{2 + s(f) \cdot C \cdot R}{1 + s(f) \cdot \frac{L_e}{R} + s(f)^2 \cdot L_e \cdot C}$$

Control transfer function for the power stage

Control circuit inputs

$R_{mo} := 10 \cdot 10^3$	Multiplier resistance
$R_{ci} := R_{mo}$	PI controller feedback resistance
$R_z := 33 \cdot 10^3$	PI controller feedback capacitance in series with R_z
$C_z := 47000 \cdot 10^{-12}$	PI controller feedback capacitance in series with R_z
$C_p := 880 \cdot 10^{-12}$	

Overall Transfer function

Calculate PI zero

$$wz := \frac{1}{Rz \cdot Cz}$$

$$fz := \frac{wz}{2 \cdot \pi} \quad fz = 102.614$$

$$wp := \frac{1}{Rz \cdot \frac{Cz \cdot Cp}{Cz + Cp}}$$

$$fp := \frac{wp}{2 \cdot \pi}$$

$$fp = 5.583 \cdot 10^3 \quad \text{PI pole}$$

$$Gcc(f) := \frac{1 + \frac{s(f)}{wz}}{s(f) \cdot Rci \cdot (Cz + Cp) \cdot \left(1 + \frac{s(f)}{wp}\right)}$$

PI controller transfer function

Peak Voltage of the timing capacitor

$$Vtc := 5.2$$

$$Rs := 0.1$$

H := Rs The current sense resistor is the feedback path gain

$$GL(f) := Gcc(f) \cdot \frac{1}{Vtc} \cdot Gb(f) \cdot H$$

Loop Transfer function

$$i := 10, 11 \dots 500 \quad f_i := 10^{\frac{i}{100}}$$

Plots of loop gain

$$MGcc(f) := 20 \cdot \log(|Gcc(f)|)$$

$$MGL(f) := 20 \cdot \log(|GL(f)|)$$

$$MGB(f) := 20 \cdot \log(|Gb(f)|)$$

$$PHGL(f) := (\arg(Gcc(f)) + \arg(Gb(f))) \cdot \frac{180}{\pi}$$

APPENDIX - D

ANALYSIS AND DESIGN OF THE VOLTAGE LOOP

Inputs

$V_{rms} := 110$	Input rms voltage
$W := 200$	Define Operating output power
$V_{dc} := 180$	Output voltage (dc)
$C := 2000 \cdot 10^{-6}$	Output (dc side) filter capacitance

Derived quantities

$V_{in} := \sqrt{2} \cdot V_{rms}$	Peak input voltage
$R := \frac{V_{dc}^2}{W}$	calculate load resistance
$k := \frac{V_{in}}{V_{dc}}$	The boost factor

Feed Forward section

$w(f) := 2 \cdot \pi \cdot f$	Generalized frequency in rad/sec		
$s(f) := i \cdot w(f)$	define parameters		
$R_{ff1} := 15 \cdot 10^3$	$R_{ff2} := 15 \cdot 10^3$	$C_{ff1} := 0.68 \cdot 10^{-6}$	$\omega_{ffp1} := R_{ff2} \cdot C_{ff1}$
$ffp1 := \frac{1}{2 \cdot \pi \cdot \omega_{ffp1}}$	$ffp1 = 15.603$	$R_{ff3} := 10 \cdot 10^3$	$C_{ff2} := 1 \cdot 10^{-6}$
$\omega_{ffp2} := R_{ff3} \cdot C_{ff2}$	$ffp2 := \frac{1}{2 \cdot \pi \cdot \omega_{ffp2}}$	$ffp2 = 15.915$	
$k_{ff} := \frac{R_{ff3}}{R_{ff1} + R_{ff2} + R_{ff3}} \cdot \frac{2}{\pi} \cdot \frac{12}{115}$			dc gain of the feedforward voltage
$V_{ff} := k_{ff} \cdot V_{in}$	$k_{ff} \cdot V_{in} = 2.584$		

$$G_{ff}(f) := \frac{1}{\left(1 + \frac{s(f)}{\omega_{ffp1}}\right) \cdot \left(1 + \frac{s(f)}{\omega_{ffp2}}\right)}$$

Control circuit inputs

$V_{ref} := 3$	As per UC 3854 data sheet
$H_v := \frac{V_{ref}}{V_{dc}}$	Feedback path gain

$$R_{ac} := 900 \cdot 10^3$$

Current reference resistor

$$I_{sine} := \frac{V_{in}}{R_{ac}}$$

Calculated operating reference current

$$R_{mo} := 10 \cdot 10^3$$

Multiplier resistance

$$R_s := 0.1$$

current sense resistor

Multiplier Section

$$\beta := 1$$

Multiplier constant of unity magnitude and unit of Voltage

$$G_m := \beta \cdot \frac{I_{sine}}{V_{ff}^2}$$

Multiplier Gain

Current loop

$$G_{cl} := \frac{R_{mo}}{R_s}$$

Power Circuit

$$G_{ps} := \frac{k}{2}$$

RC Load

$$G_{r\alpha}(f) := \frac{R}{1 + s(f) \cdot C \cdot R}$$

Voltage Controller

$$R_1 := 5.6 \cdot 10^3$$

$$R_2 := 22 \cdot 10^3$$

$$C_2 := 2.2 \cdot 10^{-6}$$

$$w_2 := \frac{1}{R_2 \cdot C_2}$$

$$f_2 := \frac{w_2}{2 \cdot \pi}$$

$$f_2 = 3.288$$

$$G_{vc}(f) := \frac{R_2}{R_1} \cdot \frac{1}{1 + \frac{s(f)}{w_2}}$$

Overall Loop gain

$$GL(f) := G_{vc}(f) \cdot G_m \cdot G_{cl} \cdot G_{ps} \cdot G_{r\alpha}(f) \cdot H_v$$

$$i := 100, 101 \dots 400$$

$$MGL(f) := 20 \cdot \log(|GL(f)|)$$

$$f_i := 10^{-2} \cdot 10^{\frac{i}{100}}$$

$$PHGL(f) := \arg(GL(f)) \cdot \frac{180}{\pi}$$

Output Impedance

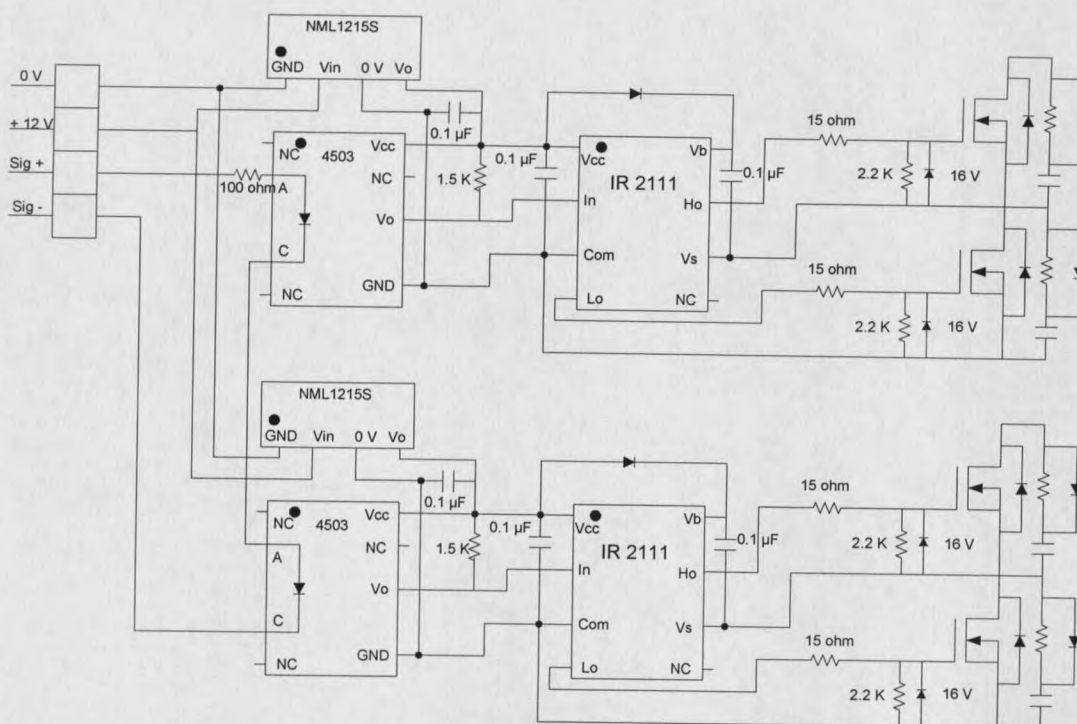
$$MOI(f) := \left| \frac{G_{r\alpha}(f)}{1 + GL(f)} \right|$$

Input susceptibility

$$MIS(f) := 20 \cdot \log \left[\left| \left(\frac{1 - 2 \cdot G_{ff}(f)}{1 + GL(f)} \right) \cdot G_m \cdot G_{cl} \cdot G_{ps} \cdot G_{r\alpha}(f) \right| \right]$$

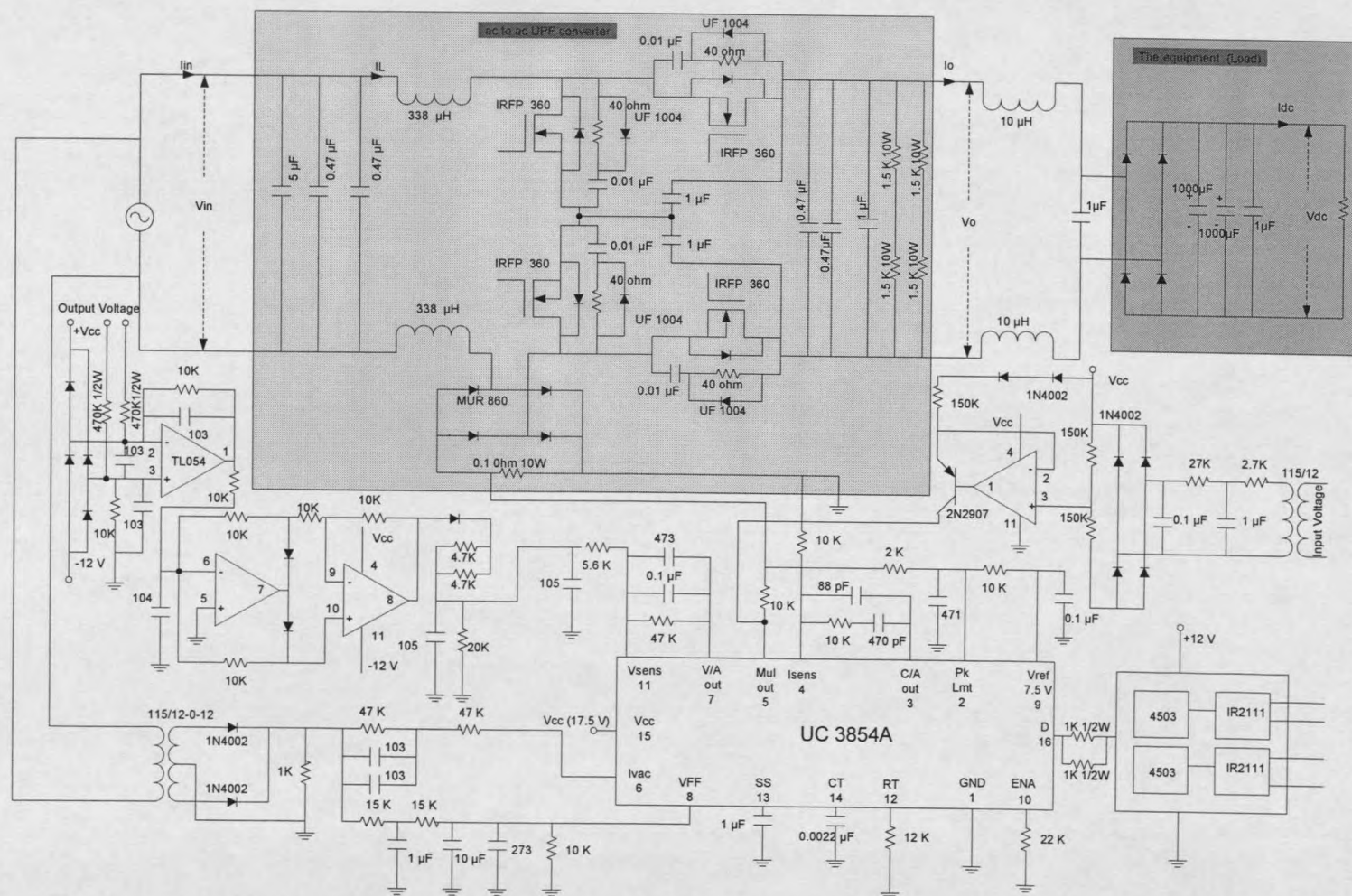
APPENDIX - E

SCHEMATIC OF THE DRIVE CIRCUIT



APPENDIX - F

SCHEMATIC OF THE CONTROL CIRCUIT



APPENDIX - G

STEADY STATE PERFORMANCE RESULTS AND INPUT CURRENT
HARMONICS

STEADY STATE PERFORMANCE RESULTS

Input							Output				Efficiency	
Voltage	Current	Power	Pf	Fund pf	THD	THD	Load	Voltage	Current	Power	Vdc	
V	A	W			V	A	setting	V	A	W		%
V _{in}	I _{in}						ohm	V	I _{dc}		V	
1. Personal computer load												
110	1.98	210	0.958	0.985	2.66	25	A	176	1.08	121	209	59.6762
110	2.8	290	0.948	0.979	2.48	27	A+B	165	1.72	214	203	73.7931
130	2.33	290	0.96	0.972	2.59	29	A+B	165	1.73	212	199	73.1034
90	3.5	303	0.966	0.987	2.62	21	A+B	163	1.95	225	199	74.2574
2. Personal computer load - Line regulation												
110	2.8	290	0.948	0.979	2.48	27	A+B	165	1.72	214	203	73.7931
80	3.88	308	0.971	0.988	2.69	20	A+B	164	1.86	218	201	70.7792
90	3.5	303	0.966	0.987	2.62	21	A+B	163	1.95	225	199	74.2574
3. Rectifier Load - Load regulation												
110	1.91	210	0.972	0.984	2.91	16	300	173	1.26	166	199	79.0476
112	2.27	248	0.976	0.986	2.81	14	220	171	1.6	205	192	82.6613
110	2.86	330	0.98	0.987	2.84	13	140	164	1.88	259	181	78.4848
110	4.09	445	0.984	0.988	2.8	11	73	182	7	359	162	80.6742
4. Resistive Load												
110	3.58	391	0.988	0.991	2.81	8.4	57	139	2.43	336	139	85.9335
110	4.76	518	0.988	0.991	2.85	8.2	33	122	3.71	444	121	85.7143

A and B are identical micron computers model AL440-LX-PII300-CR

INPUT CURRENT HARMONICS

Harmonic number	Percentage harmonics	Harmonic number	Percentage harmonics
DC	2.61	21	4.6
2	0.52	22	0.22
3	9.1	23	3.75
4	0.22	24	0.37
5	8.1	25	0.33
6	0.4	26	0.48
7	5.01	27	3.47
8	0.34	28	0.54
9	6.1	29	3.63
10	0.53	30	0.55
11	6.23	31	3.89
12	0.38	32	0.72
13	6.33	33	3.95
14	0.49	34	0.47
15	6.1	35	4.25
16	0.3	36	0.82
17	5.1	37	3.71
18	0.39	38	0.42
19	4.45	39	3.59
20	0.31	40	0.6

These results are for 110 V input voltage
and two Micron computers as load.

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