Synthesis techniques useful in the generation of precise microwave frequencies
by Kenneth Eugene Marcotte

A thesis submitted to the Graduate Faculty in partial fulfillment of the requirements for the degree of DOCTOR OF PHILOSOPHY in 4 Electrical Engineering
Montana State University
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Abstract:
The general principles of direct and indirect methods of frequency synthesis are described. Signal operations of frequency translation, multiplication and division are analyzed and degradation of the input signal stability is discussed.

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2. The analysis of a broadband frequency divider using a Step Recovery diode is presented. The divider executes subharmonic oscillations of order 1/2 and has an operational bandwidth greater than an octave in frequency. Graphs showing performance characteristics are presented.

3. A ring modulator is described using broadband transformer coupling and matched Hot Carrier diodes to perform frequency translation through 1 GHz.

Experimental data presented for the VHF and lower UHF frequency range appears to confirm the analyses of the various signal operations under investigation.

SYNTHESIS TECHNIQUES USEFUL IN THE GENERATION OF PRECISE MICROWAVE FREQUENCIES

by

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A thesis submitted to the Graduate Faculty in partial fulfillment of the requirements for the degree

of

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in

Electrical Engineering

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ABSTRACT

The general principles of direct and indirect methods of frequency synthesis are described. Signal operations of frequency translation, multiplication and division are analyzed and degradation of the input signal stability is discussed.

Synthesis techniques which have application in the VHF and UHF frequency ranges under investigation are presented as follows:

1. Several broadband frequency multiplication techniques employing the Hot Carrier and Step Recovery diodes are analyzed. Graphs showing performance characteristics allow prediction for wide ranges of circuit parameters and input and output operating frequencies.

2. The analysis of a broadband frequency divider using a Step Recovery diode is presented. The divider executes subharmonic oscillations of order 1/2 and has an operational bandwidth greater than an octave in frequency. Graphs showing performance characteristics are presented.

3. A ring modulator is described using broadband transformer coupling and matched Hot Carrier diodes to perform frequency translation through 1 GHz.

Experimental data presented for the VHF and lower UHF frequency range appears to confirm the analyses of the various signal operations under investigation.

1.0 STATEMENT OF THE PROBLEM.

Frequency synthesis is the generation of sinusoidal rf signals of a desired frequency from a frequency standard in such a manner that the accuracy and stability of the derived frequency is not seriously degraded from that of the standard. Modern communication systems and precision laboratory measurement techniques in many different fields require signal sources which possess this frequency precision and stability. Electronic circuits and system techniques for use in solving the specific frequency synthesis requirement are fairly well known for the frequency range of a few cycles per second to several hundred megacycles per second [1-7]. This is not the case for the lower UHF and microwave frequencies. This study treats several synthesis techniques which have direct application in the VHF, UHF, and microwave frequency ranges.

This thesis is divided into six chapters. The statement of the problem and a discussion of techniques to be investigated for application in frequency synthesis systems are presented in Chapter 1.

The system concept of a frequency synthesizer is presented in Chapter 2. The significant differences in the overall system operation are discussed with the aid of several block diagrams of typical direct and indirect synthesis methods.

In Chapter 3 signal operations, which are used in either the direct or indirect synthesis methods, are analyzed. These operations are frequency translation, multiplication and division. The purpose

of this chapter is to investigate the input signal stability degradation in the output signals with reference to input as the signal operations are performed.

The basic operating principles and analysis of techniques of performing a desired signal operation are presented in Chapter 4. Many authors have described the various performance characteristics of several of the techniques under investigation, but no one of these has treated the data presentation in a manner with sufficient depth for the general design situation. In these cases theoretical computations have been carried out and the results presented in a manner which is felt presents a much broader scope. These presentations allow performance prediction for wide ranges for variation of circuit parameters, of operating characteristics and of input or output operating frequencies. The analysis presented formulates the basic operational limitations regarding the signal operation being considered, and gives the basis by which experimental results of implemented operation may be compared.

In Chapter 5 the design, implementation and testing of the techniques analyzed in Chapter 4 are carried out to determine the performance capabilities of the practical realization.

In Chapter 6 the summary and conclusions are presented. Several specific application of the investigated signal operation techniques are discussed. Suggestions for further research investigations are

also presented.

2.0 FREQUENCY SYNTHESIS

When crowding of the frequency spectrum was not a problem and frequency inaccuracies could be tolerated, the tunable L-C oscillator was a practical means of providing the required channel frequencies for various multi-channel equipment. Crowding of the spectrum required closer channel spacing and increased frequency accuracy. The crystal oscillator was used to satisfy this required increased frequency accuracy. The multiple-crystal synthesizer was developed to satisfy the requirements of multi-channel equipment. The single crystal frequency synthesizer was proposed to fulfill the accuracy and stability requirement in equipment covering a very large number of communication channels.

The single crystal frequency synthesizer retains the properties of the multiple crystal synthesizer and at the same time eliminates the problem of maintaining a large number of crystals to the same accuracy. The accuracy and stability of the output signal are essentially equal to that of the reference oscillator.

Present day frequency synthesizers, regardless of the synthesis scheme used, have the common objective of referencing all generated frequencies to a single standard frequency. This single standard frequency is generated by an extremely accurate and stable oscillator. The required output frequencies are obtained in some synthesis procedure by direct multiplication and division of the standard frequency, which are combined by the operation of either addition or

subtraction to give the derived output frequency. In other schemes, the final output frequency is compared directly or divided down to a frequency which can be compared with the standard frequency. The comparator output furnishes the control signal for locking the output signal to the standard.

Synthesizers can be divided into two main categories. These are termed direct and indirect. Mixing of a set of frequencies derived directly from the standard to obtain the final specific output frequency is defined as direct synthesis. Methods which ultimately control the output of a phase-locked oscillator are defined as indirect synthesis. The common characteristic regardless of the synthesis method employed is to generate a desired frequency from a frequency standard in such a manner that the stability and accuracy of the derived frequency is not seriously degraded from that of the standard. The multiplicity of output signals available are all harmonically related to a specific subharmonic of the standard oscillator.

2.1 DIRECT FREQUENCY SYNTHESIS.

For frequency generating systems that are classed as direct synthesis the general principles of operation can be illustrated as in Fig. 2-1. From this block diagram it is clear that the output frequency is related to a subharmonic of the reference oscillator.

The selection of positive integers a and b will determine the sub-harmonic spacing between available output frequencies.

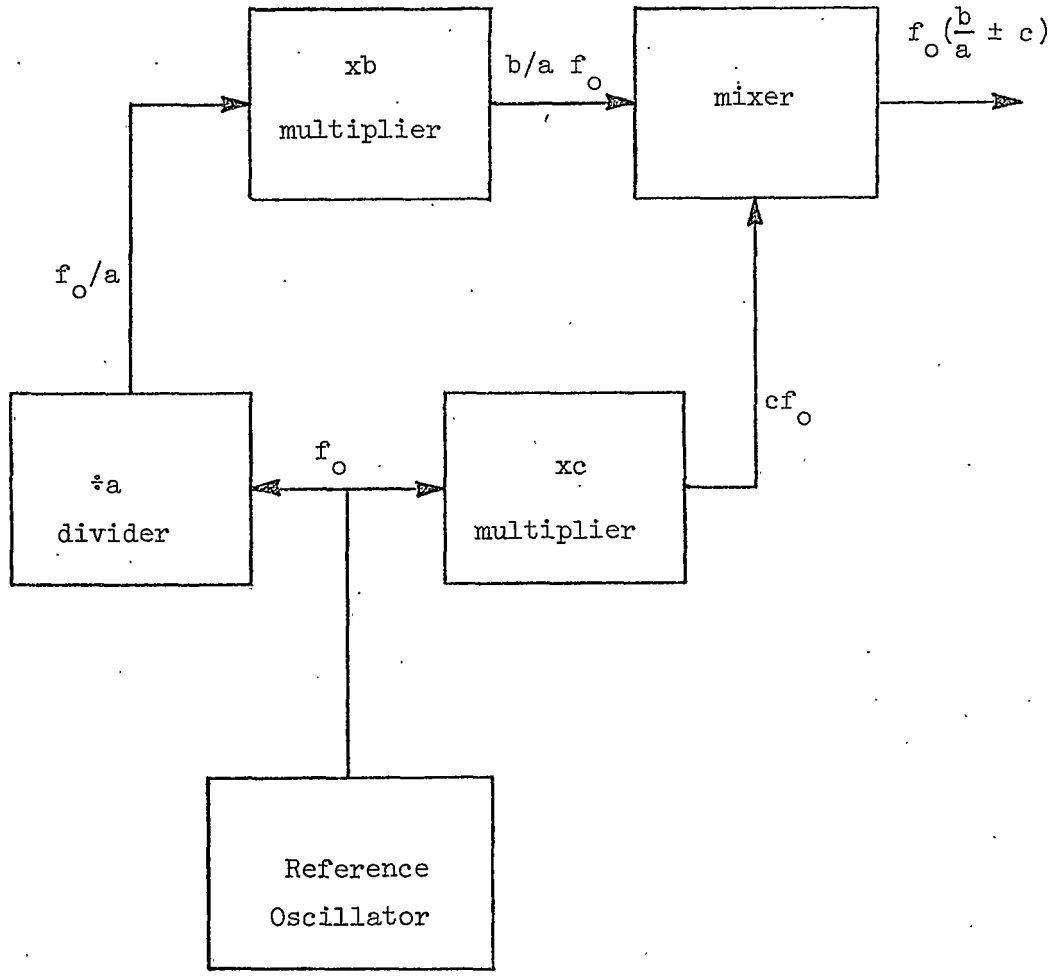


Fig. 2-1. BLOCK DIAGRAM OF DIRECT FREQUENCY SYNTHESIS.

In the actual system realization of a synthesizer using this method to obtain many possible output frequencies, a highly stable reference oscillator with multiples and sub-multiples are mixed in elaborate ways to produce the desired outputs. A more general block diagram, which indicates the complexity that may be involved in generating a set of output frequencies for a given application, is illustrated in Fig. 2-2.

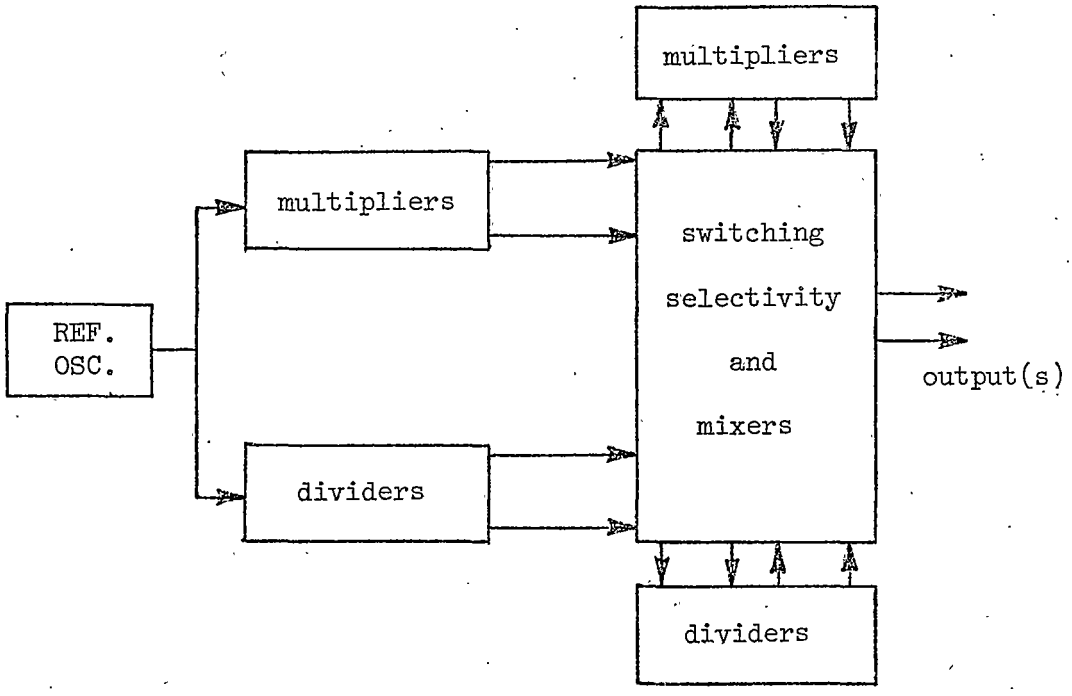


Fig. 2-2. GENERAL BLOCK DIAGRAM FOR DIRECT FREQUENCY--SINGLE SOURCE SYNTHESIZERS.

The synthesizer of least system complexity would consist of multipliers and dividers directly connected to the reference oscillator and their outputs used to generate the desired output frequencies. The next level of system complexity would be several parallel multiplier-divider combinations to generate the desired outputs. The complexity can be continued on to the multipliers and dividers that are not directly connected to the reference oscillator.

The majority of synthesizer equipments that have been built fall under this category. These systems typically provide 1 to 50 million frequencies that are manually selectable.

2.2 INDIRECT FREQUENCY SYNTHESIS.

For frequency generating systems that are classed as indirect synthesis, a controlled oscillator feeds the output terminals of the synthesizer directly. The frequency of the output oscillator is continuously monitored and compared to a reference frequency, and automatic adjustment of the oscillator frequency is made to maintain its output at precisely the desired frequency.

As in the direct synthesis class, this discussion cannot include all the many types of synthesizers that have been developed in the indirect synthesis category. Two examples have been selected that include a wide cross-section of the systems in this class.

The automatic phase control (APC) method of frequency synthesis

is presented in Fig. 2-3. This system is an electronic servo that does not permit a steady-state frequency error to be developed between the reference frequency and the voltage controlled oscillator (VCO).

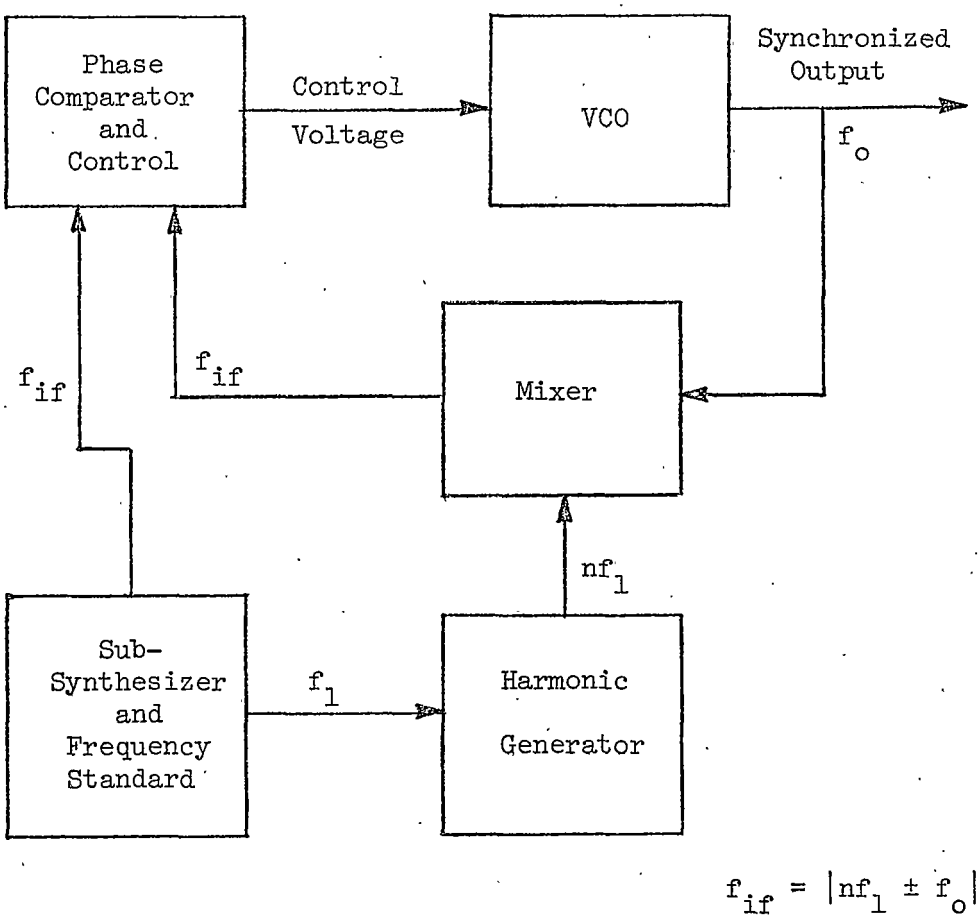


Fig. 2-3. AUTOMATIC PHASE CONTROL SYSTEM BLOCK DIAGRAM.

The VCO output is mixed with a harmonic of the sub-synthesizer output f_1. This produces an intermediate frequency signal f_{if} which is compared in the phase comparator with f_{if} from the sub-synthesizer. The comparator output is a voltage proportional to the phase error of the converted f_{if} signal to the synthesizer f_{if} signal. The comparator output is passed to the control circuitry of the VCO.

The APC system holds the VCO on frequency by varying the control voltage so that the two f_{if} signal frequencies are identical but, in general, differing in phase. This overall operation provides a frequency lock for $f_o = |nf_1 \pm f_{if}|$.

Figure 2-4 illustrates an example of digital method of indirect frequency synthesis. The output of the VCO is divided by n and fed to the phase comparator.

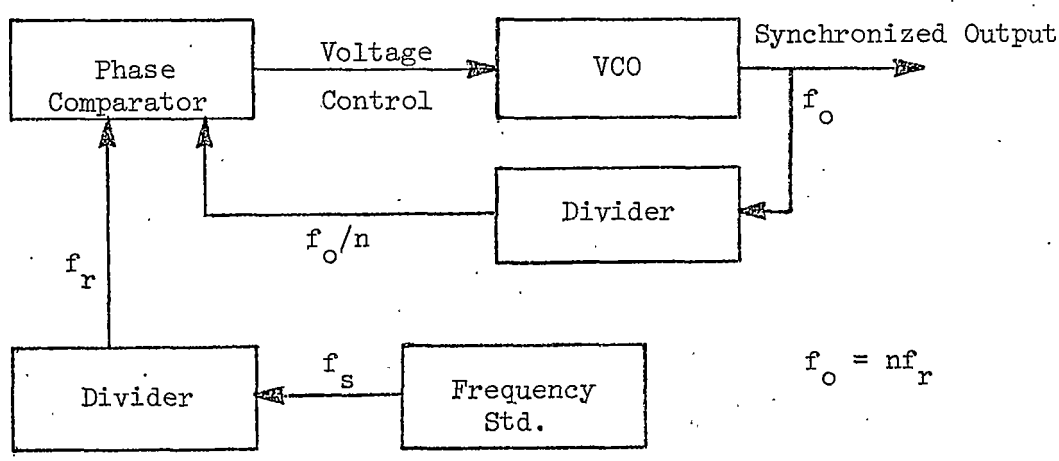


Fig. 2-4. DIGITAL FREQUENCY SYNTHESIS BLOCK DIAGRAM.

The comparator has the divided reference frequency, f_r, as the other input. The output of the phase comparator provides the VCO correction voltage if the two inputs are not identical in frequency. Therefore, the frequency of the VCO is automatically phase-locked to the reference standard.

2.3 SYNTHESIZER PERFORMANCE SPECIFICATIONS.

In general, the system application determines the performance and configuration of the synthesizer. The specific application will dictate several or all of the following performance specifications:

1) frequency coverage and resolution

2) method of frequency selection

3) speed of switching to desired output frequency

4) accuracy and stability

5) spectral purity.

The rf tuning range for a specified application (or equipment) in which the synthesizer is to be incorporated will in general set the frequency coverage needed. The system channel capability will determine the number of incremental frequencies required for communications applications.

Spectral purity is one of the more critical performance factors of a synthesizer. Complete spectral purity implies the absence of noise and spurious frequencies. In general the reference frequency

standard used to drive a synthesizer will be of resonable quality and possess an output signal power spectrum as shown in Fig. 2-5.

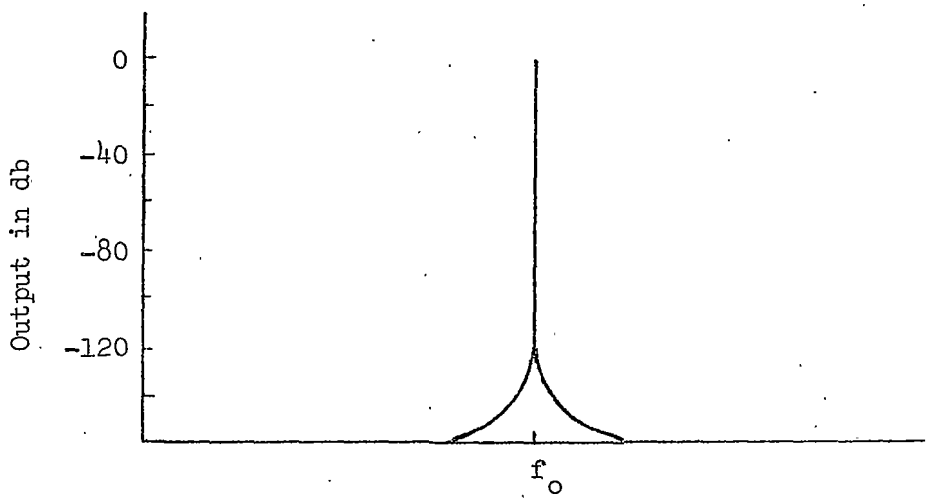


Fig. 2-5. OUTPUT SPECTRUM OF A FREQUENCY STANDARD.

The output signal of the frequency standard is specified by the harmonic distortion present, the non-harmonic related outputs, and the signal-to-noise ratio for a specific output signal bandwidth. Each of the quantities are specified in db. The db (decibel) measure is defined as

$$\text{number of db} = -10 \log \frac{P_o}{P_i}, \qquad (2\text{-}1)$$

where, for the specification of a frequency standard, P_o is the power at the output frequency f_o. For the harmonic distortion specification, P_1 is the power at each of the harmonics of f_o. For the

non-harmonic components, P_1 is the power at each of the spurious frequencies. For the signal-to-noise ratio P_1 is the total power associated with the specified output signal bandwidth.

A high order of spectral purity existing in the synthesizer output requires that noise and spurious frequency generation be kept to a minimum throughout the entire synthesis process. The spurious frequencies appearing in the synthesizer output are the result of either the filters used within the synthesizer presenting a finite attenuation (rather than infinite) to undesired frequency components or improper shielding of the various subsystems. In some cases the spurious outputs may be a combination of both the filtering and shielding problems. Spurious frequency generation coupled with a find incremental frequency resolution capability requires much greater system complexity.

Direct frequency synthesizers have been constructed which maintain the spurious component level at 90-100 db below the desired output signal levels. Indirect synthesizers, using filter time-constants up to 1 second in the control loop, have been able to obtain spurious levels greater than 100 db below the output level.

The stability of the synthesized outputs are dependent on both spurious levels and the frequency resolution.

In applications requiring fast switching between selected output frequencies, the design dictated is usually the direct method.

The required control loop filters in the indirect method limit their speed of response due to the bandwidth of the filter used.

2.4 SUMMARY

An attempt has been made to show that frequency synthesizer designs evolve from a few basic signal operations. The signal operations are frequency translation, frequency multiplication and frequency division. The grouping of these signal operations may be performed in a wide variety of combinations depending upon the specific system requirement. By skillful choice of operations, systems may be designed for a given application with an accuracy limited only by the primary reference oscillator.

3.0 SIGNAL REPRESENTATIONS AND OPERATIONS APPLICABLE TO FREQUENCY SYNTHESIS.

The basic signal operations that must be combined to describe a specific frequency synthesizer of the two broad classes discussed in Chapter II are frequency translation, frequency multiplication and frequency division. In all these operations the prime concern is minimum degradation of the initial standard short-term stability while performing the desired operation. These signal operations are defined and their theoretical performance criteria set down. This then will form the basis to which actual circuit performance can be compared.

3.1 SIGNAL REPRESENTATION

The signal and noise which the basic standard delivers at the output terminals is the input signal for the various signal operations considered. This signal is assumed to have a large signal-to-noise ratio along with a very narrow output signal bandwidth. It is assumed that the standard has been in operation for a sufficient length of time such that the start-up transients of the standard can be neglected. Also, the long-term effects of frequency drift in the standard output due to component drifts from aging or temperature fluctuations will not be considered in this analysis. These long-term effects can be eliminated by appropriate control of the standard. As in any system there exist possible transient responses

along with the normal steady-state response for the signal operations being analyzed. The analysis that follows is concerned only with the steady-state response.

For the stated assumptions the signal being generated by the standard can be expressed as

$$s(t) = A \cos \omega_o t. \tag{3-1}$$

and the noise being considered expressed as

$$v_n(t) = v_c(t) \cos \omega_o t + v_s(t) \sin \omega_o t. \tag{3-2}$$

where

A = fixed amplitude

ω_o = standard output frequency

$v_c(t)$ and $v_s(t)$ are both narrow-band random processes which are slowly varying functions compared to the individual cycles of $s(t)$. A detailed discussion leading to equation (3-2) may be found in reference [8].

The result of adding signal and noise to obtain the output signal delivered by the standard is

$$v_1(t) = s(t) + v_n(t) \tag{3-3}$$

Substituting (3-1) and (3-2) into (3-3) yields

$$\begin{aligned} v_1(t) &= (A + v_c(t)) \cos \omega_o t + v_s(t) \sin \omega_o t \\ &= B(t) \cos (\omega_o t + \phi(t)). \end{aligned} \tag{3-4}$$

where

$$B(t) = \sqrt{(A + v_c(t))^2 + v_s(t)^2} \tag{3-5}$$

and

$$\tan \phi(t) = \frac{v_s(t)}{A+v_c(t)} . \tag{3-6}$$

For large signal-to-noise ratios

$$\phi(t) \tilde{=} A^{-1} v_s(t) \tag{3-7}$$

Equation (3-4) to (3-7) specify the input signal to be used in the analysis of the signal operations presented in this Chapter. A complete model of the standard, setting down the mechanisms by which it generates this output signal, has not been described. The signal and noise that it delivers to the next element of the system is the oscillator feature of interest.

3.2 FREQUENCY TRANSLATION.

Frequency translation has been used for many years, but the general problem of spurious frequency generation has often been treated lightly or ignored. In this section some of the general properties of frequency translation including the generation and suppression of spurious frequencies is discussed.

3.2.1. GENERAL TRANSLATION

Mixers with filtering perform the function of frequency translation in a signal chain. Mixing is essentially a modulation

in which one signal is modulated by another signal producing the lower and upper side frequency components. Mixing action is achieved by means of a non-linear device and thus many frequency components may be present in the output of the mixer circuit. The operating parameters of the mixer stage will determine the ratio of the desired output(s) power level to the undesired outputs.

Frequency translation is in general accomplished by multiplying the signal to be translated by a sinusoidal signal of appropriate frequency to provide the desired translation. For the ideal case, consider $v_2(t)$ in Fig. 3-1 to be given by

$$v_2(t) = \cos \omega_2 t. \tag{3-8}$$

Then the output $v_o(t)$ is expressed as

$$v_o(t) = v_1(t) \cos \omega_2 t. \tag{3-9}$$

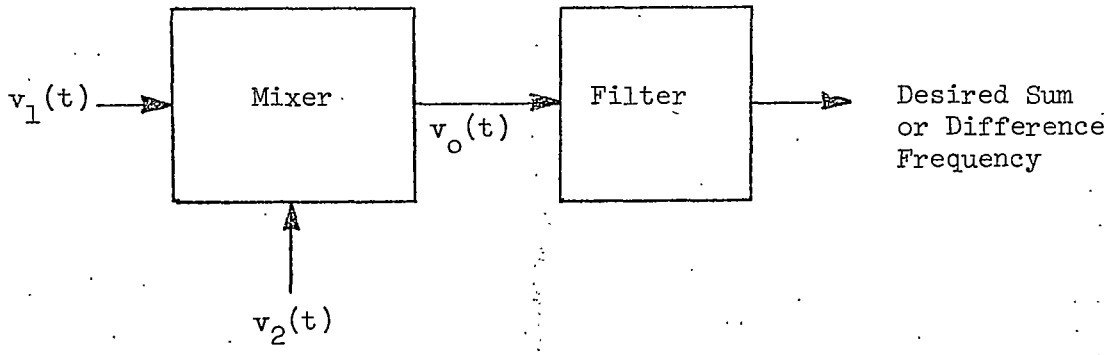


Fig. 3-1. FREQUENCY TRANSLATION.

Fourier analysis shows that this process translates the input frequency ω_1 or an input frequency spectrum by an amount $\pm \omega_2$. For a single input frequency, ω_1, the frequencies existing in the output are given by

$$\omega_o = \omega_1 \pm \omega_2. \qquad (3\text{-}10)$$

The desired sum or difference frequency is selected by filtering.

3.2.2 GENERAL MIXER

As previously stated, mixing action is fundamental to the process of frequency translation and is accomplished by use of a nonlinear device; as a result, modulation products in the output will exist and many frequencies other than $\omega_1 \pm \omega_2$ along with possible additional spurious responses at ω_o. Considering a general nonlinear mixer, the output $v_o(t)$ may be expressed as

$$v_o(t) = \sum_{m=o}^{\infty} \sum_{n=o}^{\infty} a_{mn} \cos (m\omega_1 t \pm n\omega_2 t + \phi_{mn}) \qquad (3\text{-}11)$$

where

a_{mn} = constant

ϕ_{mn} = constant phase shift

Spurious responses are generally produced with signals existing at undesired frequencies which satisfy the following condition

$$f_o = |mf_1 \pm nf_2| \qquad (3\text{-}12)$$

where

f_1 = signal frequency

f_2 = translation frequency

f_o = desired output frequency

m and n are integers ≥ 1.

The choice of frequencies which are to be used in the translation scheme depend on several factors. This dependence in all cases relies on how well the extraneous signal can be rejected in the output of the mixer. Several means are available to aid in accomplishing the required rejection such as narrow-band filters, frequency spacing, and an effective cancellations of many components by balancing techniques. In the desired translation case the frequency of translation and the sets of harmonic sum and difference components do not fall within the output bandwidth of the mixer. In these cases the required extraneous signal rejection is provided by the filter response in the mixer output. In the cases where the translation signal frequency falls in the output signal bandwidth, balancing is required to eliminate these components. The next two sections describe unbalanced and balanced mixers.

3.2.3. SINGLE DIODE MIXER

The single diode mixer will be presented in terms of solid state diode mixers in that the conversion conductance analysis

applies directly. The analysis can be extended to the transistor mixer by considering a diode mixer followed by a transistor amplifier. Then the conversion gain is the sum of the diode conversion loss at the linear signal frequency and the transistor gain at the desired output frequency.

The high conductance of a diode in the forward direction and very low conductance in the reverse direction provides the necessary non-linearity for mixing. The dc voltage-current characteristics of the diode is expressed as

$$i(t) = I_o \left[e^{\alpha(v(t)+V_o)} - 1\right]$$

$$= \sum_{k=o}^{\infty} a_k v(t)^k \qquad (3\text{-}13)$$

where V_o is the dc bias voltage, a_k is related to the diode conductance, and $v(t)$ is the total instantaneous ac voltage across the junction. Therefore, no diode mixer is truly piecewise linear nor truly square law in its operation. The commonly used diode is an exponential law mixer.

The exponential expression expanded as a Taylor series yields

$$i(t) = a_o + a_1 v(t) + a_2 v^2(t) + a_3 v^3(t) + \ldots \qquad (3\text{-}14)$$

The output voltage for a conventional mixer, Fig. 3-2, is equal to the diode current times the load resistance. The voltage, $v(t)$, is the sum of the translating and signal voltages,

$v_1(t)$ and $v_2(t)$.

Applying $v_1(t) = A_1 \sin \omega_1 t$ and $v_2(t) = A_2 \sin \omega_2 t$ to the mixer, the current expression for $v(t) = v_1(t) + v_2(t)$ becomes

$$\begin{aligned} i(t) &= a_o + a_1 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t) \\ &\quad + a_2 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^2 \\ &\quad + a_3 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^3 \\ &\quad + \cdots \\ &= a_o + a_1 A_1 \cos \omega_1 t + a_1 A_2 \cos \omega_2 t \\ &\quad + \frac{a_2 A_1^2}{2} + \frac{a_2 A_2^2}{2} + \frac{a_2 A_1^2}{2} \cos 2\omega_1 t \\ &\quad + \frac{a_2 A_2^2}{2} \cos 2\omega_2 t \\ &\quad + a_2 A_1 A_2 \cos (\omega_1 + \omega_2) t \\ &\quad + a_2 A_1 A_2 \cos (\omega_1 - \omega_2) t \\ &\quad + \cdots \end{aligned} \tag{3-15}$$

If equation (3-14) contains high order terms then the diode current expression (3-15) will have components associated with the harmonic sum and difference frequencies.

In the output of the mixer for the case $a_n \neq o$ for $n > 2$, the frequency components present are ω_1, ω_2, $\omega_1 \pm \omega_2$, $m\omega_1$, $n\omega_2$, $m\omega_1 \pm n\omega_2$ (m and n are integers).

The signal-to-noise ratio of this mixer with an ideal translating signal and coefficients higher than a_2 being zero will be

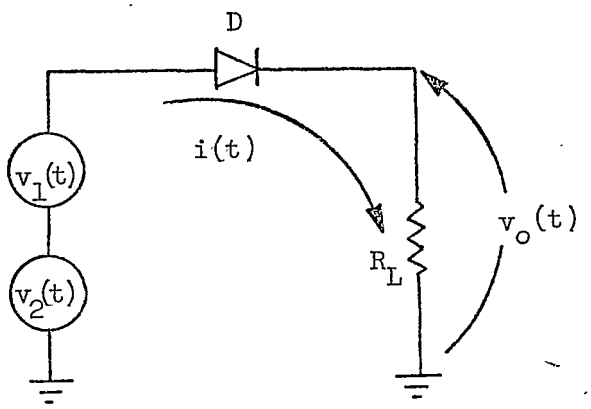


Fig. 3-2. CONVENTIONAL MIXER.

that of the signal input. However, if even ordered coefficients greater than a_2 are not zero then the output signal-to-noise ratio will be degraded since these products fall in the desired output bandwidth and therefore cannot be removed by filtering.

3.2.4 BALANCED MIXERS

The single diode mixer discussed generates a large number of spurious products. Suppression of the signal and translation frequencies along with some of the harmonic differences generated is desired. Two types of balanced mixers, generally called full lattice and half lattice, are commonly employed to meet these requirements. The half lattice modulator allows suppression of only one of the injected signals. The full lattice or ring modulator

allows suppression of both injected signals and their harmonics. However, some harmonic sum and difference components still remain.

The half lattice modulator can be represented as shown in Fig. 3-3.

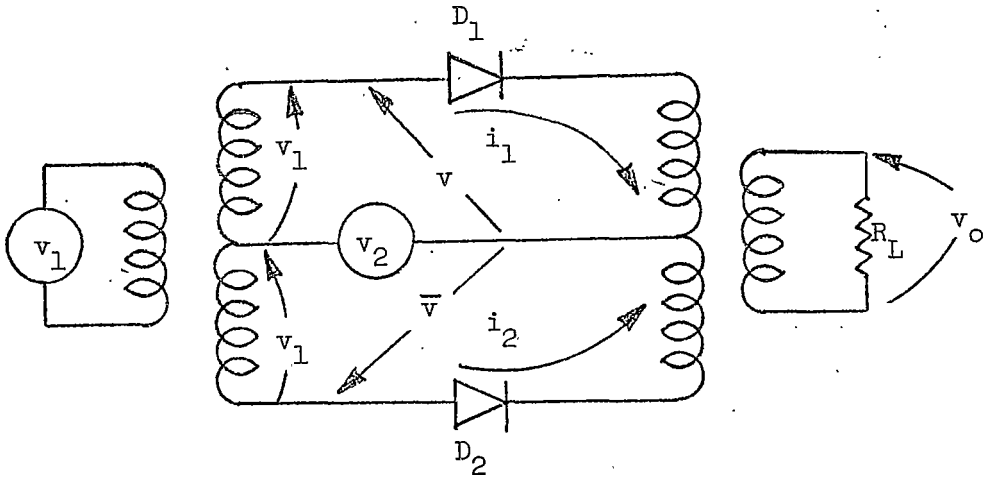


Fig. 3-3. HALF LATTICE BALANCED MODULATOR.

Assuming balanced diodes and transformers the output currents $i_1(t)$ and $i_2(t)$ are expressed as

$$i_1 = a_o + a_1 v + a_2 v^2 + a_3 v^3 + \ldots$$

$$i_2 = a_o + a_1 \bar{v} + a_2 \bar{v}^2 + a_3 \bar{v}^3 + \ldots \qquad (3\text{-}16)$$

where

$$v = v_1 + v_2$$

$$\bar{v} = -v_1 + v_2.$$

These voltages and currents are all functions of time as was the case in the single diode analysis. The notation has been changed merely for simplicity. The modulator output across R_L is given by

$$\begin{aligned} v_o &= (i_1 - i_2)\, R_L \\ &= R_L\, (2a_1\, v_1 + 4a_2\, v_1\, v_2 + 2a_3\, v_1^3 \\ &\quad + 6a_3\, v_1\, v_2^2 + 8a_4\, v_1^3\, v_2 \\ &\quad + 8a_4\, v_1\, v_2^3 + \ldots) \end{aligned} \tag{3-17}$$

As before, if we consider only coefficients a_o, a_1, and a_2, we obtain the desired translation, $\omega_1 + \omega_2$, with no degradation in the signal-to-noise ratio at the output. The even harmonics of ω_1 and all harmonics of ω_2 have been cancelled out. For the general case, $a_n \neq o$ for $n > 2$, the frequency components present are ω_1, $\omega_1 \pm \omega_2$, $n\omega_1$, $m\omega_2 \pm n\omega_1$ (m an integer and n an odd integer). As in the single diode case, the signal-to-noise ratio will be degraded if the even ordered coefficients greater than a_2 are not zero.

The double balanced ring or full lattice modulator is shown in Fig. 3-4. Using the same analysis as used for the half lattice modulator and balanced transformers and diodes the load currents are those of the previous modulator plus two additional currents associated with the reversed polarity diodes D_3 and D_4. The load currents due to the addition of these diodes are

$$i_1' = a_o - a_1 v + a_2 v^2 - a_3 v^3 + a_4 v^4$$

$$i_2' = a_o - a_1 v + a_2 v^2 - a_3 v^3 + a_4 v^4 \qquad (3\text{-}18)$$

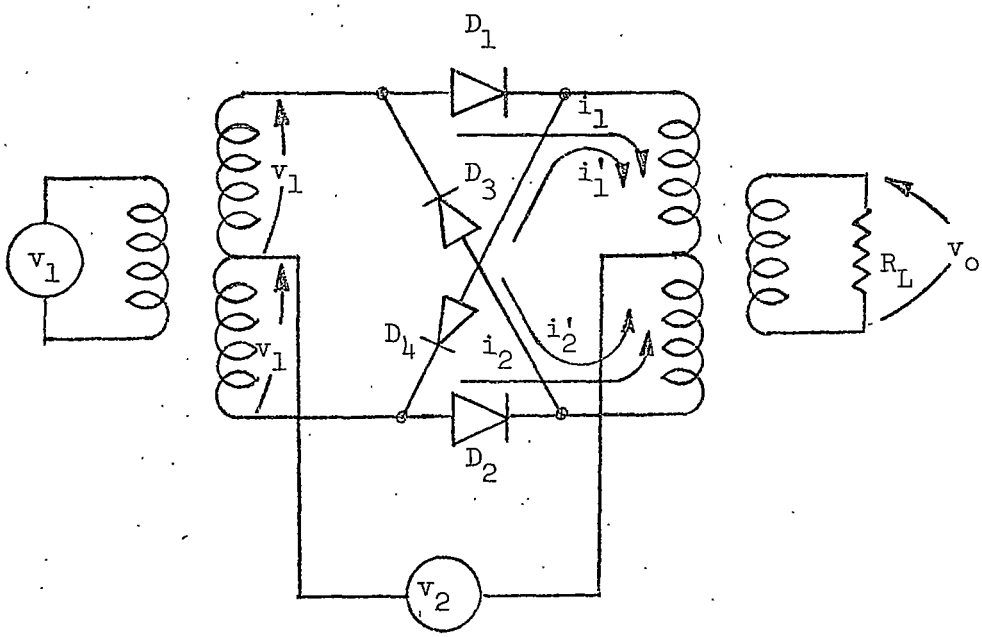


Fig. 3-4. RING MODULATOR.

The negative signs are the result of reversing the polarity and cross-connection of the additional diodes. These current equations are obtained by substituting in equation (3-16) $-v$ and $-\overline{v}$ for v and $\overline{v}$ respectively.

The output voltage associated with these currents is

$$(i_1' - i_2') R_L = R_L [-2a_1 v_1 + 4a_2 v_1 v_2 - 2a_3 v_1^3 - 6a_3 v_1 v_2^2 + 8a_4 v_1^3 v_2 + 8a_4 v_1 v_2^3 + \ldots] \quad (3\text{-}19)$$

The output voltage for the ring modulator is obtained by adding equations (3-17) and (3-19) which yields

$$v_o = R_L [8a_2 v_1 v_2 + 16a_4 v_1^3 v_2 + 16a_4 v_1 v_2^3 + \ldots] \quad (3\text{-}20)$$

Considering coefficients a_o, a_1, and a_2, we obtain the desired translation $\omega_1 \pm \omega_2$ with the cancellation of the two input signal frequency components. For the general case, $a_n \neq o$ for $n > 2$, the components present in the modulator output are $m\omega_2 \pm n\omega_1$ (m and n odd integers).

A comparison of the spurious products in the output of the several mixers discussed clearly points out the advantage of the ring modulator.

The statement was made regarding the various mixer circuit configuration considered as to a reduction of the input signal-to-noise ratio in the mixer output if the even order coefficients greater than a_2 were not zero. This can be easily checked by considering a higher order expansion and using equation (3-4) as the expression for the input signal and assuming a noise-free, sinusoidal translation signal at frequency f_2. It will be found that the noise level is increased for the condition of a higher order transfer function than a_2. In Appendix A the short-term frequency stability of a signal is

related to the existing signal-to-noise ratio. This relationship provides a means for determining the effects on the stability for a given decrease in the mixer output signal-to-noise ratio. The common definition of short-term stability (for measurement interval τ) is used in the derivation of Appendix A. Short-term stability is the ratio of the rms frequency deviation in the measurement time to the nominal frequency.

The relationship between the fractional frequency stability and the signal-to-noise ratio is given by

$$S = \frac{1}{\omega_o} \left[\frac{W_1}{(SNR)_1 \tau} + \frac{1}{(SNR)_2 \tau^2} \right]^{1/2} \qquad (3\text{-}21)$$

where

ω_o = Midband angular frequency

$(SNR)_1$ = Signal-to-noise associated with memory type (Type 1) noise in the mixer output.

$(SNR)_2$ = Signal-to-noise associated with non-memory type (Type 2) noise in the mixer output.

τ = Measurement interval.

W_1 = Bandwidth of the type 1 noise.

Memory noise (Type 1) is associated with noise generated within the oscillator generating the signal to be translated. Non-memory noise (Type 2) is associated with noise which originates between the

basic oscillator and the oscillator unit output terminals. The mixer will not be able to distinguish between the two types of noise and both signal-to-noise ratios in the mixer output will be reduced by the same amount.

3.3 FREQUENCY MULTIPLICATION.

In this section the general properties of an ideal frequency multiplier are discussed. It will be pointed out that the fractional frequency stability in the output of the ideal frequency multiplier is the same as the stability of the input signal.

Consider a device whose input-output relationships are as shown in Fig. 3-5, with the input $v_1(t)$ and output $v_2(t)$. Consider an input, $v_1(t)$, to the multiplier of the form

$$v_1(t) = A \cos \omega_o t, \tag{3-22}$$

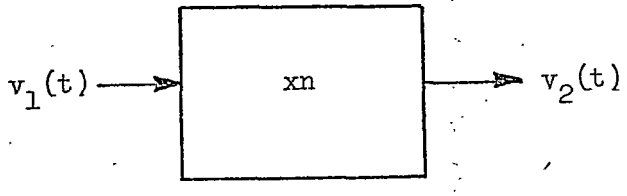


Fig. 3-5. IDEAL FREQUENCY MULTIPLIER.

Then the output of the frequency multiplier is

$$v_2(t) = A' \cos n\omega_o t, \tag{3-23}$$

where

A' = fixed amplitude related to A by a constant (A' = kA)

n = desired harmonic (integer > 1)

The means of obtaining the desired frequency multiplication under consideration here is that of employing a nonlinear device. The input signal is applied to the nonlinear device to generate the n^{th} harmonic of the input frequency ω_o. The input-output relationship of the device is expressed as

$$v_2(t) = a_n [v_1(t)]^n, \tag{3-24}$$

where

a_n = constant of the device

n = desired harmonic

Consider an input, $v_1(t)$ to this multiplier as given by

$$v_1(t) = A \cos \omega_o t \tag{3-25}$$

Then the output from the frequency multiplier is

$$v_2(t) = a_n [A \cos \omega_o t]^n. \tag{3-26}$$

The n^{th} harmonic terms at the output is

$$v_{2n}(t) = \frac{a_n A^n}{2^{n-1}} \cos n\omega_o t. \tag{3-27}$$

Now let the input signal also contain a noise voltage as discussed in Sec. 3.1, and given by (3-4). The output of the multiplier as a result of adding signal and noise is

$$v_2(t) = a_n [(A + v_c(t)) \cos \omega_o t + v_s(t) \sin \omega_o t]^n. \tag{3-28}$$

The input signal-to-noise ratio to the multiplier must be very large if it is to yield a narrow spectrum after multiplication in frequency synthesis systems. Assuming a large signal-to-noise ratio the output of the multiplier neglecting the nonlineaer noise terms can be expanded and expressed as

$$v_2(t) = a_n [(A^n + nA^{n-1} v_c(t)) \cos {}^n\omega_o t + nA^{n-1} v_s(t) \cos^{n-1}\omega_o t \sin \omega_o t] \tag{3-29}$$

The n^{th} harmonic term at the output is

$$v_{2n}(t) = \frac{a_n A^{n-1}}{2^{n-1}} [A \cos n\omega_o t + nv_c(t) \cos n\omega_o t + nv_s(t) \sin n\omega_o t] \tag{3-30}$$

The signal-to-noise ratio at the output can be expressed from (3-30) as

$$(SNR)_o = \frac{A^2}{n^2 (\overline{v_c(t)^2} + \overline{v_s(t)^2})} = \frac{1}{n^2} (SNR)_i. \tag{3-31}$$

Where

$(SNR)_i$ = Signal-to-noise ratio at the input

$(SNR)_o$ = Signal-to-noise ratio at the output.

Thus the noise power has been increased by n^2, the multiplication factor squared, relative to the output signal power.

In Appendix A the fractional rms frequency deviation of an oscillator output signal is given as

$$S_\tau = \frac{1}{\omega_o}\left[\frac{W_1}{(SNR)_1\tau} + \frac{1}{(SNR)_2\tau^2}\right]^{1/2} \qquad (3\text{-}32)$$

The short-term stability of the output signal (after multiplication) can be expressed as

$$S_{\tau n} = \frac{1}{n\omega_o}\left[\frac{W_1}{(SNR)_{n1}\tau} + \frac{1}{(SNR)_{n2}\tau^2}\right]^{1/2} \qquad (3\text{-}33)$$

where

$(SNR)_{n1}$ = Signal-to-noise ratio associated with memory type noise in multiplier output

$(SNR)_{n2}$ = Signal-to-noise ratio associated with non-memory type noise in multiplier output.

Since the multiplier will not be able to distinguish between input noise sources both signal-to-noise ratios will be decreased by the square of the multiplication factor. Thus, (3-33) becomes

$$S_{\tau n} = \frac{1}{n\omega_o} \left[\frac{n^2 W_1}{(SNR)_1 \tau} + \frac{n^2}{(SNR)_2 \tau^2} \right]^{1/2} \qquad (3\text{-}34)$$

which reduces to

$$S_{\tau n} = S_\tau .$$

Therefore, the ideal multiplication process does not alter the input oscillator stability.

It is shown in the Appendix B that for a higher order transfer characteristic than required, the output signal-to-noise ratio is degraded more than that of the n^{th} order characteristic discussed here. It is shown there that the orders contributing to this degradation are the a_{n+2j} for $j > 0$.

3.4 FREQUENCY DIVISION.

In this section the general properties of an ideal frequency divider are discussed. It will be shown that the frequency stability of the output of an ideal frequency divider is the same as the stability of the input.

Consider a device whose input-output relationships are as shown in Fig. 3-6.

First, consider the device driven by a perfect input signal (noise being excluded) expressed by

$$v_1(t) = A \cos \omega_o t \qquad (3\text{-}35)$$

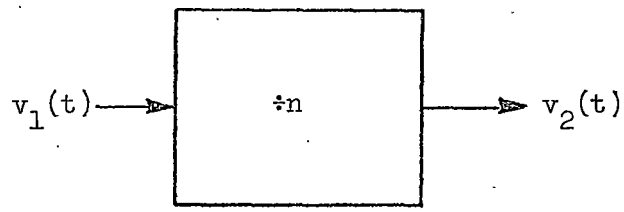


Fig. 3-6. IDEAL FREQUENCY DIVIDER.

with fixed amplitude A and frequency ω_o. The frequency divider will produce an output signal $v_2(t)$ expressed as

$$v_2(t) = A' \cos \frac{\omega_o t}{n}, \tag{3-36}$$

where n is an integer and A' = kA. This device is also referred to as a divide-by-n or n-divider.

Now let the input signal also contain a noise voltage term. The input signal $v_1(t)$ for this case as discussed in Sec. 3.1 is

$$v_1(t) = B(t) \cos [\omega_o t + \phi(t)]$$

$$= B(t) \cos \phi' (t). \tag{3-37}$$

For this $v_1(t)$ the divider output $v_2(t)$ will be expressed as

$$v_2(t) = B'(t) \cos \left[\frac{\omega_o t}{n} + \frac{\phi(t)}{n} \right] \tag{3-38}$$

where again n is an integer and B'(t) = kB(t).

From this definition of an ideal frequency divider two characteristics are apparent. First, that it is the instantaneous

frequency not the Fourier components that is being divided by the number n. In equation (3-37) $B(t)$ and $\phi'(t)$ are real functions of time. For signals of interest here, the signal-to-noise ratio will be large and therefore, $B(t)$ will be essentially a constant. For this assumption $B(t)$ will contain none of the zero crossing of $v_1(t)$, and $\phi'(t)$ is defined as the instantaneous phase angle of $v_1(t)$, and $\omega_i(t) = \frac{d\phi'(t)}{dt}$ is by definition the instantaneous frequency. The amplitude function $B(t)$ is the instantaneous amplitude and the magnitude of $B(t)$ is termed the envelope. Second, the frequency divider will leave a constant-envelope input signal unchanged except for a constant scale factor.

From (3-38) and the expression for the fractional short-term stability (A-21) given in Appendix A, it follows that the stability of the input signal after frequency division is not affected by the ideal frequency division process.

4.0 ANALYSIS OF TECHNIQUES INVESTIGATED

The availability of new semiconductors with highly refined performance characteristics has made the re-evaluation of common design approaches necessary. Several semiconductor devices now available yield system functions with significantly increased performance levels and in many cases will provide system simplification.

Techniques that employ several of the new semiconductor devices will be analyzed. The major characteristic desired in the techniques investigated is that of broadband input and output frequency characteristic while performing a specific circuit function. If the circuit operation does not naturally have this characteristic then it is desirable that it be capable of providing the required broadband operation by employing rapid electronic switching or tuning.

The discussions in this chapter are classed under the three signal operations presented in Chapter III. Parametric harmonic generators which use high Q input and output filters have been omitted from the discussions. Only two sinusoidal voltages are allowed to exist across the nonlinear capacitance. One voltage appears at the fundamental frequency, ω, and the other voltage appears at the n^{th} harmonic, $n\omega$. All other frequencies are shorted out. Analyses presented in the three references [9], [10], and [11] establish minimum and maximum efficiency levels for the varactor multiplier restricted to reverse bias operation.

4.1 SEMICONDUCTOR DEVICE CHARACTERIZATION.

The diodes used in the analysis presented in sections 4.2, 4.3, and 4.4 are classed as ideal nonlinear resistances or ideal nonlinear reactances. The ideal nonlinear resistance is approximated by the old work horse, the point contact diode and the more recently developed Hot Carrier or Schottky Barrier diodes. The ideal nonlinear reactances are approximated by the varactor diodes designed either for strictly reverse bias operation or forward conduction.

The ideal nonlinear resistor diode is a perfect rectifier as the V-I characteristics shown in Fig. 4-1 indicate. It is characterized by a devide with zero resistance under forward bias and with an infinite resistance under reverse bias. Another important characteristic of the perfect rectifier which is not pointed out by Fig. 4-1, is that the device exhibits zero capacitance. The capacitance referred to being either device case capacitance or a capacitance associated with the storage of conduction carriers.

The ideal nonlinear capacitance may be characterized as shown in Fig. 4-2. This is a charge (q) vs voltage characteristic. The nonlinear capacitance is characterized by an infinite capacitance under forward bias and zero capacitance under reverse bias, with complete recovery of charge when the voltage drops to zero.

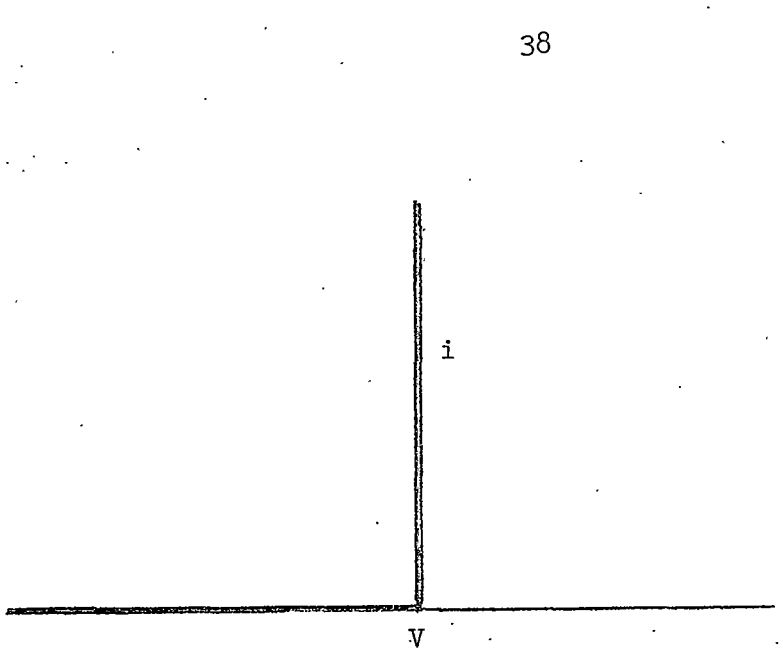


Fig. 4-1. IDEAL NONLINEAR RESISTOR CHARACTERISTICS.

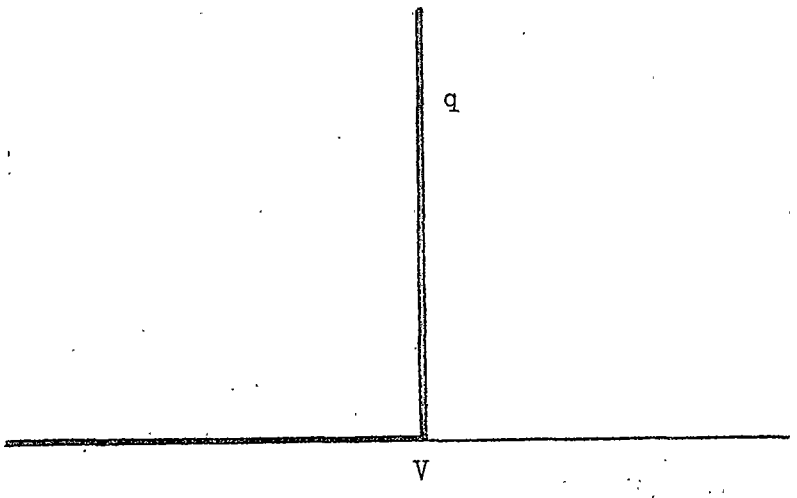


Fig. 4-2. IDEAL NONLINEAR CAPACITOR CHARACTERISTICS.

4.2 MULTIPLICATION.

Frequency multiplication using the nonlinear resistor has been developed by C. H. Page [12]. His results give an expression for the maximum harmonic generation efficiency as

$$P_i = P_o + \sum_{n>1} P_n \geq \sum_{n>1} n^2 P_n \geq n^2 P_n \tag{4-1}$$

where

P_n = power generated at the n^{th} harmonic

P_i = fundamental power

P_o = converted dc power.

For any specific value of n, two relations may be obtained from (4-1) as

$$P_n \leq \frac{1}{n^2} P_i \tag{4-2}$$

and

$$P_o \geq (n^2-1) P_n \tag{4-3}$$

Equation (4-2) gives the maximum efficiency limit as $1/n^2$ for the condition of all other harmonics being zero. Equation (4-3) shows that the remaining fundamental power (when equality holds) is converted to dc.

Greater efficiency can be expected for the nonlinear capacitor since the device would not rectify and hence input power conversion

to dc power is eliminated. Manley and Rowe [13] have derived the general set of power flow relationships for an ideal nonlinear reactance in a general circuit configuration using ideal filters. The equation they obtained are

$$\sum_{m=0}^{\infty} \sum_{n=-\infty}^{\infty} \frac{mP_{m,n}}{mf_1+nf_2} = 0 \qquad (4\text{-}4)$$

$$\sum_{n=0}^{\infty} \sum_{m=-\infty}^{\infty} \frac{nP_{m,n}}{mf_1+nf_2} = 0 \qquad (4\text{-}5)$$

where $P_{m,n}$ is the power flow into the reactance at frequency mf_1 and nf_2. These relationships are independent of the shape of the nonlinear characteristic and the power levels employed. With proper filtering, these relationships predict that a lossless nonlinear reactance used in a harmonic generator configuration has a conversion efficiency of 100%, regardless of the harmonic involved. To illustrate this result, consider power flow allowed only at two frequencies, one being the fundamental frequency (f) and the other the desired harmonic (nf). Equation (4-4) then reduces to

$$\frac{P_o}{f} + \frac{nP_n}{nf} = 0 \qquad (4\text{-}6)$$

where

P_o = power at f (supplied by input generator)

P_n = power at nf (delivered to output load).

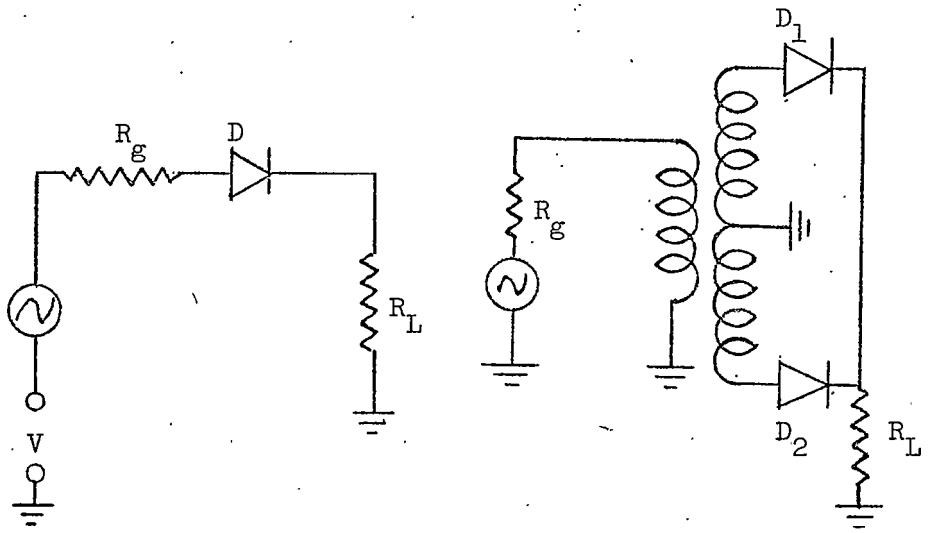
Equation (4-6) gives $P_n/P_o = -1$ which indicates the 100% harmonic conversion efficiency, independent of the multiplication order n.

The discussion thus far has served to set the theoretical limits of harmonic conversion efficiencies obtainable depending upon the nonlinearity employed. In the sections that follow, discussion will focus on techniques which perform the multiplication function but whose maximum theoretical conversion efficiencies fall short of upper theoretical limits. For a set of system specifications, these less efficient techniques may be dictated in the system realization by such factors as cost, size, tuning speed, etc.

4.2.1 RECTIFIER DIODE HARMONIC GENERATOR.

Two broadband rectifier diode circuit techniques to be analyzed are the clipped sine wave generator and the full wave rectifier. The equivalent circuits for these generators are shown in Fig. 4-3.

The analysis of the clipped sine wave generator is given in Appendix C. The theoretical conversion loss for the harmonic frequency components appearing across R_L are shown in Fig. 4-4, and Fig. 4-5, as a function of the half-conduction angle θ. The curves presented in Fig. 4-4 are for the even order harmonics of the input frequency and those presented in Fig. 4-5 are for the odd order harmonics.



(a) (b)

Fig. 4-3. RECTIFIER GENERATOR EQUIVALENT CIRCUITS.

(a) Clipped sine wave generator

(b) Full wave rectifier.

The data presented was calculated on one degree increments using a digital computer.

Figure 4-6 presents the minimum conversion loss associated with each harmonic as taken from the computed data. The minimum loss associated with the even order harmonics occurs for $\theta = 90^\circ$ and the numbers associated with each odd order graph entry indicate the value of θ at which their respective minima occurred.

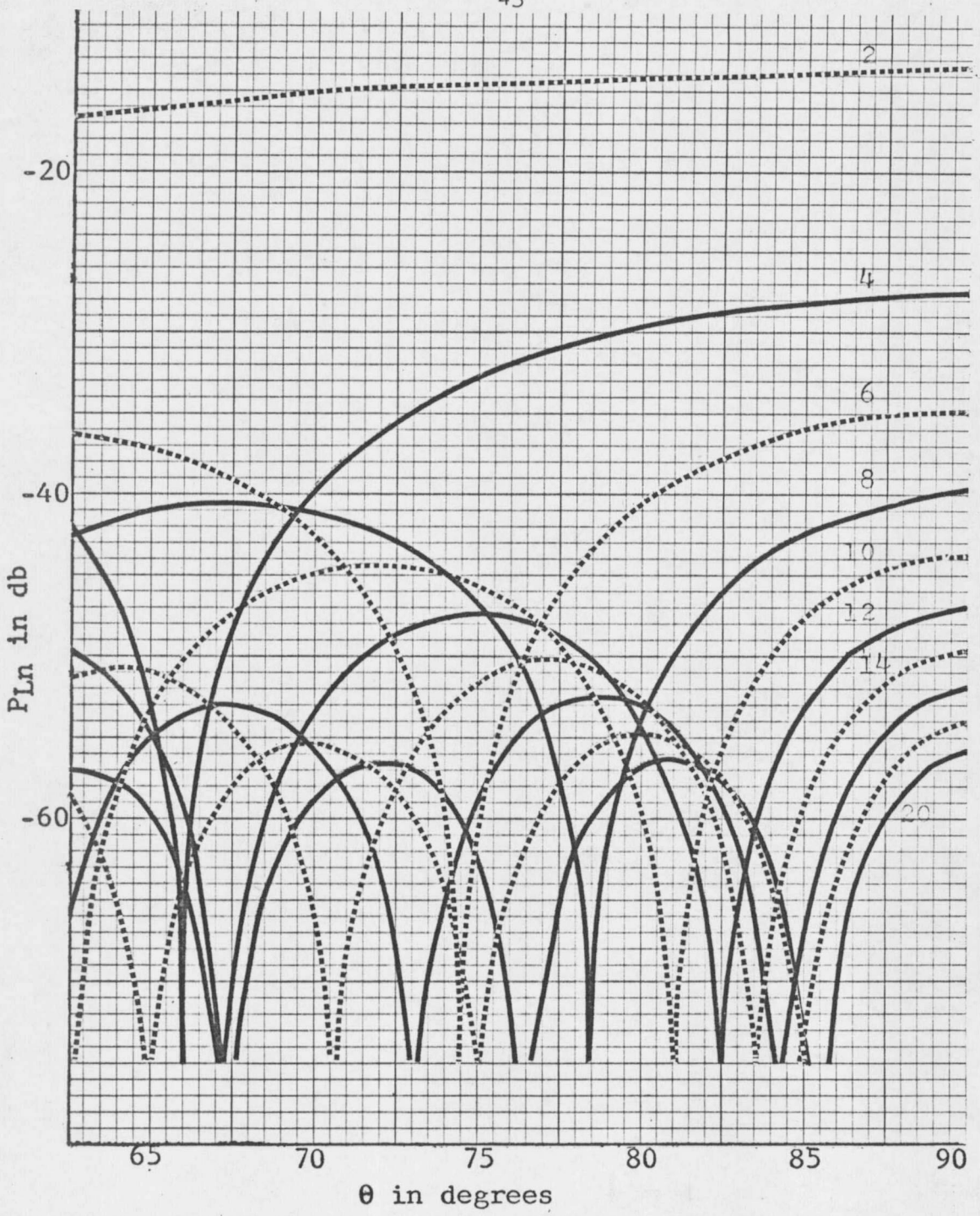


Fig. 4-4. CLIPPED SINE WAVE OUTPUT SPECTRUM n EVEN.

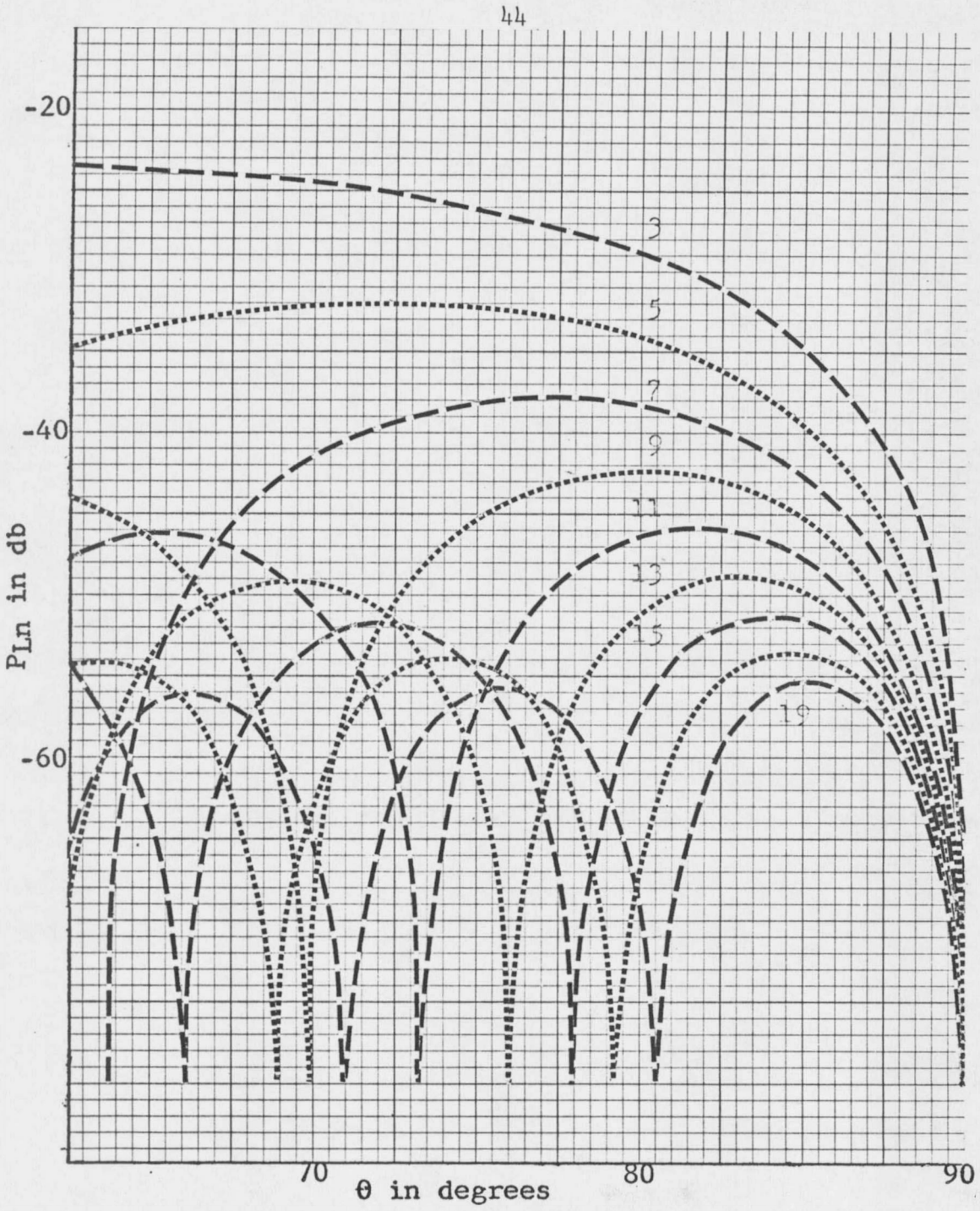


Fig. 4-5. CLIPPED SINE WAVE OUTPUT SPECTRUM n ODD.

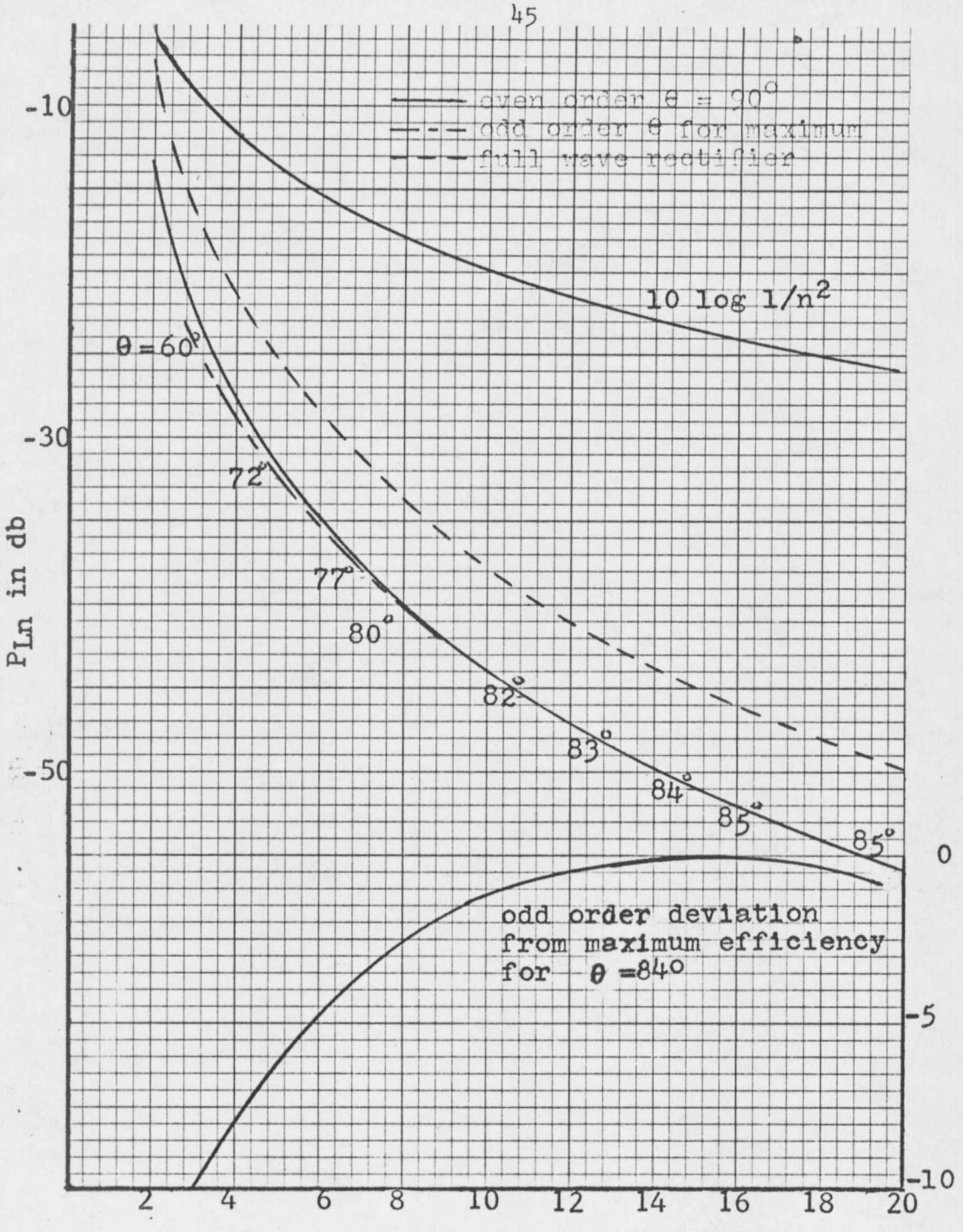


Fig. 4-6. MAXIMUM SPECTRUM AMPLITUDE-CLIPPED SINE WAVE GENERATOR.

The harmonic spectrum of the full wave rectifier can be obtained from the half wave rectifier spectrum ($\theta = 90°$) by adding 6.02 db to the even order values. These values are also presented in Fig. 4-6. The deviation from the maximum efficiency, 10 log $1/n^2$, can be determined directly for either the clipped sine wave or full wave rectifier generators.

The curve at the bottom of Fig. 4-6 indicates how this type of generator might be used when a braodband spectrum is desired. If a half-conduction angle $\theta = 84°$ were used the odd-order harmonic spectrum, 3rd to 19th harmonic, would vary less than 10 db from the maximum attainable output.

For an even and odd high order harmonic spectrum of a particular characteristic an angle θ between 85 and 90 degress would be used. As indicated in Fig. 4-6 the most efficient of the techniques under consideration here is the full wave rectifier used as a frequency doubler, $n = 2$.

4.2.2 BROADBAND NONLINEAR CAPACITOR HARMONIC GENERATOR.

The broadband-harmonic generator has been analyzed by Leenov and Uhlir [14]. The equivalent circuit for the broadband nonlinear capacitor harmonic generator is shown in Fig. 4-7. The diode used in this analysis has infinite capacitance under forward bias, complete recovery of charge when the voltage drops to zero and zero

capacitance under reverse bias.

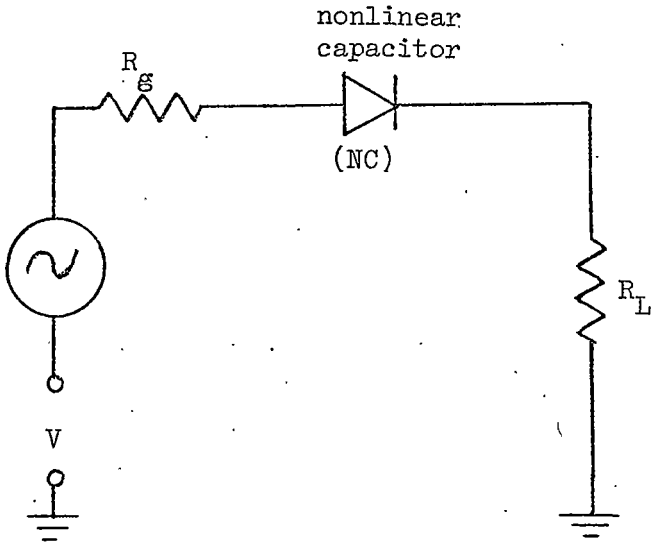


Fig. 4-7. BROADBAND HARMONIC GENERATOR EQUIVALENT CIRCUIT.

The analysis of this harmonic generator is presented in Appendix D. The theoretical conversion loss for the harmonic frequency components appearing across R_L are shown in Fig. 4-8 and 4-9 as a function of the half-forward conduction angle θ. The curves presented in Fig. 4-8 are for the even order harmonics of the input frequency and those presented in Fig. 4-9 are for the odd order harmonics. This data was computed on ten degree increments using a digital computer.

Figure 4-10 presents the minimum conversion loss associated with each harmonic as taken from the computed data disregarding the

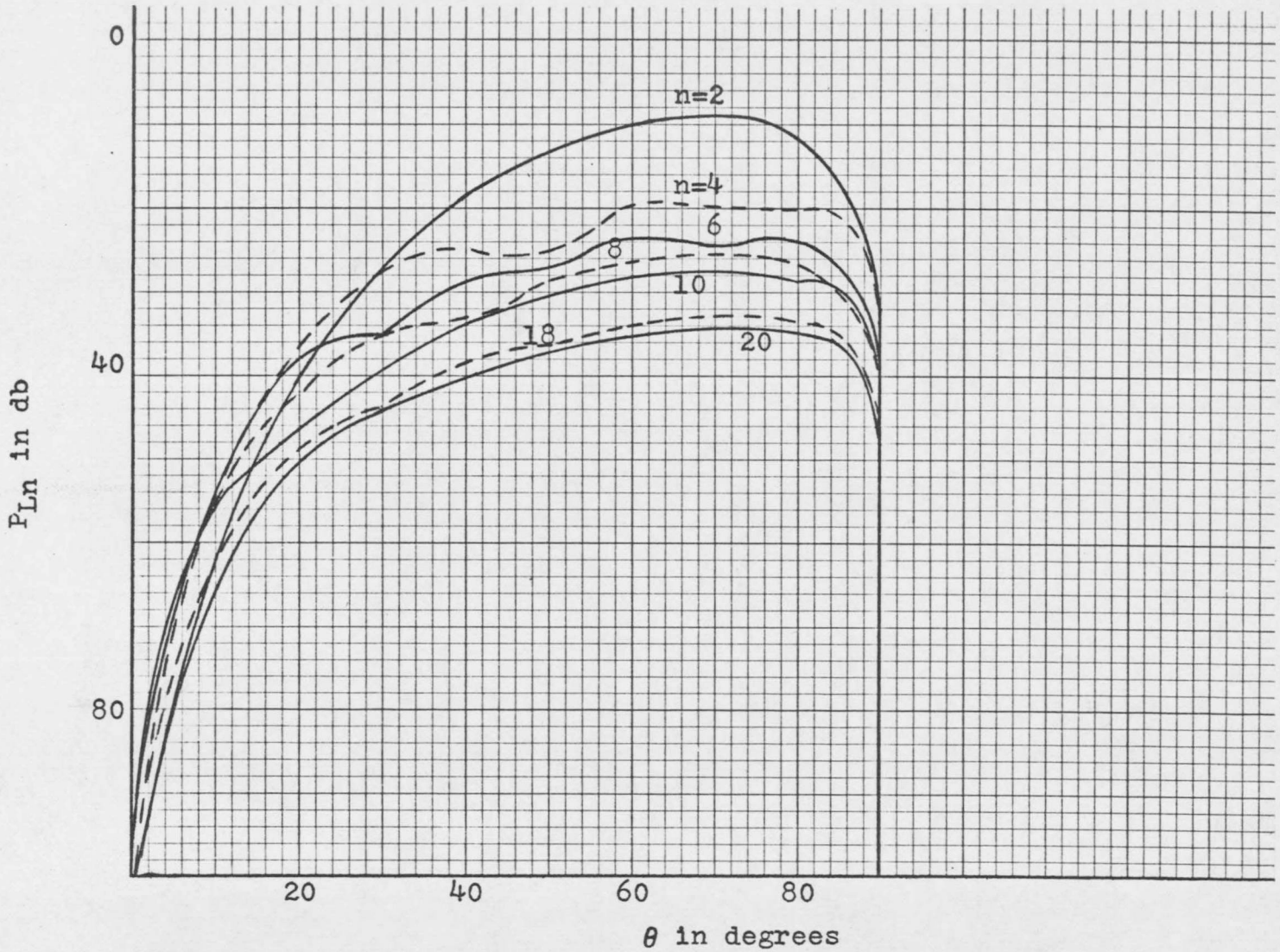


Fig. 4-8. N-C HARMONIC SPECTRUM n EVEN.

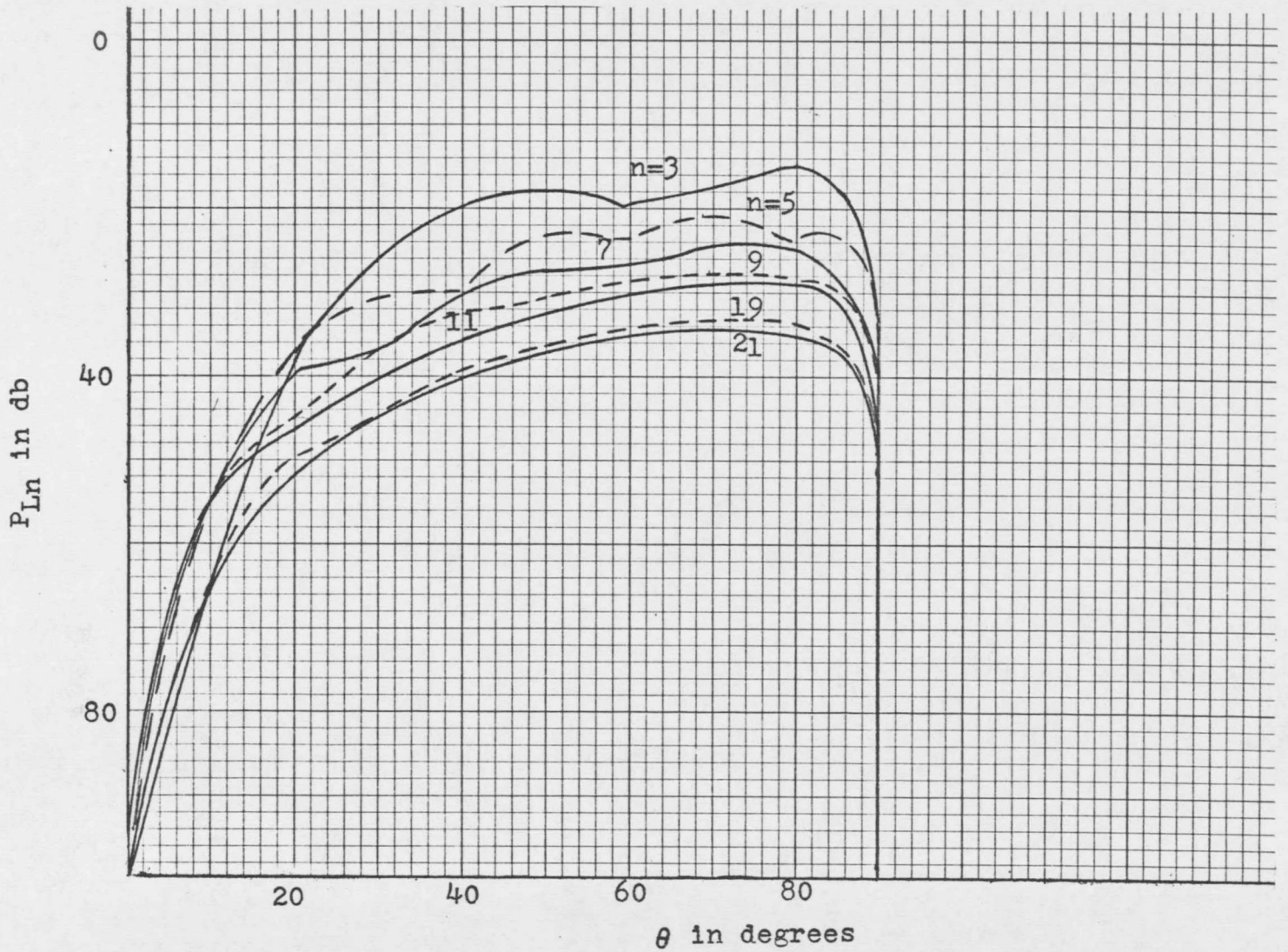


Fig. 4-9. N-C HARMONIC SPECTRUM n-ODD

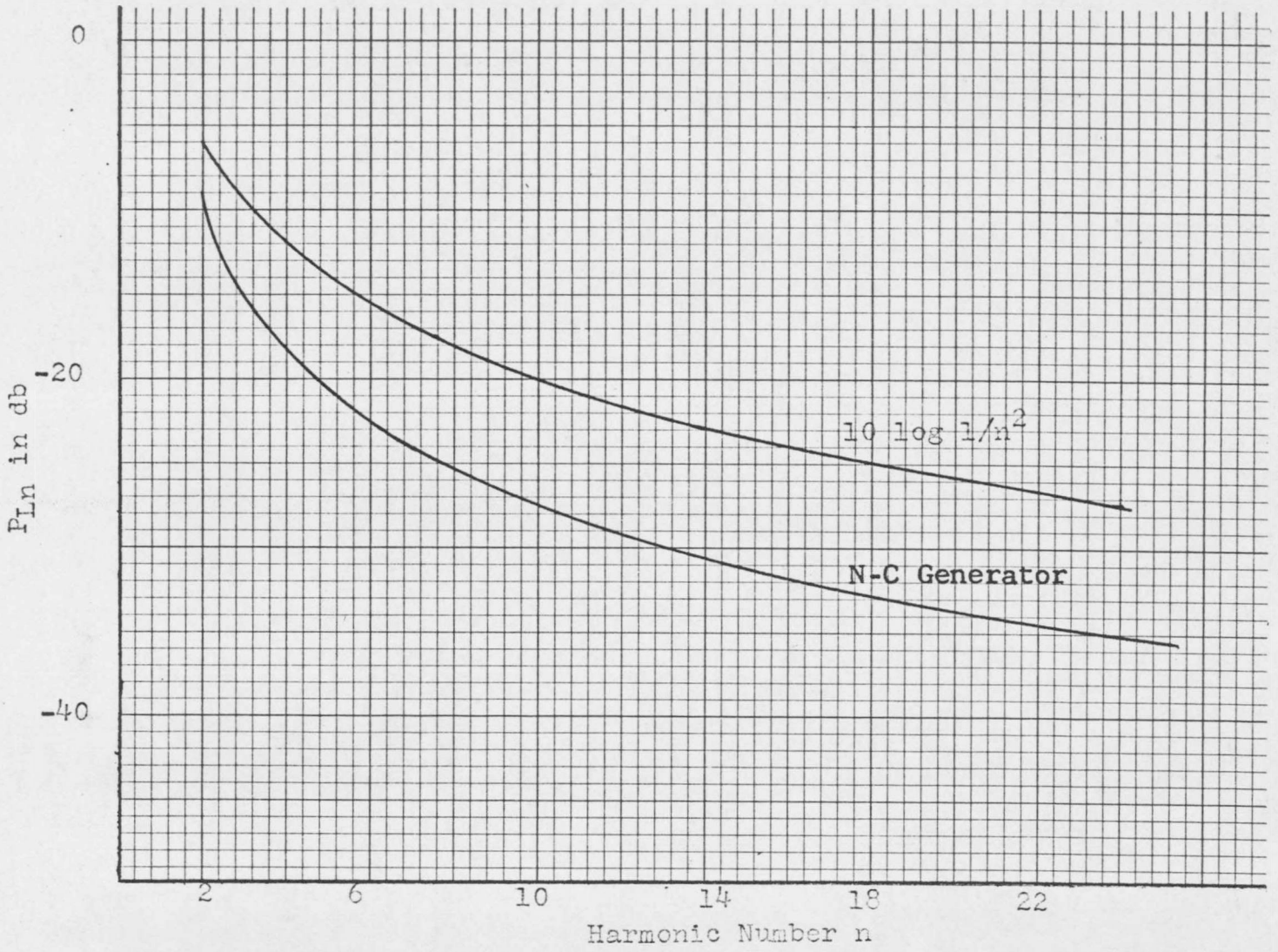


Fig. 4-10. MINIMUM CONVERSION LOSS FOR N-C GENERATOR.

conduction angles required for these minima. Comparison of Fig. 4-6 and 4-10 will indicate the superior performance of this broadband generator to the rectifier diode generator. This efficiency advantage increases as higher order harmonics are considered.

4.2.3 BROADBAND STEP RECOVERY DIODE HARMONIC GENERATOR.

In harmonic generation, where the diode is operated with intermittent forward conduction, the performance will depend on minority carrier lifetime, τ, and the junction retarding field as discussed in reference [15]. Minority carrier lifetime determines the amount of stored charge that remains in the junction at the onset of reverse recovery and the rate of carrier recombination during recovery. The junction field determines the stored charge available for removal during storage conduction. For a minority carrier lifetime of zero, the diode characteristics are those of a nonlinear resistance as used in the analysis of 4.2.1. If the minority carrier lifetime is assumed infinite, the diode characteristics are those of the nonlinear capacitance used in the analysis of 4.2.2. This section is concerned with the broadband harmonic generating characteristics associated with the class of diodes having high junction retarding fields and finite carrier lifetimes.

The broadband analysis presented here parallels and analysis presented by Krakauer [16], with many graphical additions which give

a clearer understanding of the multiplier performance as $\omega\tau$ and ϕ are varied.

The equivalent circuit and steady state current waveform for this analysis is shown in Fig. 4-11. Circuit current starts to flow at $\omega t = \theta$ when the input voltage overcomes the bias voltage, V, plus the diode barrier voltage, ψ. Diode current flows until $\omega t = \theta + \phi$ at which time the stored charge has been depleted.

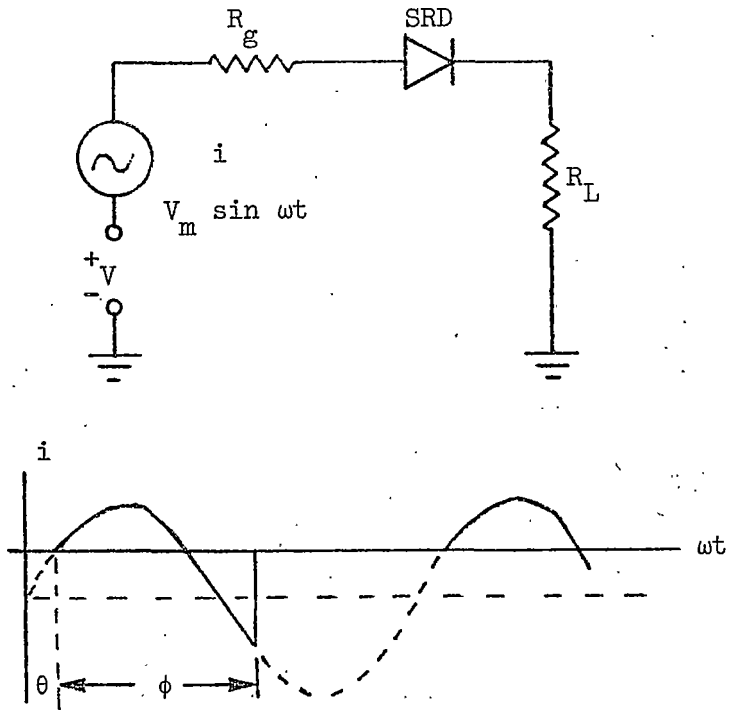


Fig. 4-11. SRD BROADBAND MULTIPLIER EQUIVALENT CIRCUIT AND CURRENT WAVEFORM.

The relation between θ and ϕ is derived in Appendix E and is expressed as

$$\text{Tan } \theta = \frac{\sin \phi - \omega\tau \cos \phi + \omega\tau e^{-\phi/\omega\tau}}{-\omega\tau \sin \phi - \cos \phi + \omega^2 \tau^2 (1-e^{-\phi/\omega\tau}) + 1} \qquad (4\text{-}7)$$

where

ω = input frequency

τ = minority carrier lifetime

θ and ϕ as indicated in Fig. 4-11.

Values for θ were computed, for $\omega\tau$ values between 0.1 and 1,000,000, as a function of ϕ. The results are presented in Fig. 4-12. As illustrated, the $\omega\tau$ dependence is essentially eliminated for $\omega\tau > 10$.

The harmonic spectrum conversion loss associated with the current waveform of Fig. 4-11 is also presented in Appendix E. The calculation was carried out using a digital computer. Several graphs of the computed data are presented for various value of $\omega\tau$. Fig. 4-13, 4-14, 4-15, 4-16 are the harmonic spectrum presentations for $\omega\tau = 3.0$. Fig. 4-17, 4-18, 4-19, 4-20 are the presentations for $\omega\tau = 10.0$, and Fig. 4-21, 4-22, 4-23, 4-24 are for $\omega\tau = 100.0$.

Fig. 4-25 presents the minimum conversion loss associated with each harmonic disregarding the condition angle, ϕ, required for these minimums. The dependence of the generator conversion loss as a function of the $\omega\tau$ product is clearly illustrated.

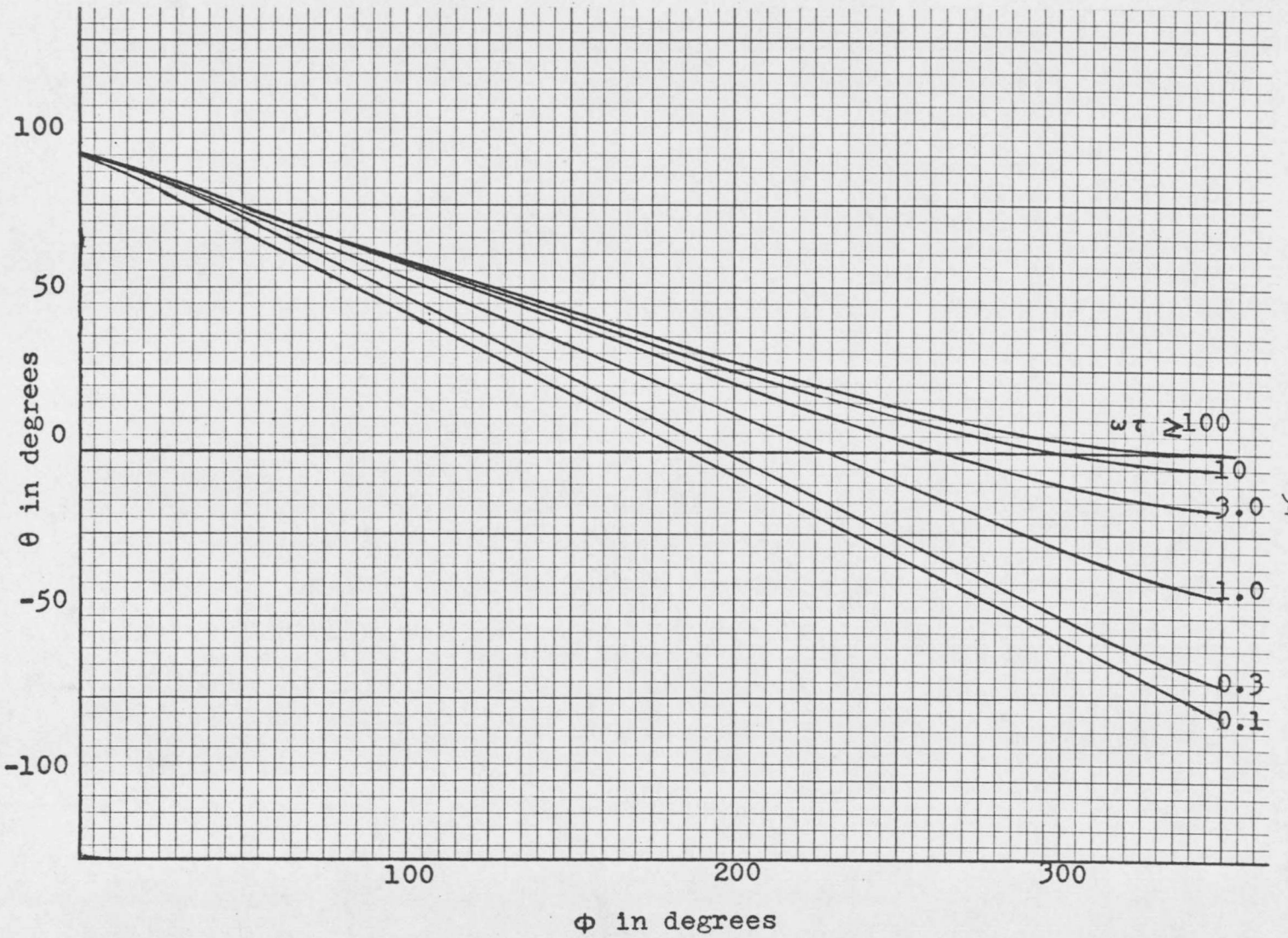


Fig. 4-12. θ AND Φ FOR SRD MULTIPLIER.

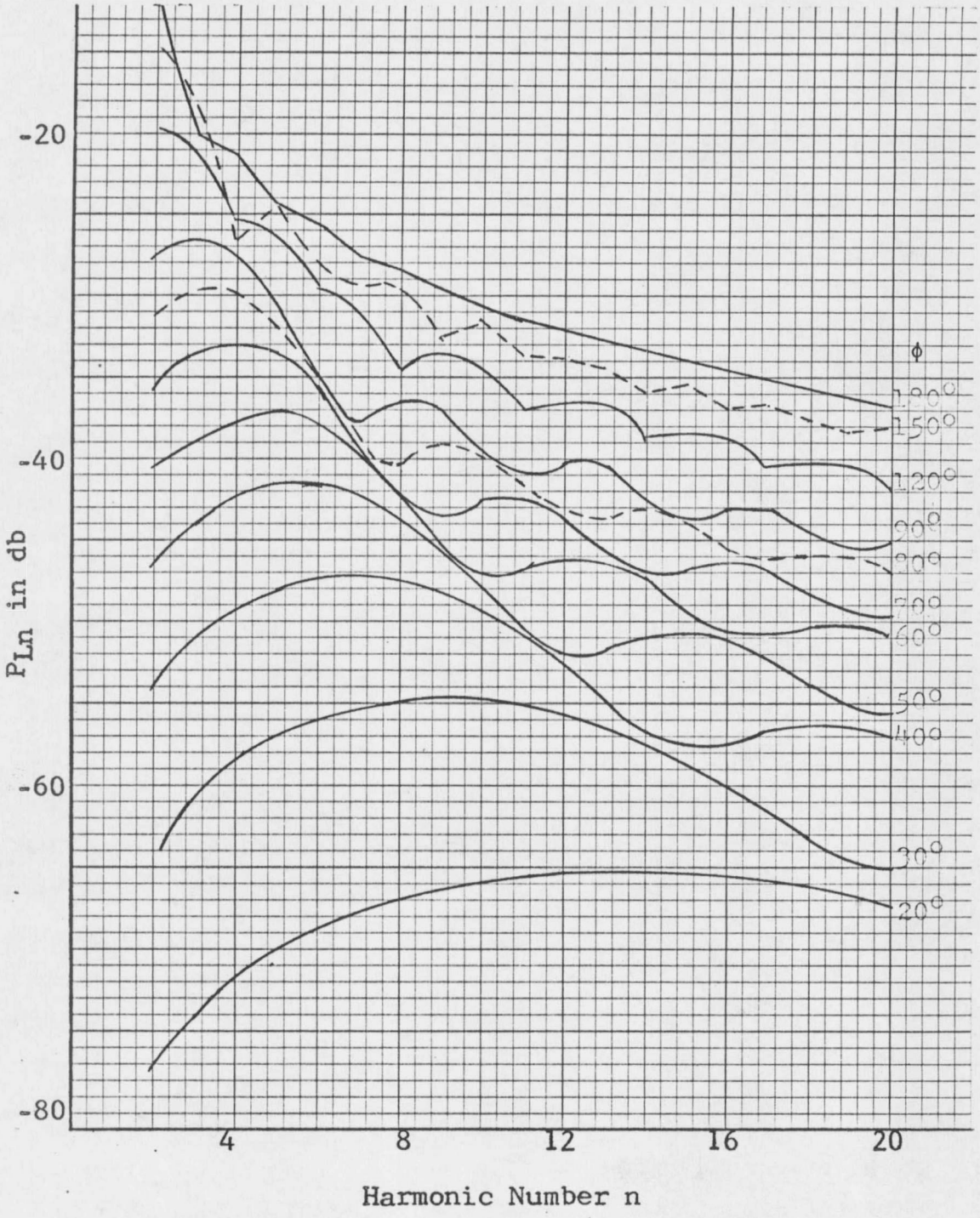


Fig. 4-13. SRD HARMONIC SPECTRUM $\omega\tau = 3.0$.

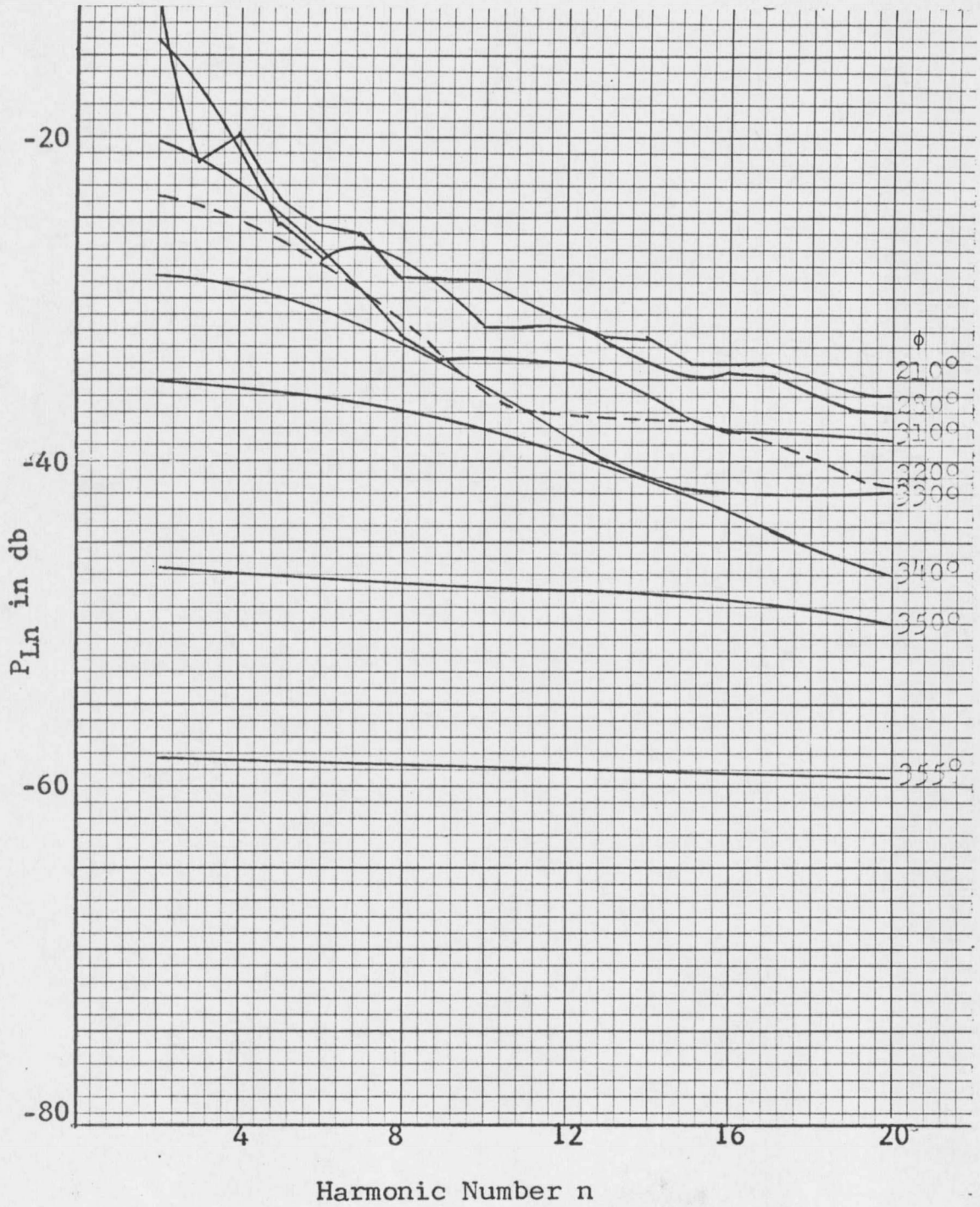


Fig. 4-14. SRD HARMONIC SPECTRUM $\omega\tau = 3.0$.

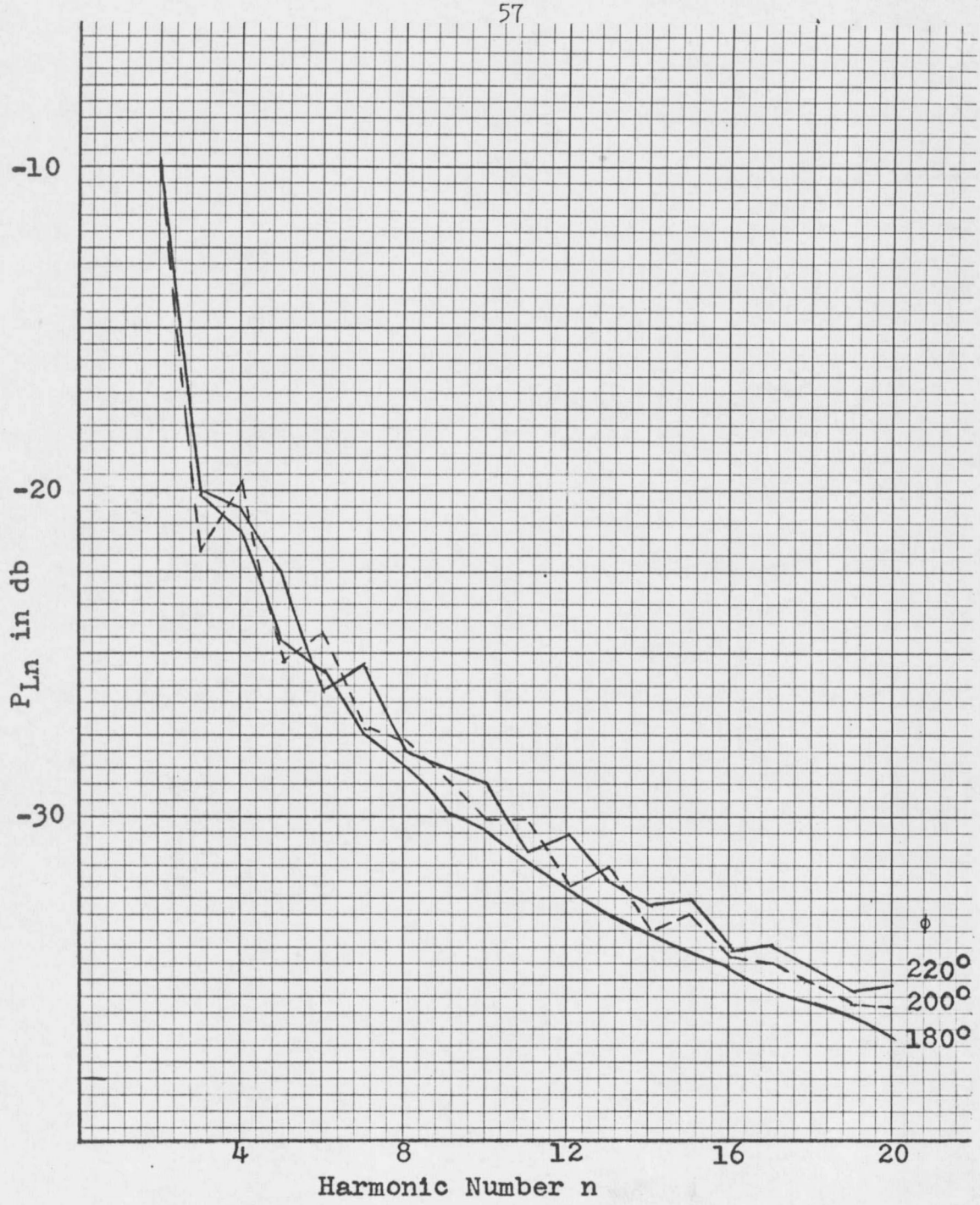


Fig. 4-15. SRD HARMONIC SPECTRUM $\omega\tau = 3.0$.



Fig. 4-16. SRD HARMONIC SPECTRUM $\omega\tau = 3.0$.

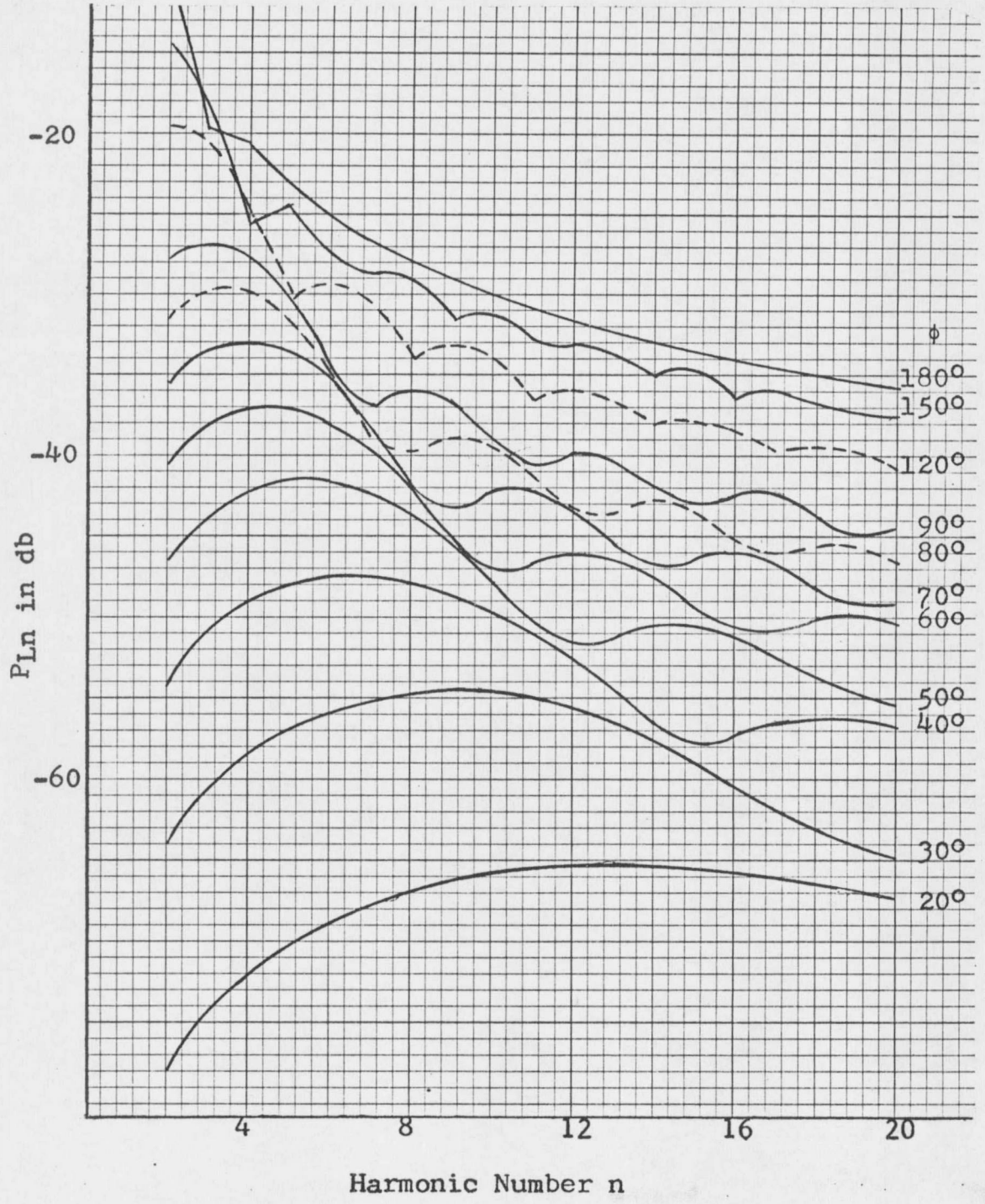


Fig. 4-17. SRD HARMONIC SPECTRUM $\omega\tau = 10$.

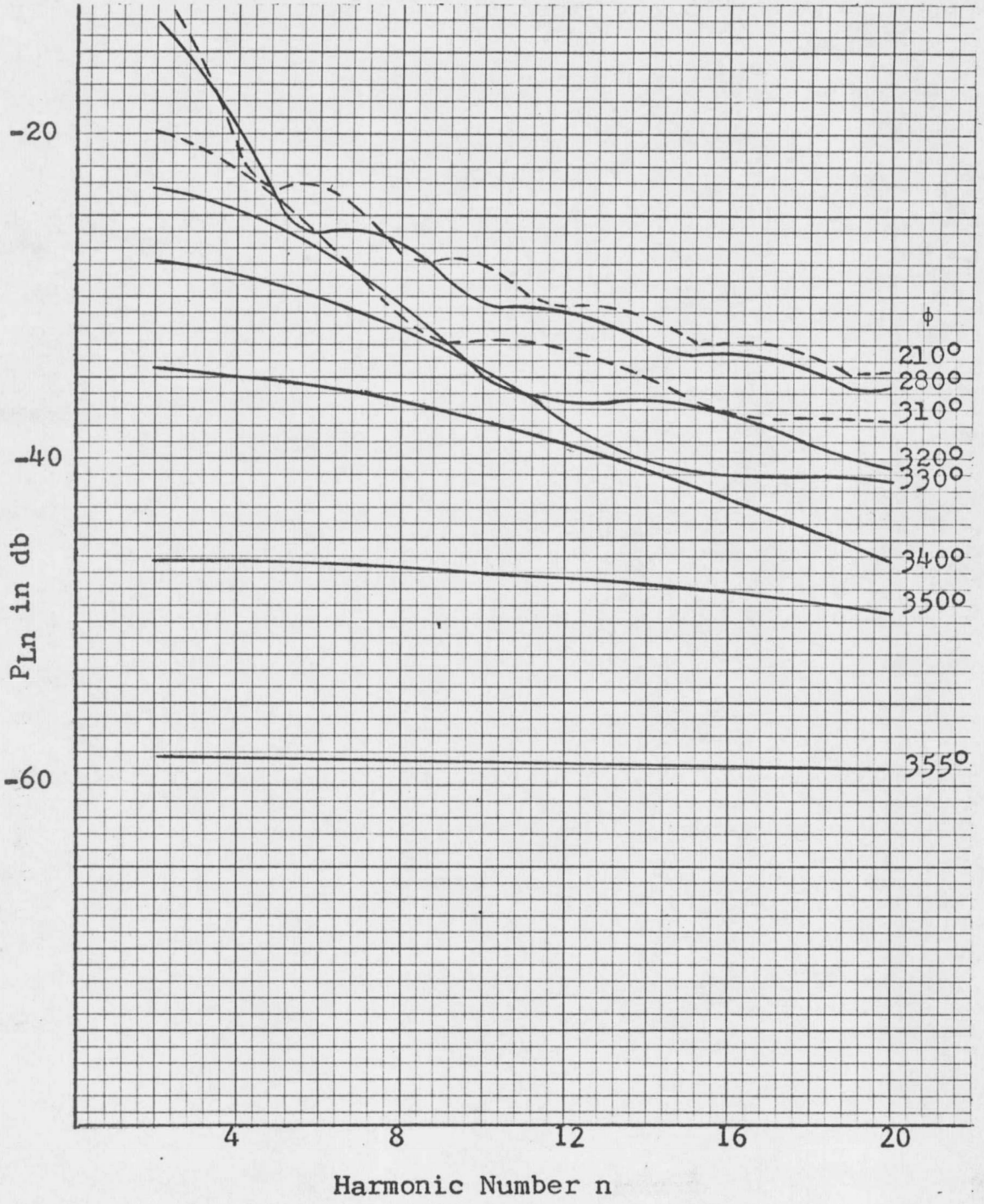


Fig. 4-18. SRD HARMONIC SPECTRUM $\omega\tau = 10.$

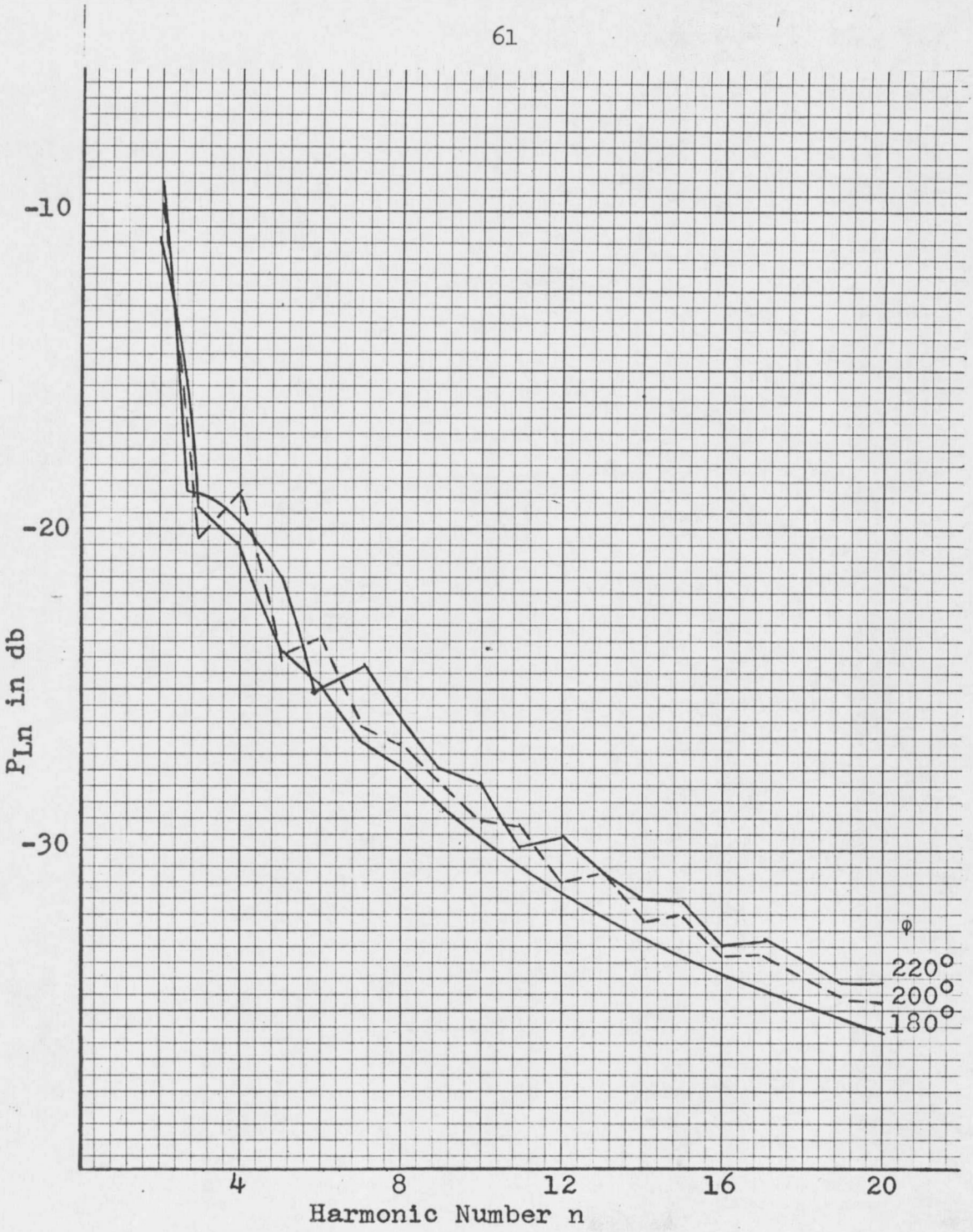


Fig. 4-19. SRD HARMONIC SPECTRUM $\omega\tau = 10.$

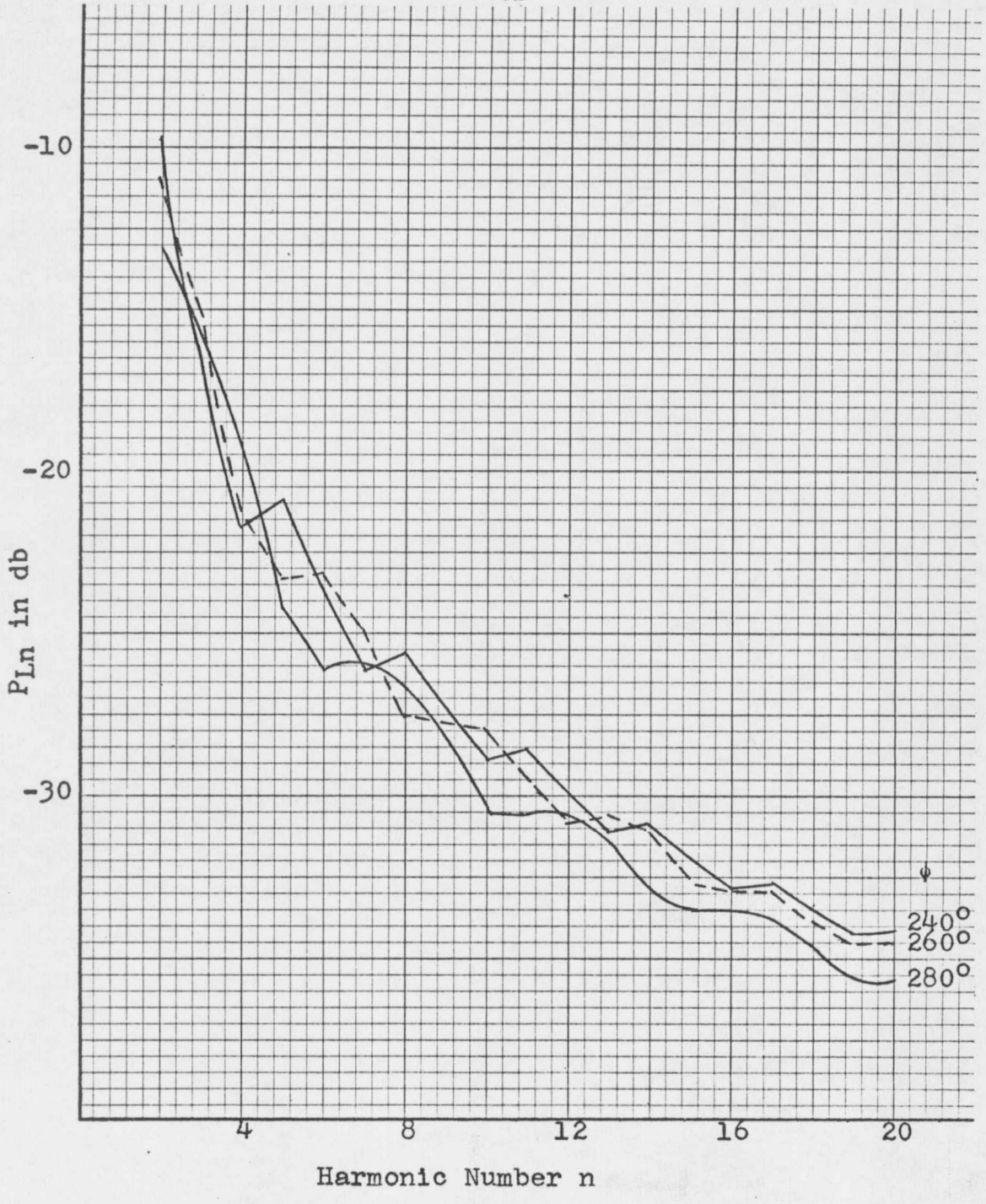


Fig. 4-20. SRD HARMONIC SPECTRUM $\omega\tau = 10$.

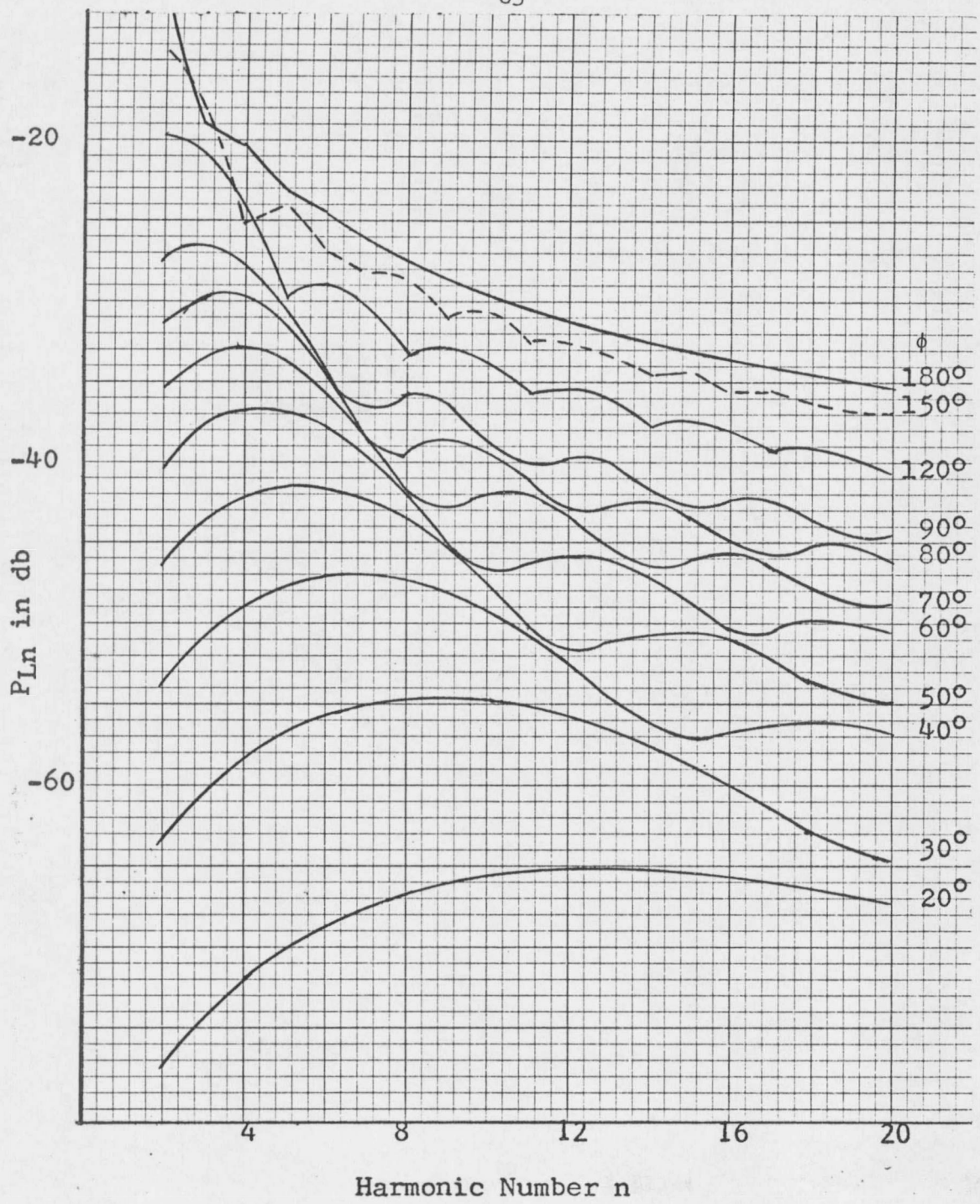


Fig. 4-21. SRD HARMONIC SPECTRUM $\omega\tau = 100$.

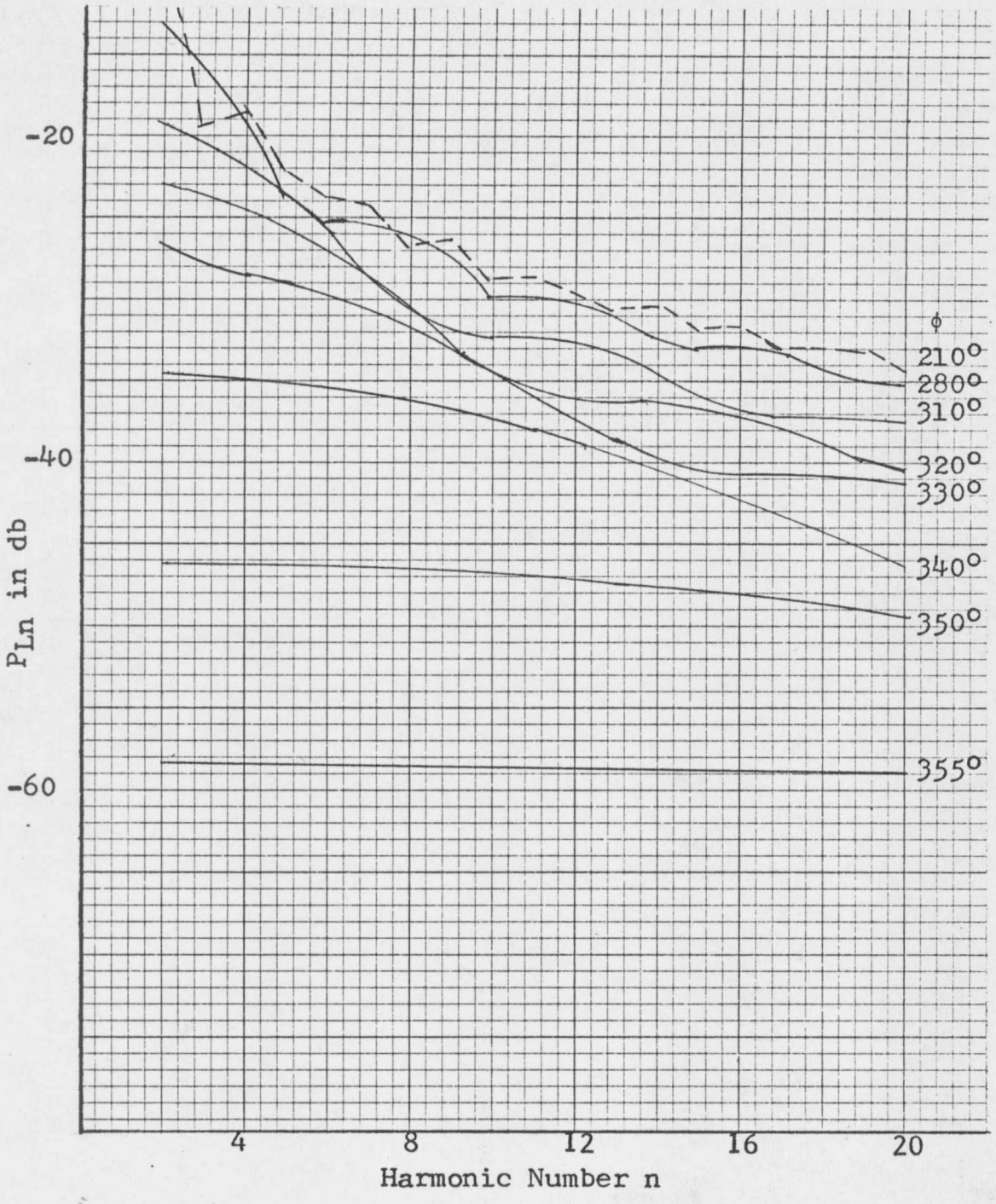


Fig. 4-22. SRD HARMONIC SPECTRUM $w\tau = 100$.

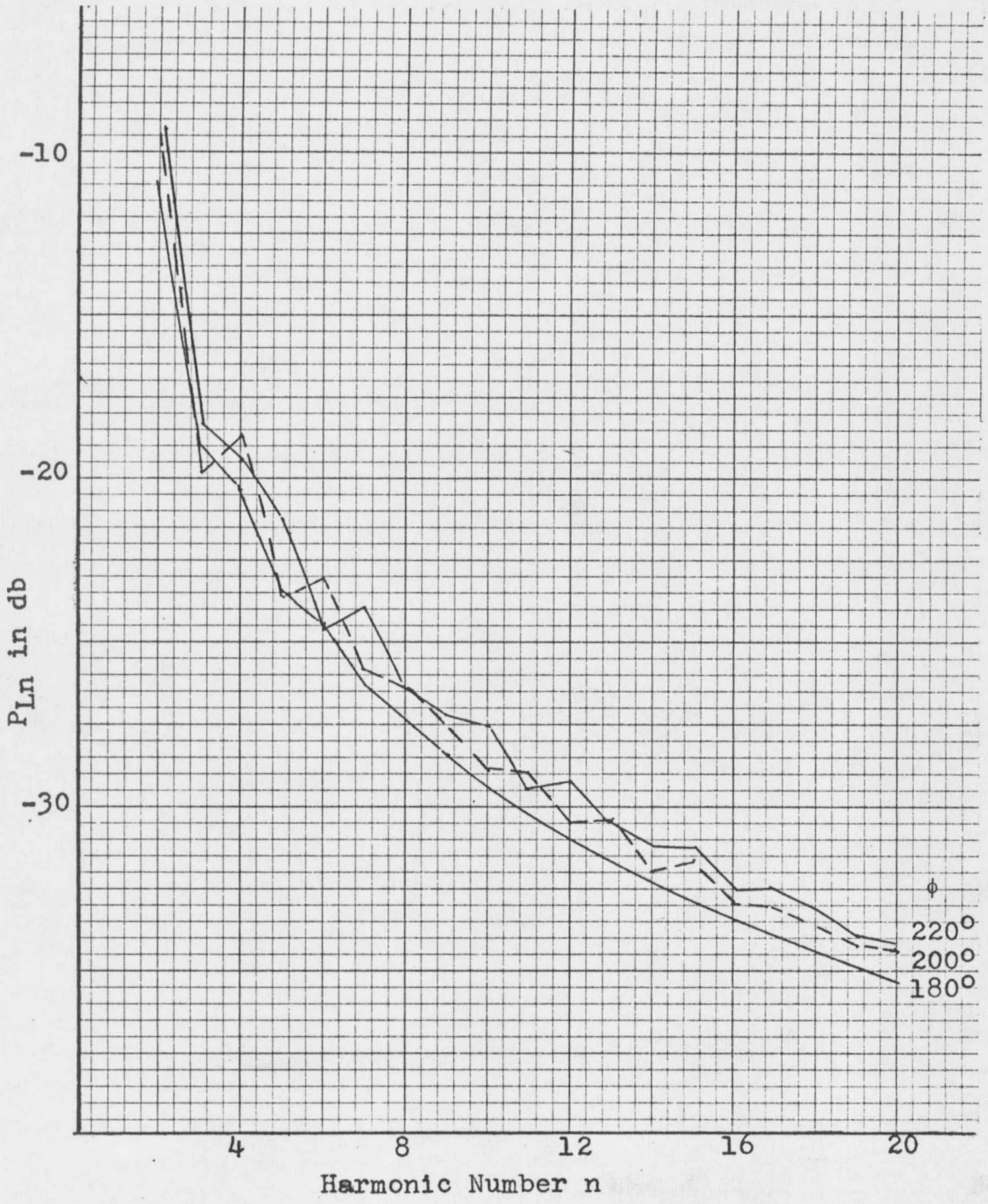


Fig. 4-23. SRD HARMONIC SPECTRUM $\omega\tau = 100$.

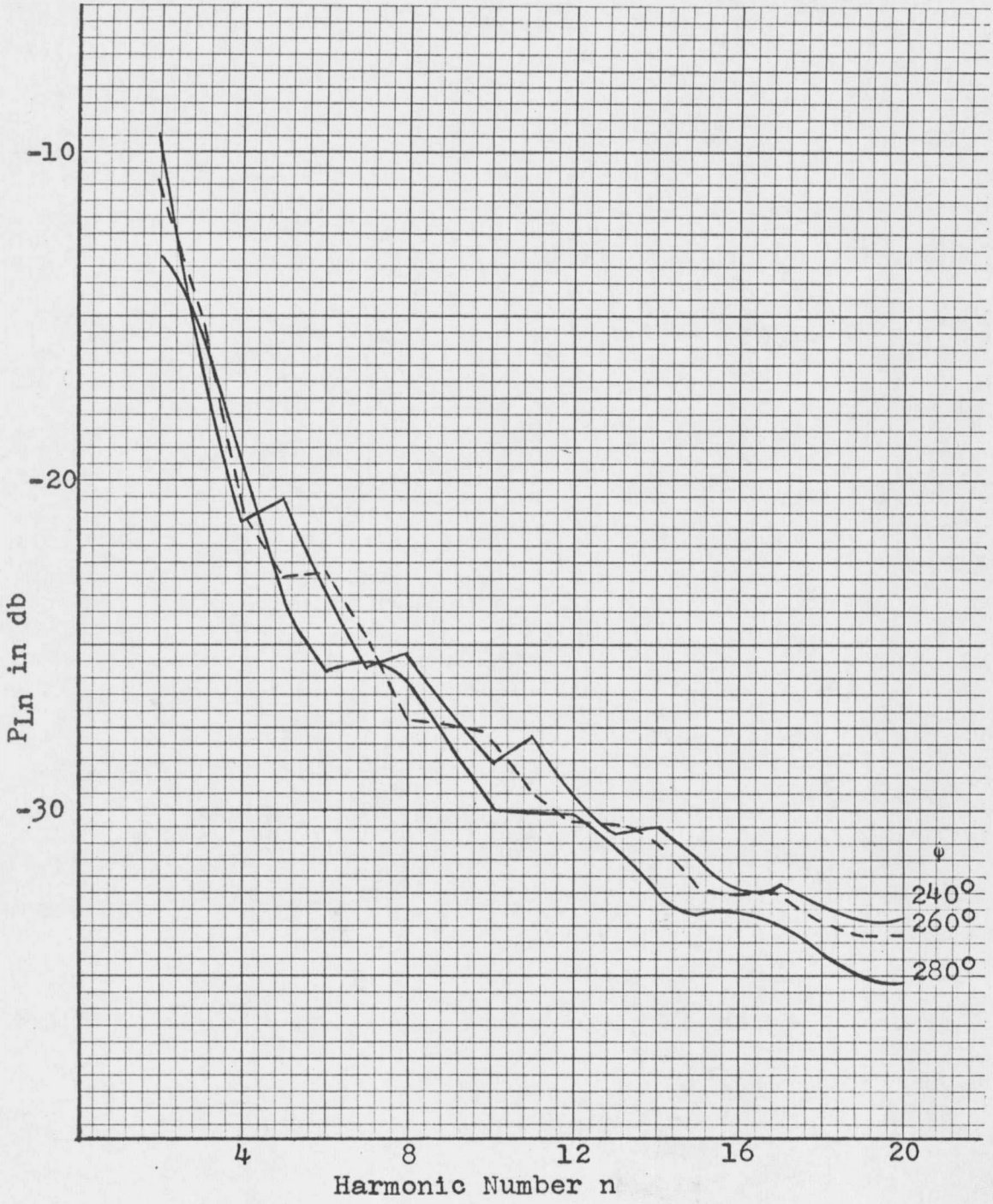


Fig. 4-24. SRD HARMONIC SPECTRUM $\omega\tau = 100.$

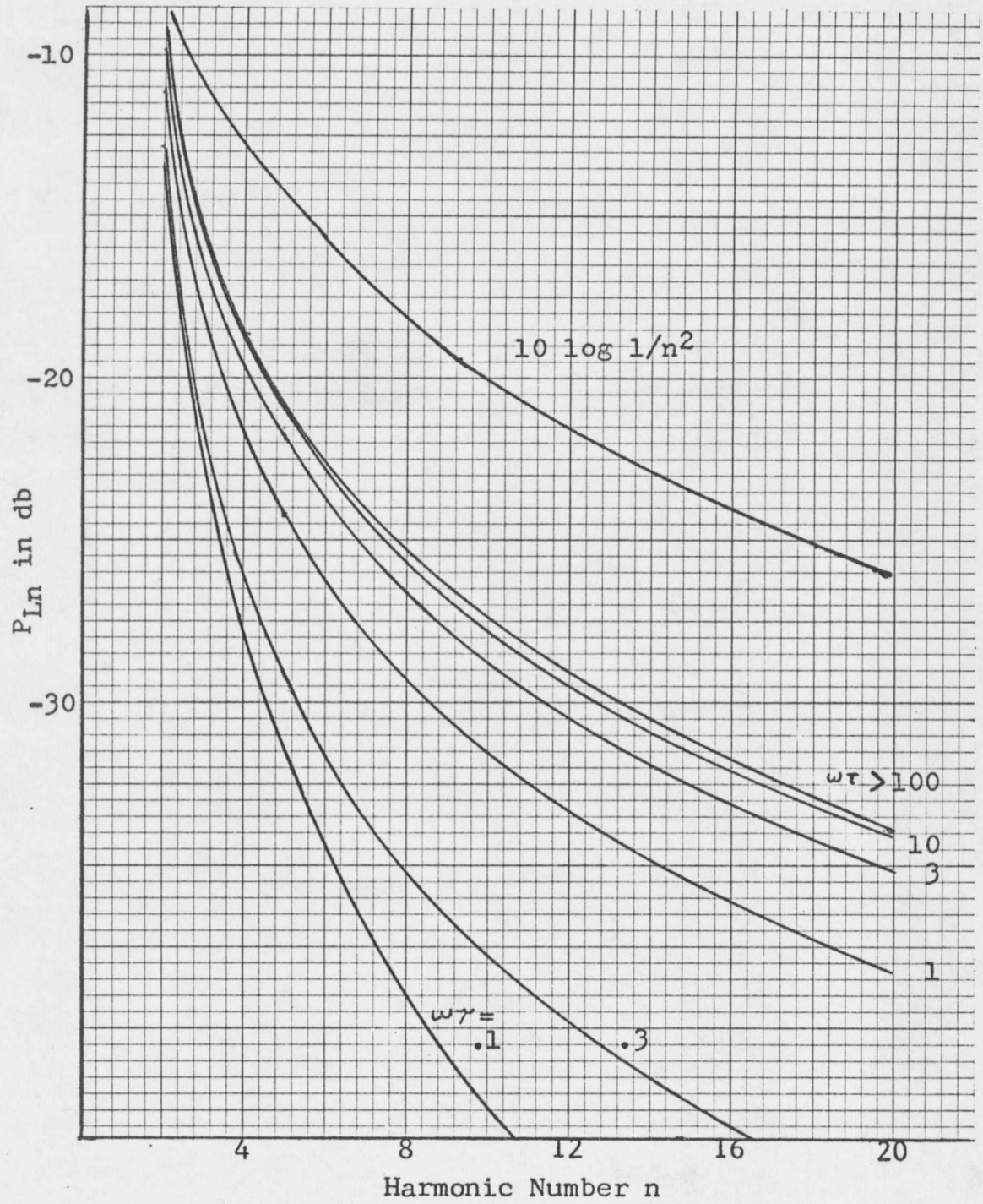


Fig. 4-25. SRD MINIMUM CONVERSION LOSS.

Another set of curves can be presented from the computed data which indicate more clearly the conversion loss dependence for a specific harmonic as a function of ϕ. A set for even and odd order harmonics for $\omega\tau = 3.0$ are given in Fig. 4-26 and 4-27 respectively.

Still another graphical presentation which relates harmonic number, conversion loss variation and ϕ may be presented as in Fig. 4-28. This presentation along with that of Fig. 4-25 would present the necessary design information for a specific application.

Curves similar to those of Fig. 4-28 were drawn for $\omega\tau = 1.0$, 10, 100, and 1000. If the design application can tolerate a deviation from the minimum conversion loss presented in Fig. 4-25 then ϕ will have a range of values. The range of ϕ for selected deviation levels of 1 and 3 db of the minimum conversion loss as a function of $\omega\tau$ are given in table 4-1.

The diode discontinuity for this analysis was assumed to be instantaneous. In the practical multiplier a finite transition time, t_t, exists. The effect of this on the harmonic generation will be discussed in Chapter 5.

4.2.4 STEP RECOVERY DIODE HARMONIC GENERATOR WITH RESONANT LOAD.

Replacing the load resistance in the multiplier circuit of Fig. 4-11 with a resonant load yields a significant increase in the conversion efficiency at the harmonic associated with this

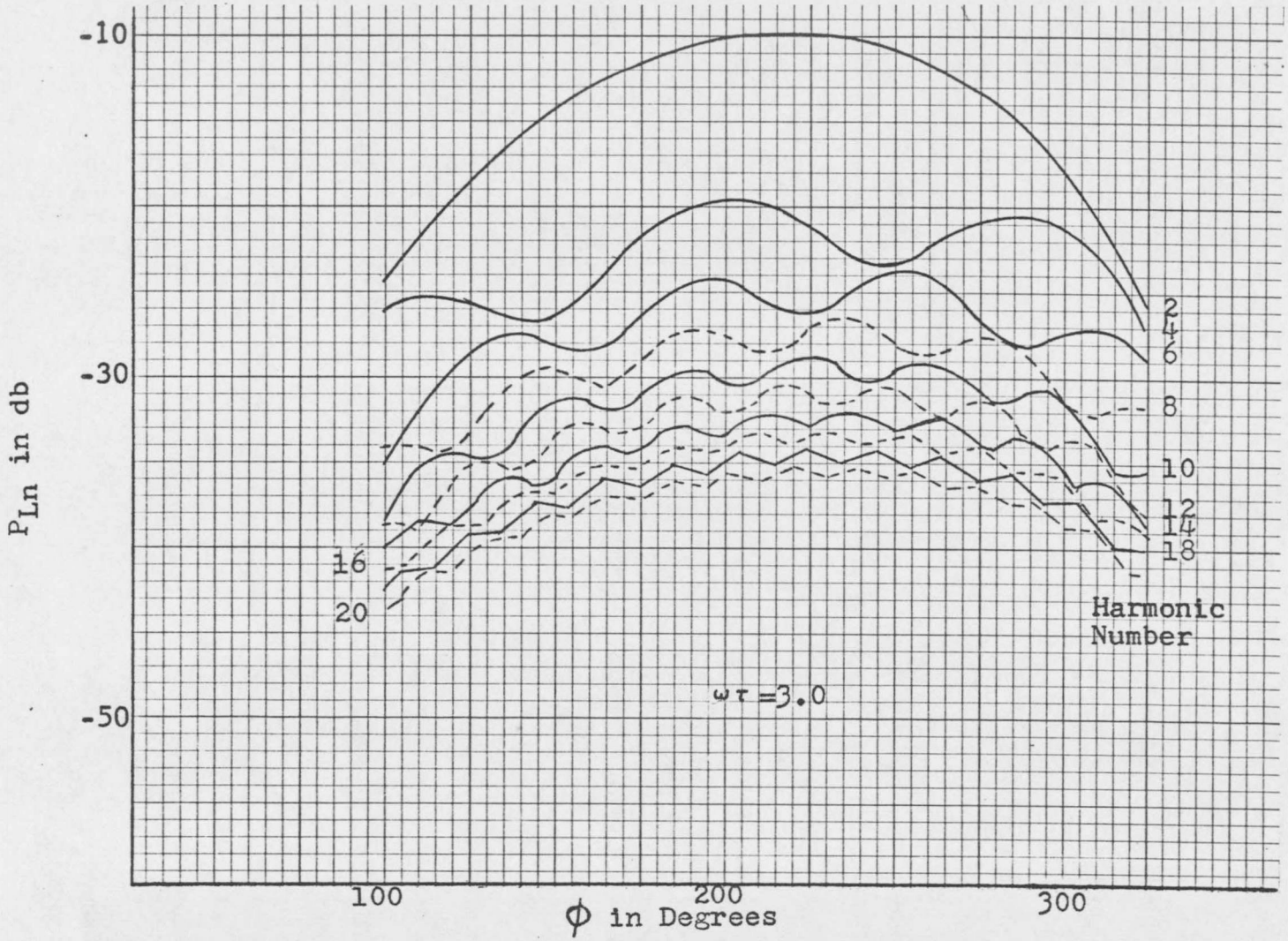


Fig. 4-26. CONVERSION LOSS vs Φ n EVEN.

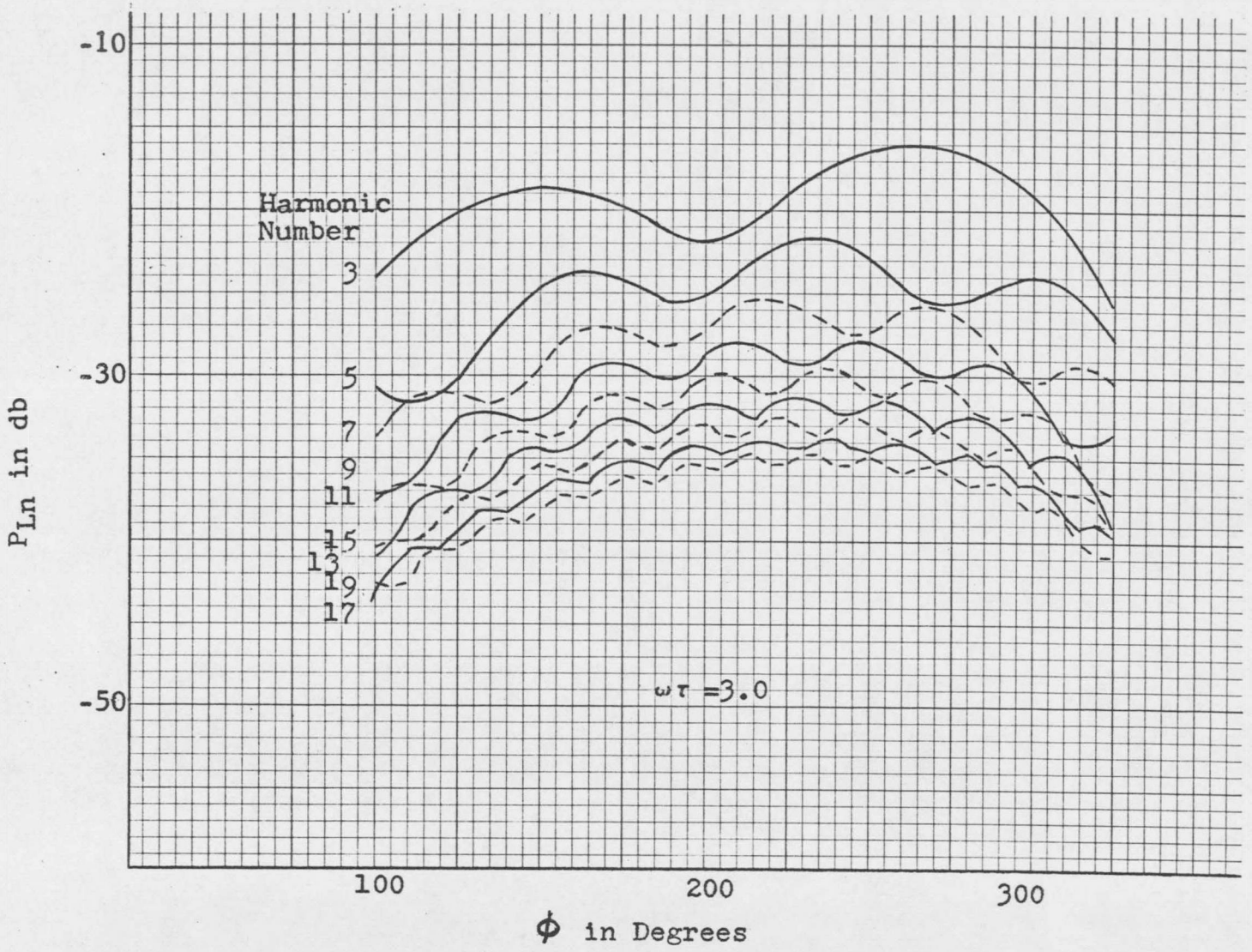


Fig. 4-27. CONVERSION LOSS vs Φ n ODD.

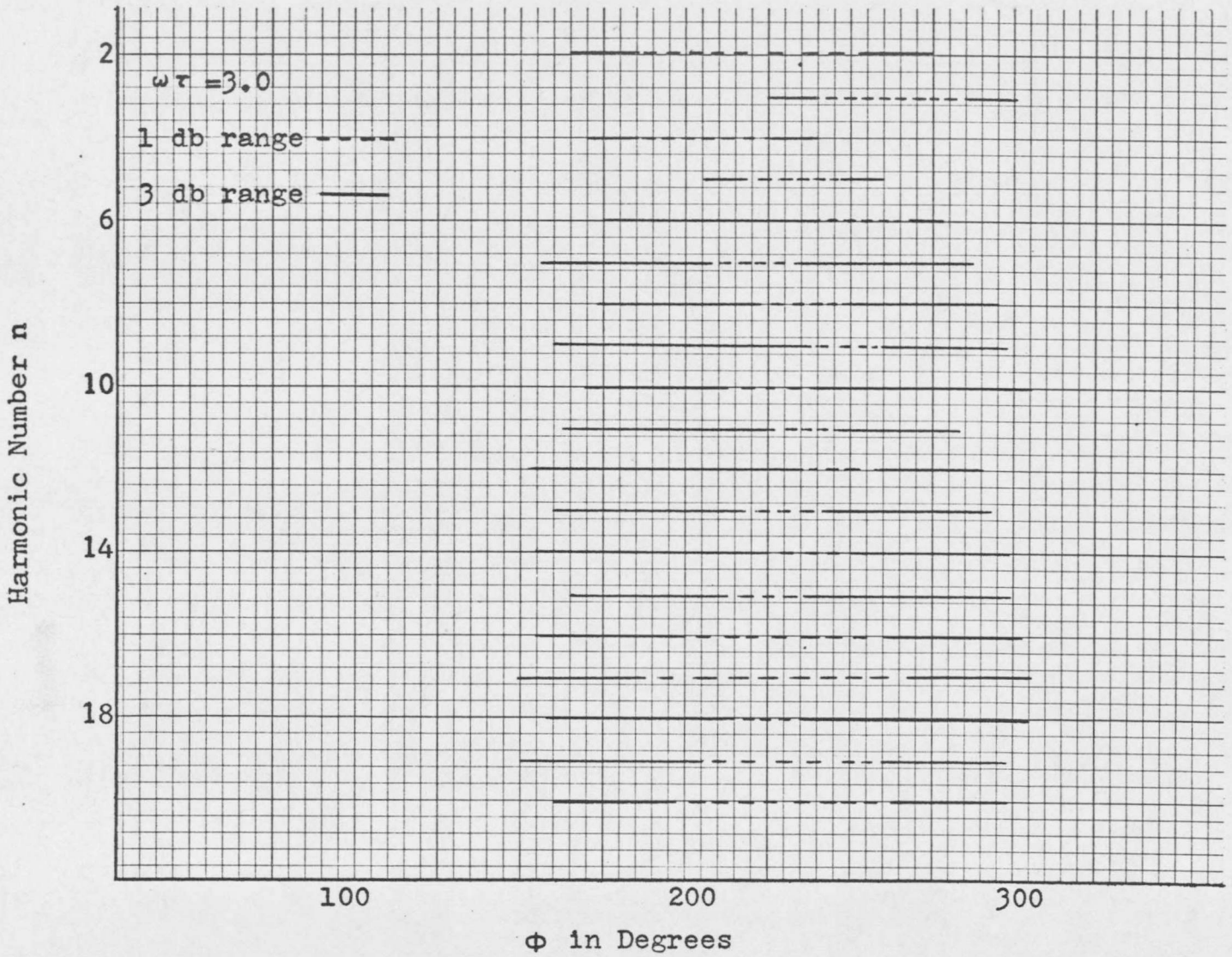


Fig. 4-28. RANGE OF Φ .

Table 4-1

RANGE OF ϕ

$\omega\tau$	1 db		3 db	
1.0			175-255	$n \geq 8$
3.0	225-235	$n \geq 13$	175-275	$n \geq 6$
10.0	225-240	$n \geq 10$	175-280	$n \geq 6$
100.	225-240	$n \geq 10$	175-280	$n \geq 6$
1000	225-250	$n \geq 9$	175-280	$n \geq 6$

resonance. An analysis of this type of multiplier [17] has been presented which allows its performance to be determined. The discussion that follows will parallel this analysis with several graphical additions which give a clearer understanding of circuit parameter variation on multiplier performance.

The equivalent circuit for the harmonic generator with a resonant load is shown in Fig. 4-29. In this analysis, only exponentially decaying sinewave outputs are considered. The circuit shown consists of an ac driving source and source resistance R_g in series with a bias source V driving the SRD diode and the parallel resonant circuit. The diode for this analysis is considered to be an ideal nonlinear capacitor. For $\omega\tau > 10$ this idealization is reasonable.

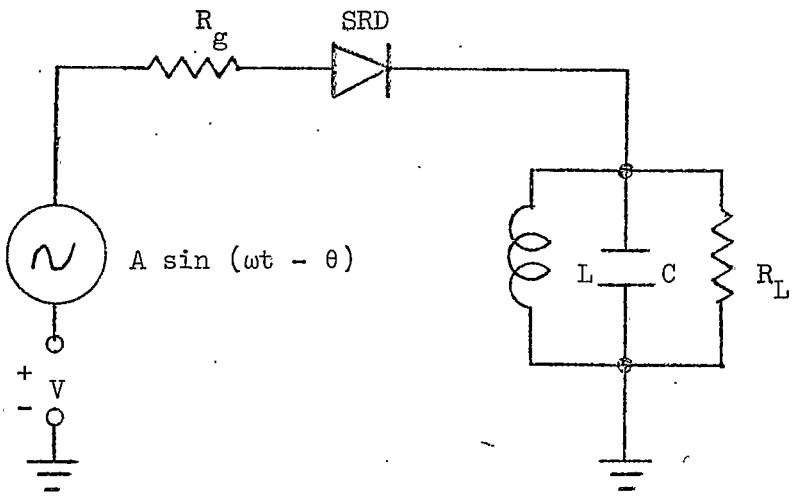


Fig. 4-29. EQUIVALENT CIRCUIT OF HARMONIC GENERATOR WITH A RESONANT LOAD.

Harmonic energy is generated by this circuit in the following sequence. When the diode is forward biased, current flows through the circuit. Diode conduction is sustained until the charge that has passed through it becomes zero. The diode then ceases to conduct leaving a current, I, flowing in the inductance L. With the diode cut off the energy stored in the inductance is dissipated in the load. It is assumed that the circuit starts from rest for each conduction state. This requires that the energy in the resonant circuit be dissipated by the time the next conduction interval begins.

The analysis of this multiplier is given in Appendix E. Two conversion efficiencies are defined, which when combined yield the

overall performance of the multiplier. One efficiency is defined in terms of the conduction characteristics and is expressed as

$$P_{L1} = 10 \log \left[\frac{\pi}{2Q_1 I^2} \right] \text{ db} \qquad (4\text{-}8)$$

where

$Q_1 = \frac{\omega L}{R_g}$

E = amplitude of driving source

R_g = generator source resistance

I = current in the inductance at the end of the diode conduction.

Values for this relationship were computed, for Q_1 values between .1 and 80, as a function of ϕ. The results are presented in Fig. 4-30 and Fig. 4-31.

The relationship between θ (angle of diode current initiation) and ϕ (angle at which diode current ceases) is given in Fig. 4-32.

The second conversion efficiency is defined in terms of non-conducting state and for the desired harmonic is expressed as

$$P_{L2} = 1.96 - 10 \log \left[\frac{Q_2}{n} \left[1-e^{-n/Q_2(\pi-\phi/2)}\right]^2 \right] \text{ db.} \qquad (4\text{-}9)$$

where

$Q_2 = n\omega C R_L$

n = harmonic number

$n\omega = (L C)^{-1/2}$

Values for this relationship were computed, for Q_2/n values between .2 and 2 as a function of ϕ. These results are presented in Fig. 4-33.

From Fig. 4-30, 4-31, and 4-33 the overall conversion loss, P_T, for the harmonic generator can be determined by adding the two appropriate conversion losses for a given conduction requirement. From ϕ the value of θ can be determined and therefore, the bias voltage V.

From the computed values, conversion loss characteristics as functions of Q_1 and Q_2/n were determined. These characteristics are plotted in Fig. 4-34 and 4-35. It can be seen from these curves that the minimum value of P_T is 8.5 db. This minimum occurs for $Q_1 \cong 1.2$ and $Q_2/n \cong 0.8$. In designing multipliers of this type, these two sets of curves may readily be used to set limits on circuit values to be used where an acceptable P_T is specified.

In the design of a multiplier, variation of the conduction characteristic ϕ and the resulting performance degradation are of considerable interest. Table 4-2 presents the degradation expected for stated range of ϕ and specific values of Q_1. This table was generated by considering all values of Q_2 between 0.1 and 2.0 and letting the corresponding minimums set the range of ϕ to be considered. This table then places a lower tolerance level on each curve of Fig. 4-35.

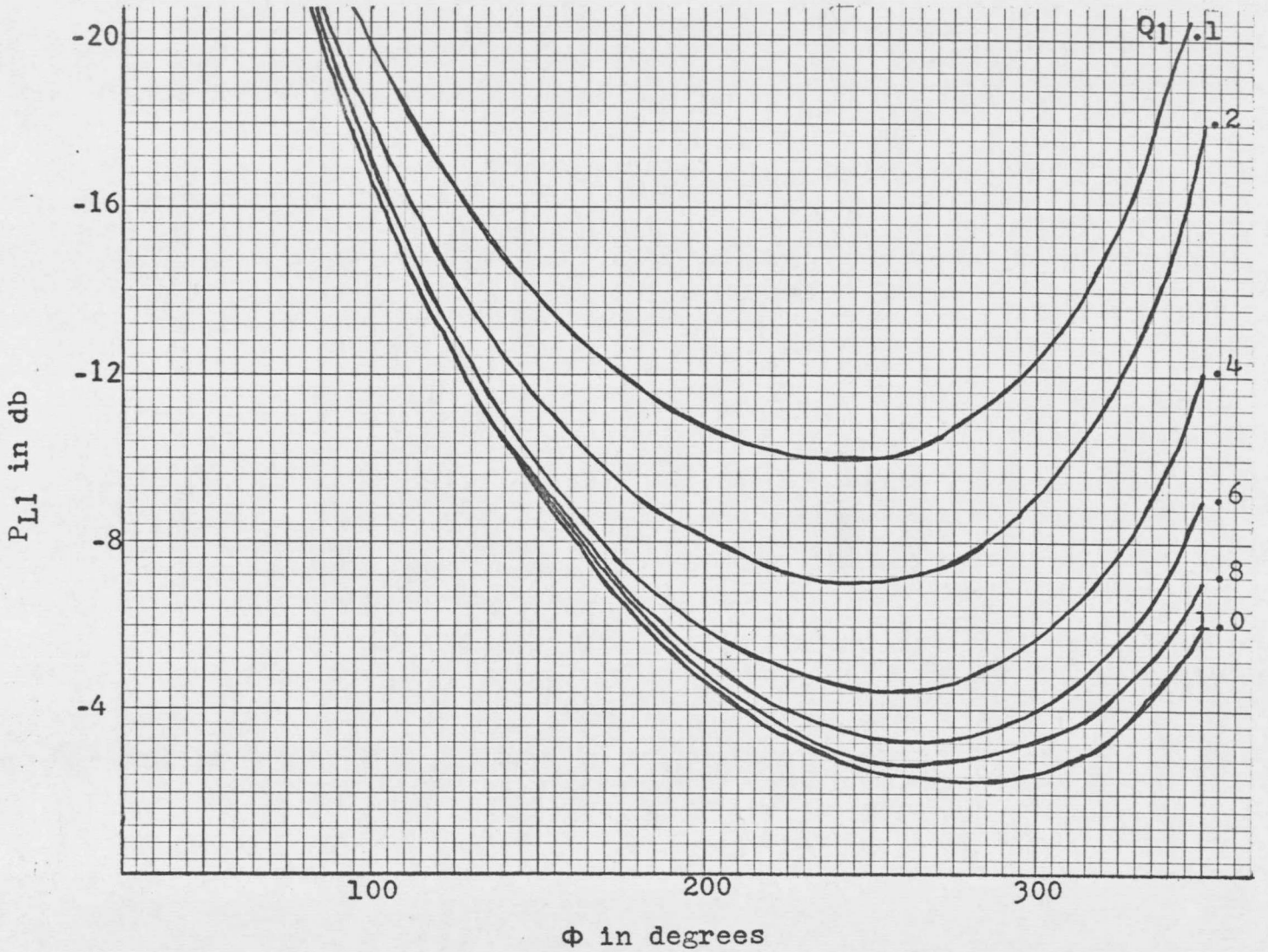


Fig. 4-30. CONVERSION LOSS Q_1=.1 to 1.0 R-L SERIES CIRCUIT.

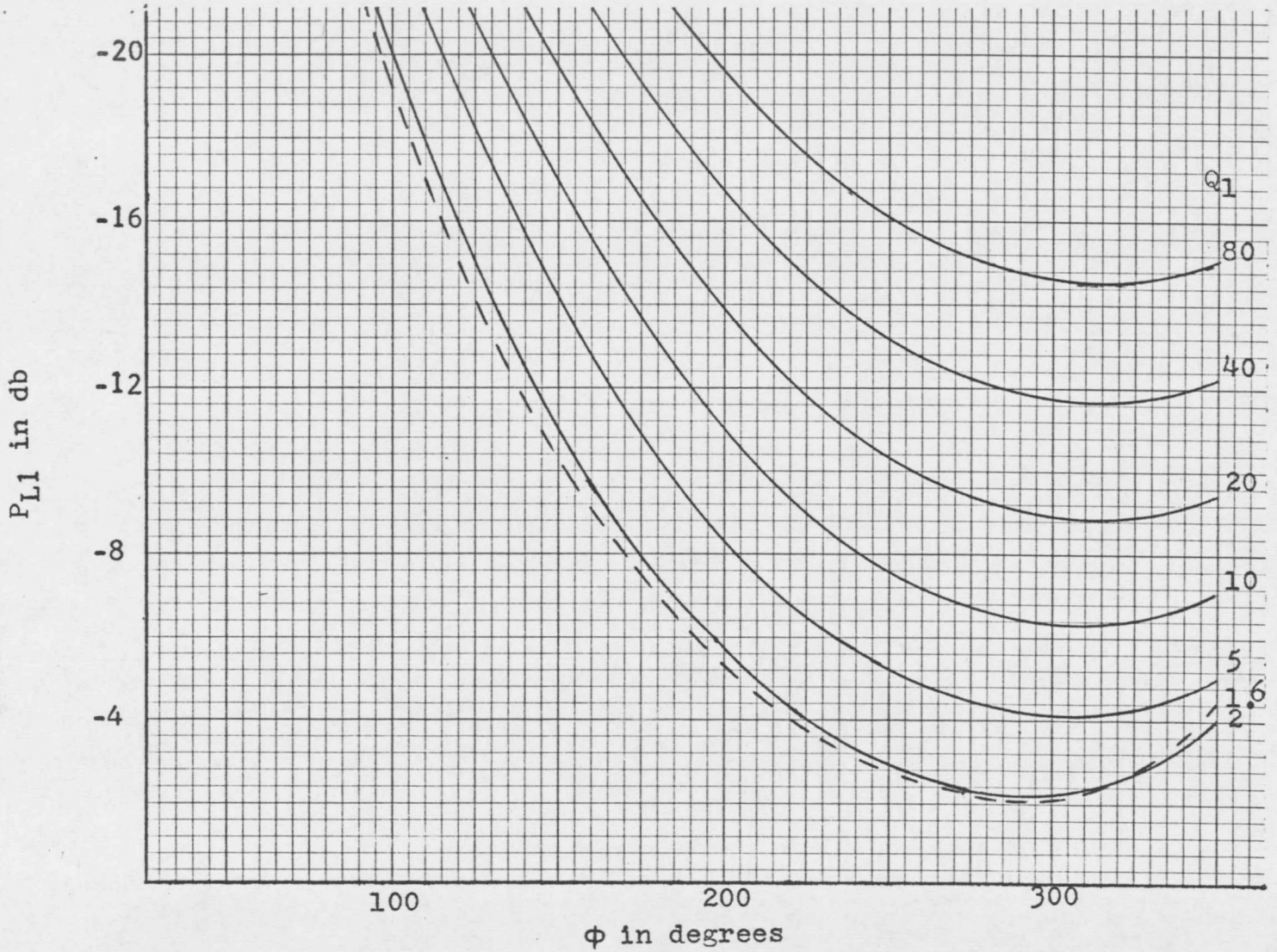


Fig. 4-31. CONVERSION LOSS Q_1-1.6 to 80 R-L SERIES CIRCUIT.

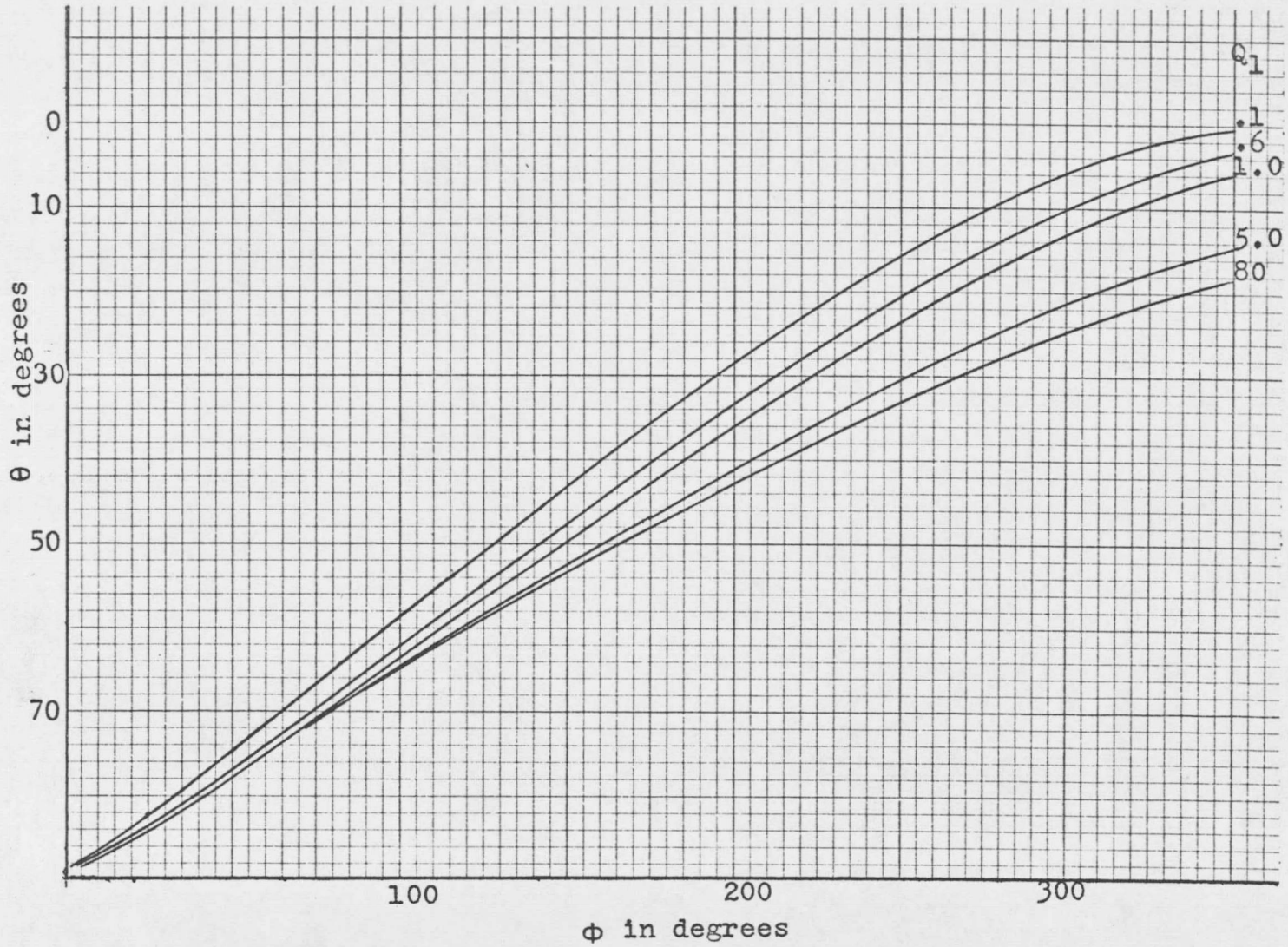


Fig. 4-32. θ AND Φ CONDUCTION CHARACTERISTICS.

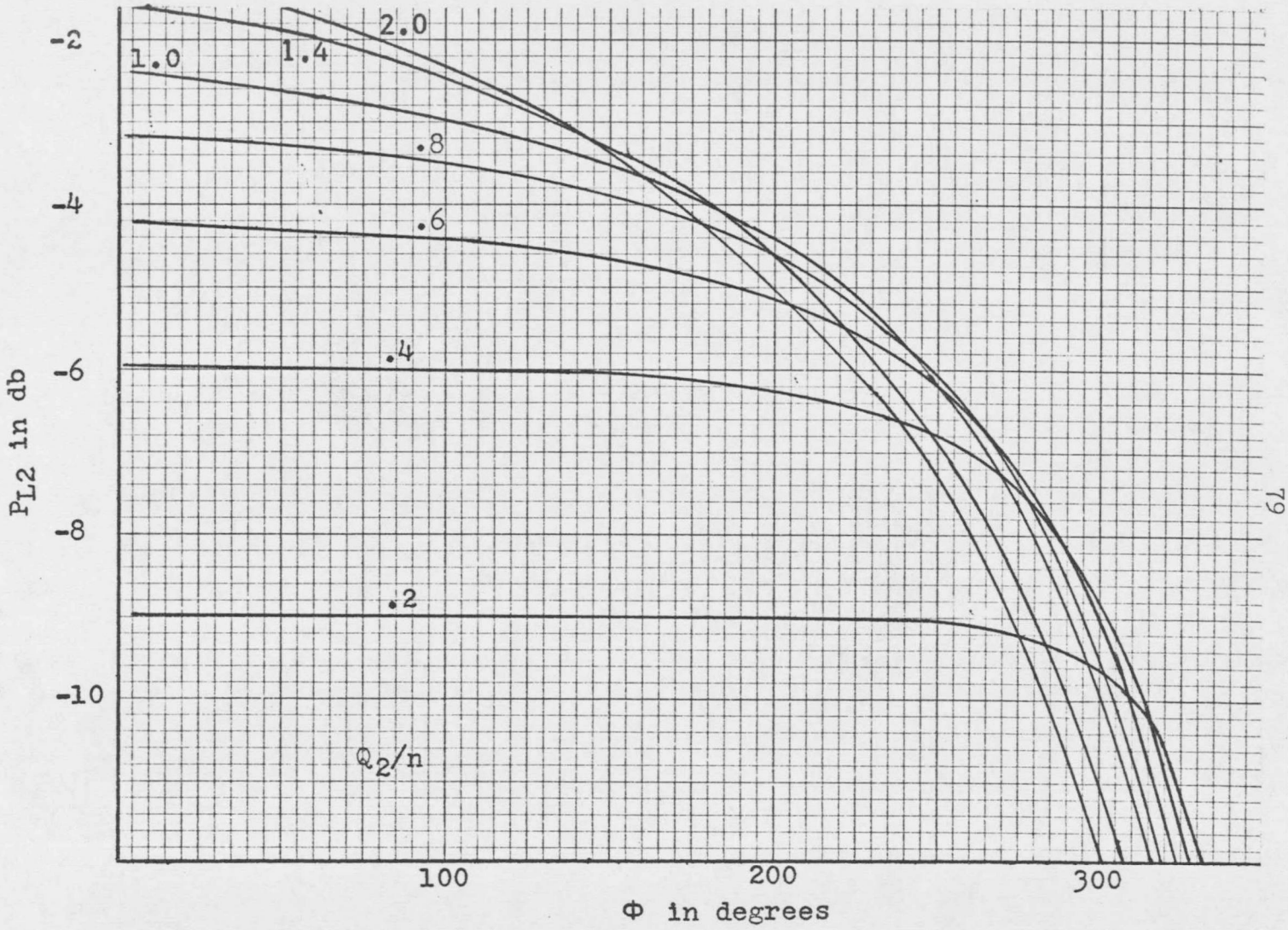


Fig. 4-33. HARMONIC POWER LEVEL RLC PARALLEL CIRCUIT.

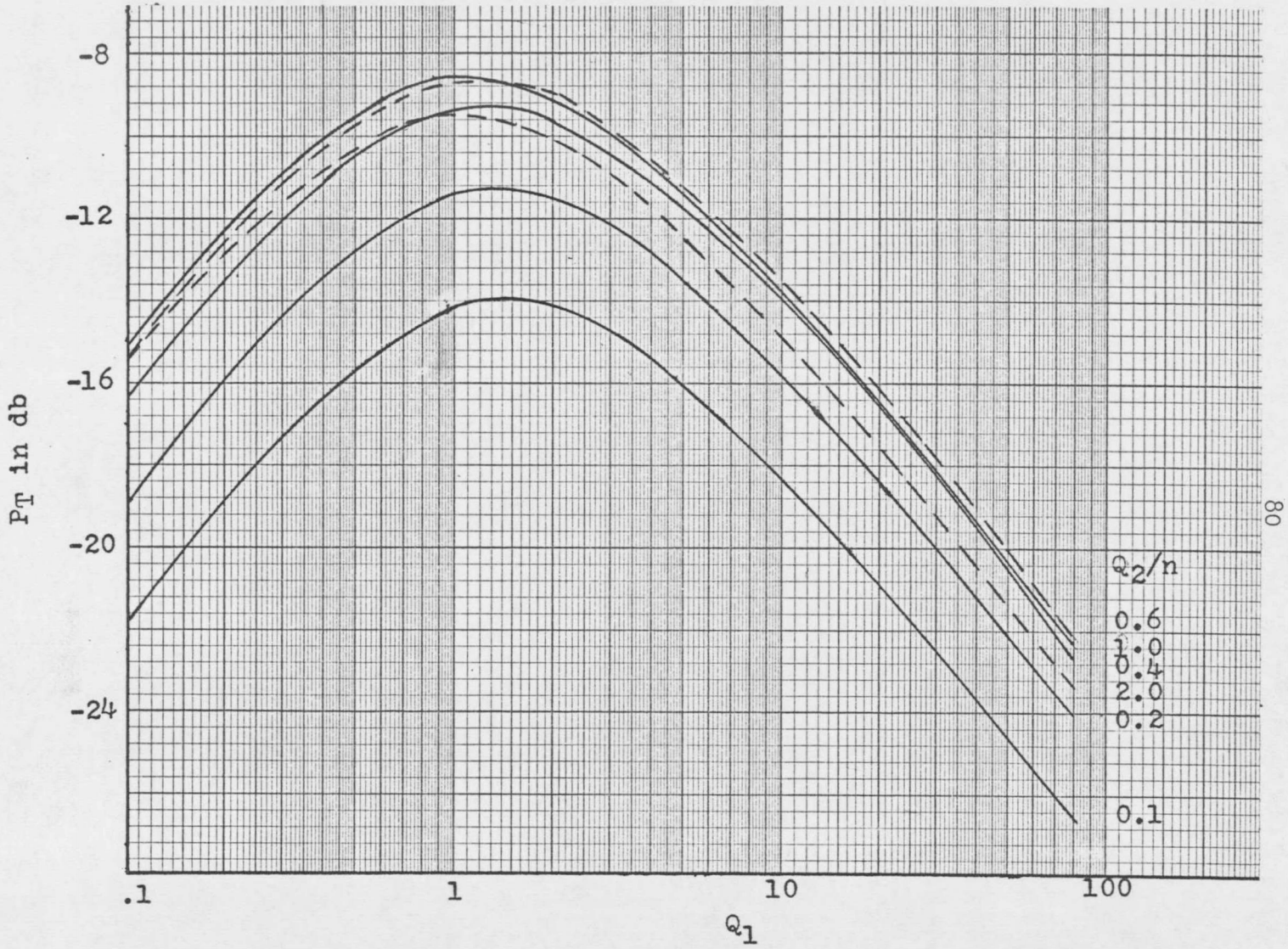


Fig. 4-34. MINIMUM CONVERSION LOSS AS A FUNCTION OF Q_1.

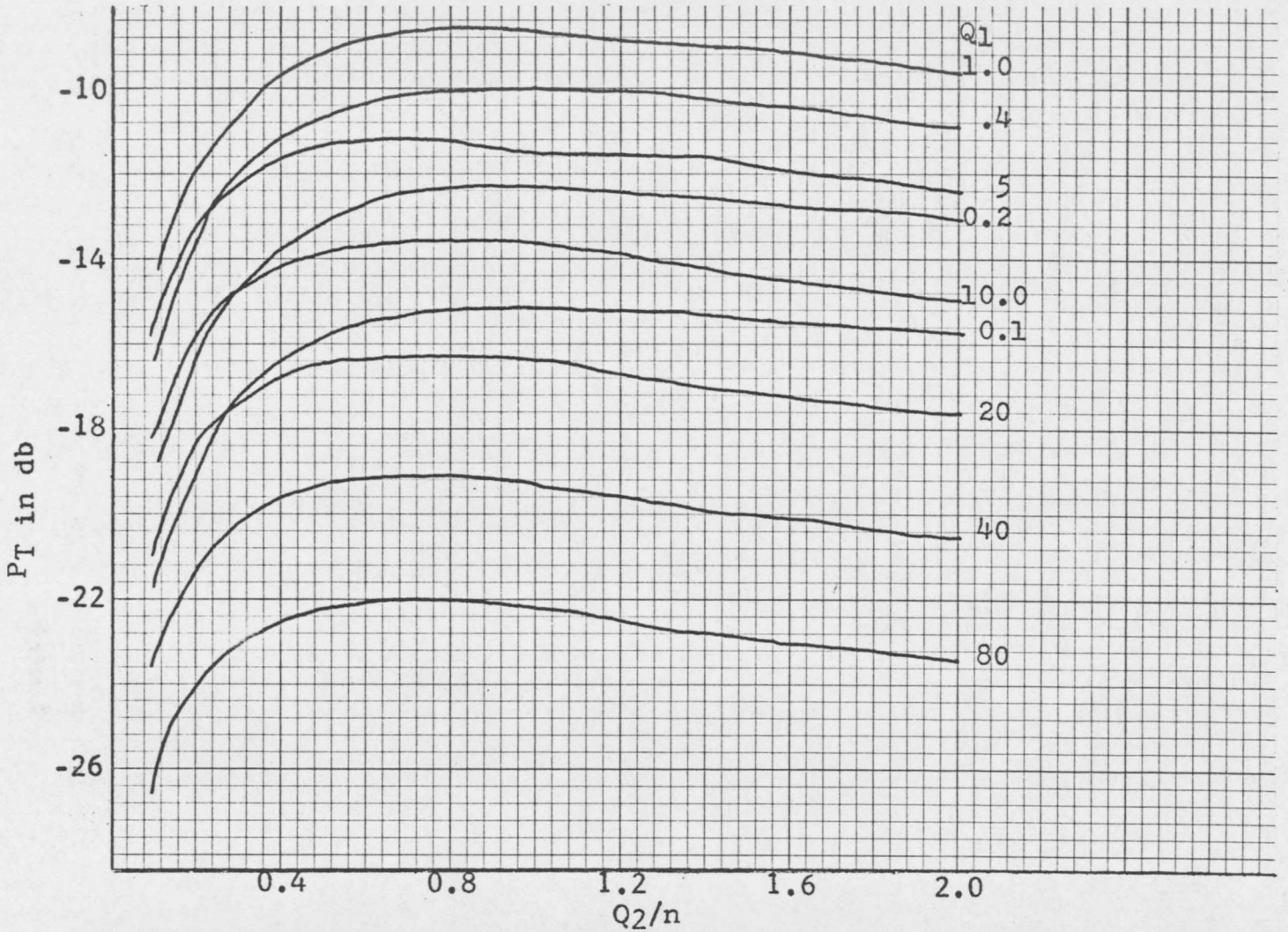


Fig. 4-35. MINIMUM CONVERSION LOSS AS A FUNCTION OF Q_2/n.

Table 4-2

OVERALL CONVERSION EFFICIENCY DEGRADATION

Q_1	Variation (deg.)	P_T Variation (db)
0.1	240-200	1.0
0.2	245-205	1.13
0.4	255-210	1.33
0.6	265-215	1.66
0.8	270-220	1.75
1.0	275-225	1.92
1.2	280-225	2.15
1.4	285-225	2.47
1.6	285-230	2.34
1.8	290-230	2.74
2.0	290-235	2.65
5.0	300-240	3.24
10.0	305-240	3.68
20.0	305-240	3.58
40.0	305-240	3.53
80.0	305-240	3.5

4.3 DIVISION

A variety of circuit techniques have been used for many years to provide frequency division. These techniques are classed under

the categories of relaxation, counter, or sinusoidal devices.

The relaxation divider accomplishes division by the premature termination of its natural period due to the injection of a signal to be divided in such a manner that synchronization is maintained. Reliable operation of the relaxation divider is limited to frequencies of several MHz.

The digital counter operation is normally that of a frequency divider. The counter output is generated as a function of the required number of input pulses. The advantage of this type of divider is that of wide integral division ratios and ease of changing this ratio either electronically or by switches. At present the upper frequency limit of these dividers in solid state integrated packages is 150 MHz.

Sinusoidal dividers are used for division at higher frequencies. The regenerative dividers, locked oscillator divider and parametric diodes are employed at the higher frequencies. In general the operational frequency range of these dividers is limited by the tuned circuits employed. The locked oscillator divider has the advantage of simplicity over the regenerative divider and some forms of the parametric divider but has the major disadvantage of providing an output with the loss of the synchronizing signal.

Parametric oscillators of the type which satisfy the Manley Rowe relationship discussed in Chapter 3 have been discussed by

Hilibrand and Beam [18] for order 1/2. This type of divider requires input and out filters tuned at frequency ω and $\omega/2$ respectively. Due to the filters, this divider has a limited operational frequency range.

Hedderly [19] and Ryan and Williams [20] present analysis for parametric dividers possessing wide operational frequency range. The results of their analysis are illustrated for the case of subharmonic oscillations of order 1/2. In the first analysis [19] infinite diode lifetime is assumed and in the second analysis [20] the analysis is for $\omega\tau \leq 1$. Analyses predicts octave operational frequency bandwidth. In both analyses the load and generator resistances are ignored.

In the broadband divider circuit presented in the next section both load and generator resistances are included. Analog computer simulations presented predict broadband operational frequency range for a division ratio of 1/2.

4.3.1 BROADBAND STEP RECOVERY DIODE FREQUENCY DIVIDER.

The divider presented in this section was an out-growth of several broadband input diode multiplier circuits and experimentation with the two broadband frequency dividers mentioned previously. The divider executes subharmonic oscillations of order 1/2 and has an operational bandwidth greater than an octave in frequency.

The circuit for the divider is shown in Fig. 4-36, and consists

of an ac generator in series with the reactive T-section of C and L's driving a SRD diode in series with the load resistance.

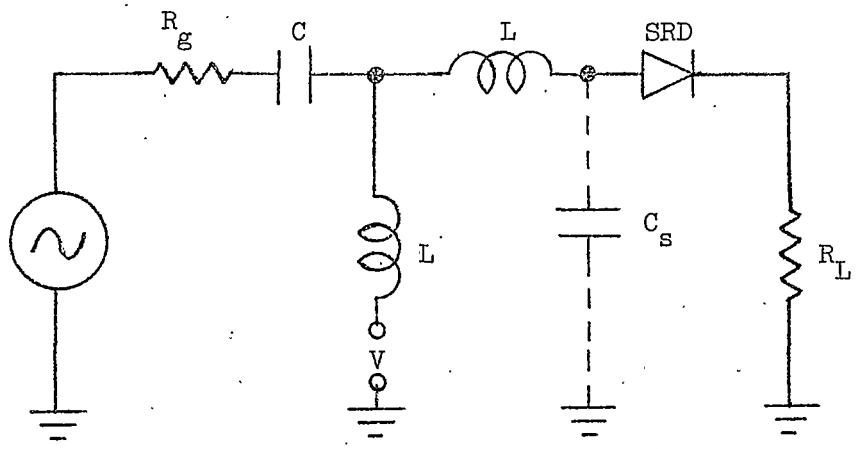


Fig. 4-36. BROADBAND DIVIDER EQUIVALENT CIRCUIT.

The more popular method of finding the solutions for the circuit equations in circuits of this type is to assume piecewise-linear operation. The method of approach is to assume a piecewise-linear representation of the nonlinear element, solve the circuit equations for the linear regions, and match these solutions at appropriate boundries of operation. The difficulty with this approach is that, while the equations in general may be easily set up, they are usually difficult to solve. This difficulty exists for systems with only one conducting and one nonconducting state.

For this discussion the SRD diode in Fig. 4-36 is assumed to be an ideal nonlinear capacitance. As discussed in Section 4.1, its operation is described in terms of the charge flowing through it and the voltage across it.

An attempt was made to solve the circuit equations describing the operation of the circuit of Fig. 4-36. While the equations are relatively easy to set up, a general solution for two linear regions of operation was not obtained. The analysis in general cannot be restricted to the case where all conducting and nonconducting states are, respectively, identical.

The divider circuit operational waveforms shown in Fig. 4-38 to 4-44 were obtained by analog computer simulation. v_1' appearing at the top of Fig. 4-38 to Fig. 4-43 is dv_1/dt. v_1' is the required input for the analog simulation and this waveform was recorded to provide a timing reference. The circuit of Fig. 4-37 was used to generate the set of system equations to be simulated. The exchange of circuit placement of R_g and C from that of Fig. 4-36 was required to remove an oscillation that appeared in the simulation of the circuit of Fig. 4-36. Also a value of capacitance has to be assumed for C_s, the stray-wire circuit capacitance.

An analysis of this divider given in Appendix F was used in the analog computer simulation. The values used for the two inductors, L, and the input capacitor, C, were calculated for divider action

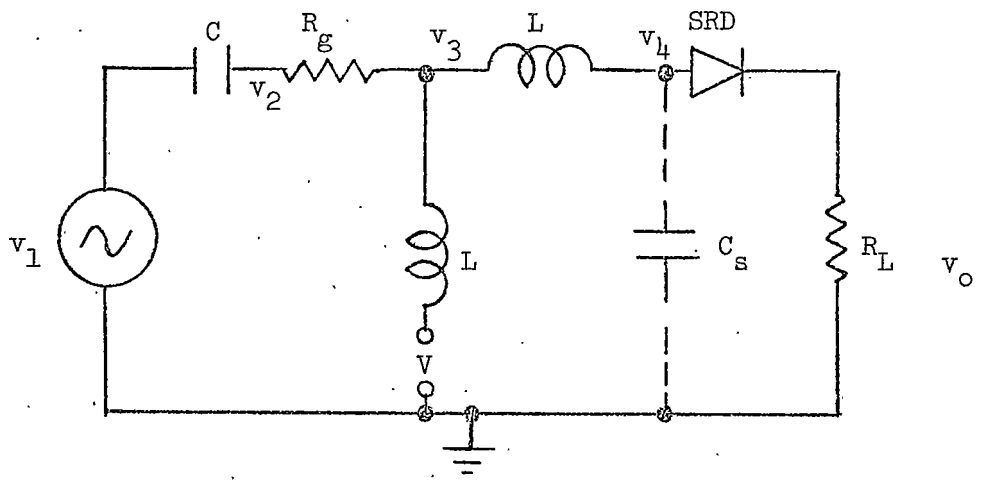


Fig. 4-37. DIVIDER EQUIVALENT CIRCUIT USED FOR ANALOG SIMULATION.

in the 500-1000 MHz frequency range. The value for the stray-wire capacitor, C_s, was assumed to be 2 pf.

The three frequencies of 500, 750, and 1000 MHz were selected to obtain typical circuit waveforms and operational power level. Fig. 4-38 and Fig. 4-39 show the divider waveforms associated with the circuit of Fig. 4-37 for an input frequency of 500 MHz. Fig. 4-40 and Fig. 4-41 present the 750 MHz circuit waveforms, and Fig. 4-42 and Fig. 4-43 present the 1000 MHz operation.

The operational frequency thresholds are shown in Fig. 4-44. At both end limit frequencies the circuit barely sustains the sub-harmonic oscillation.



Fig. 4-38. DIVIDER WAVEFORMS 500 MHz OPERATION.

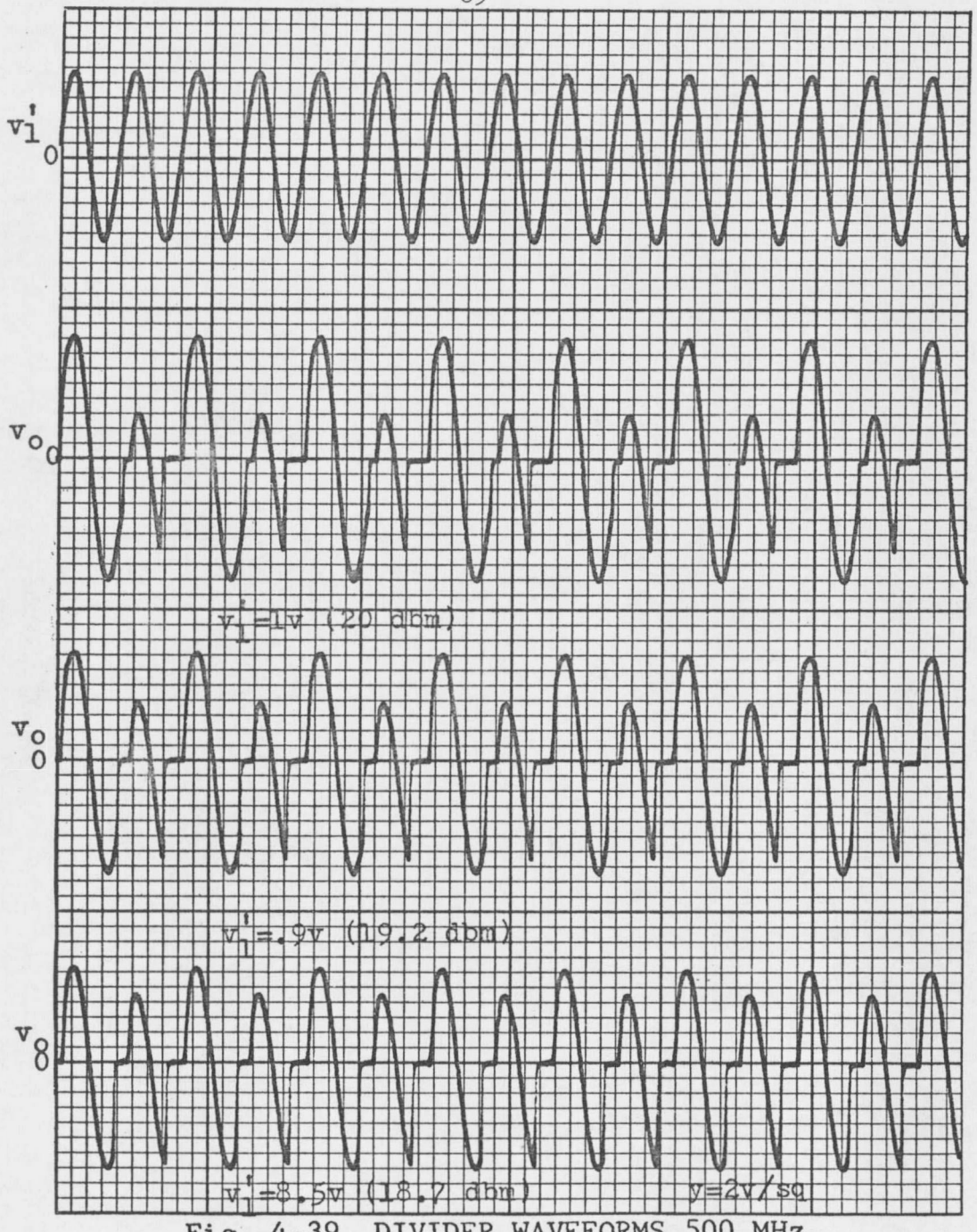


Fig. 4-39. DIVIDER WAVEFORMS 500 MHz

POWER - FREQUENCY CHARACTERISTICS.

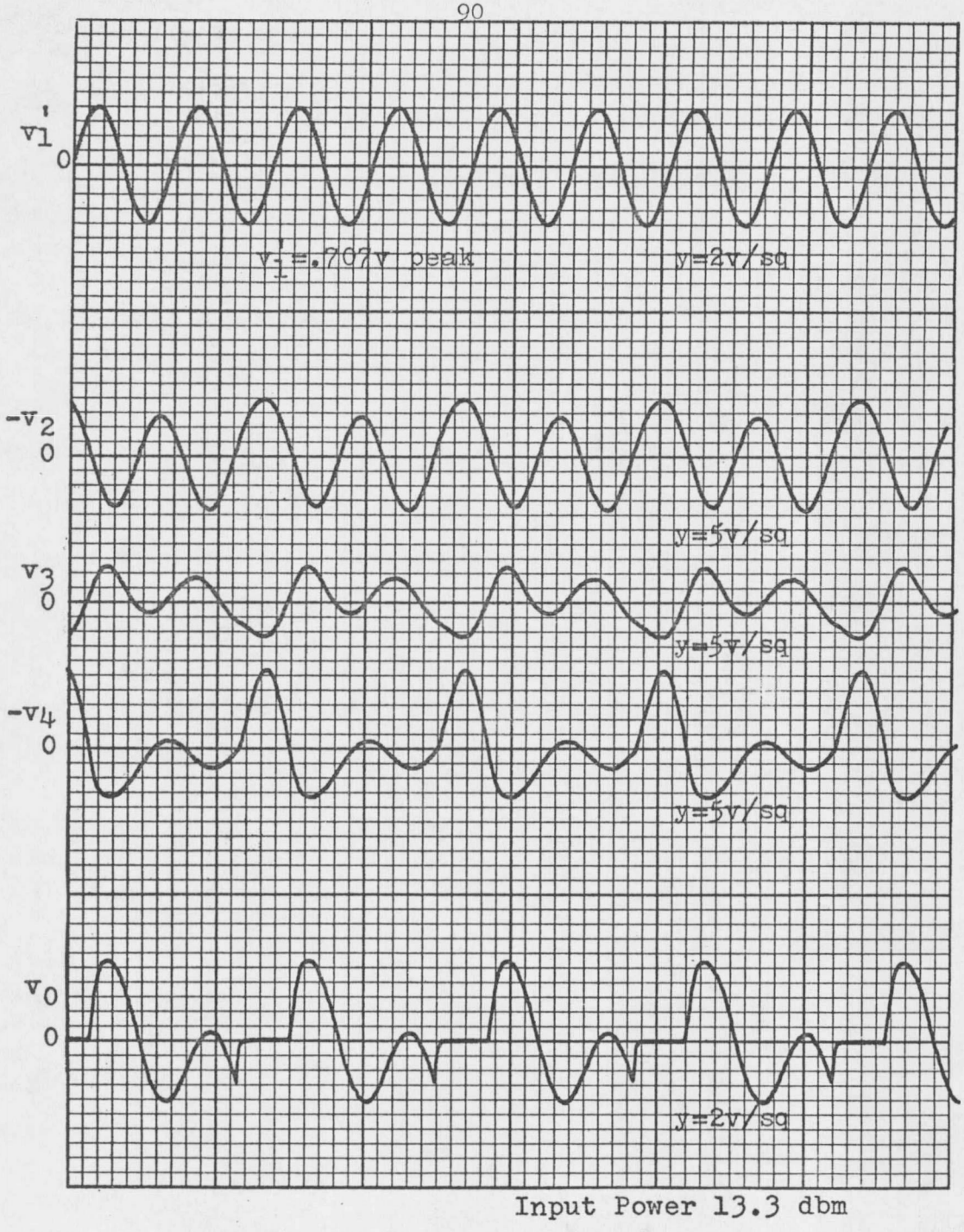


Fig. 4-40. DIVIDER WAVEFORMS 750 MHz OPERATION.

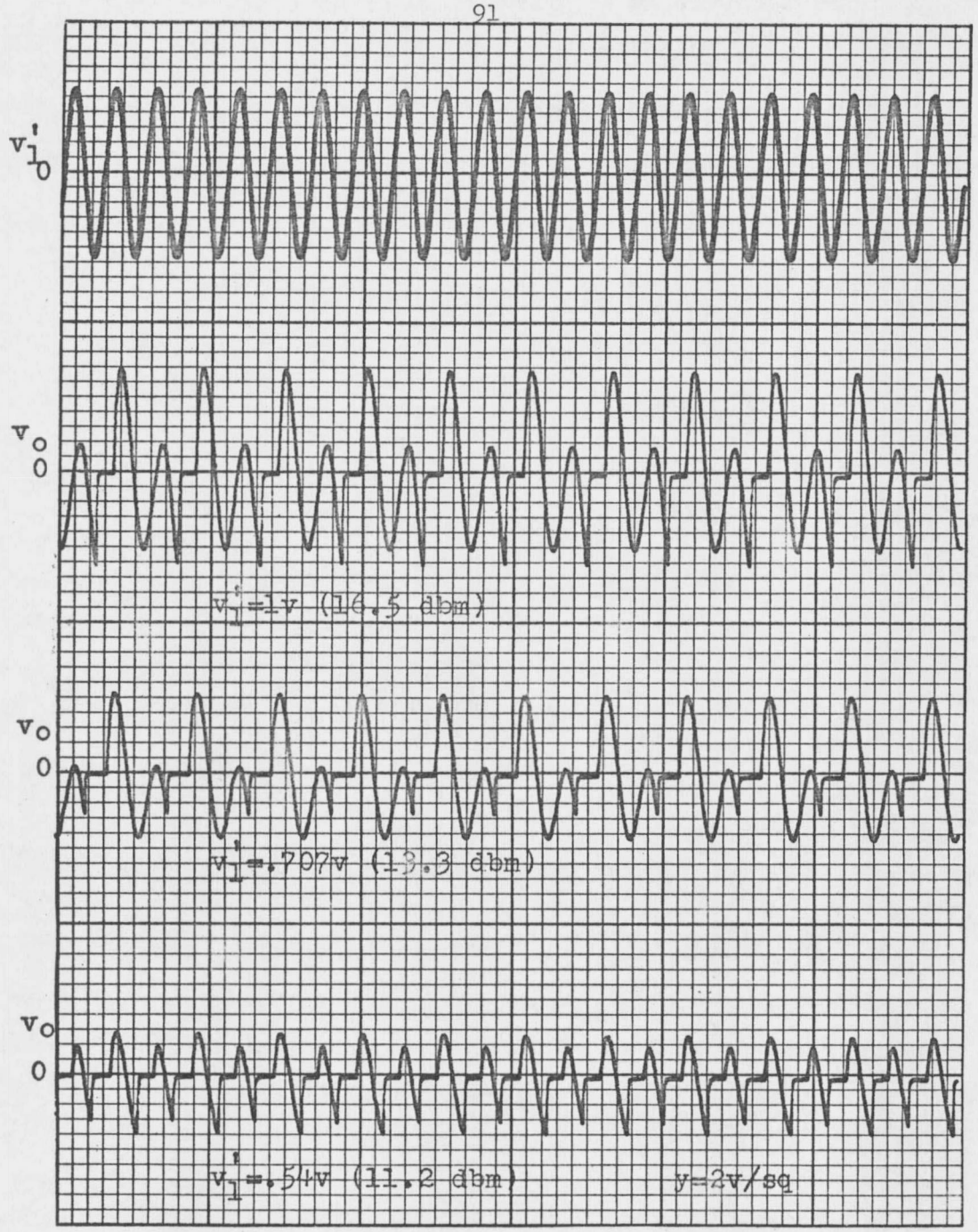
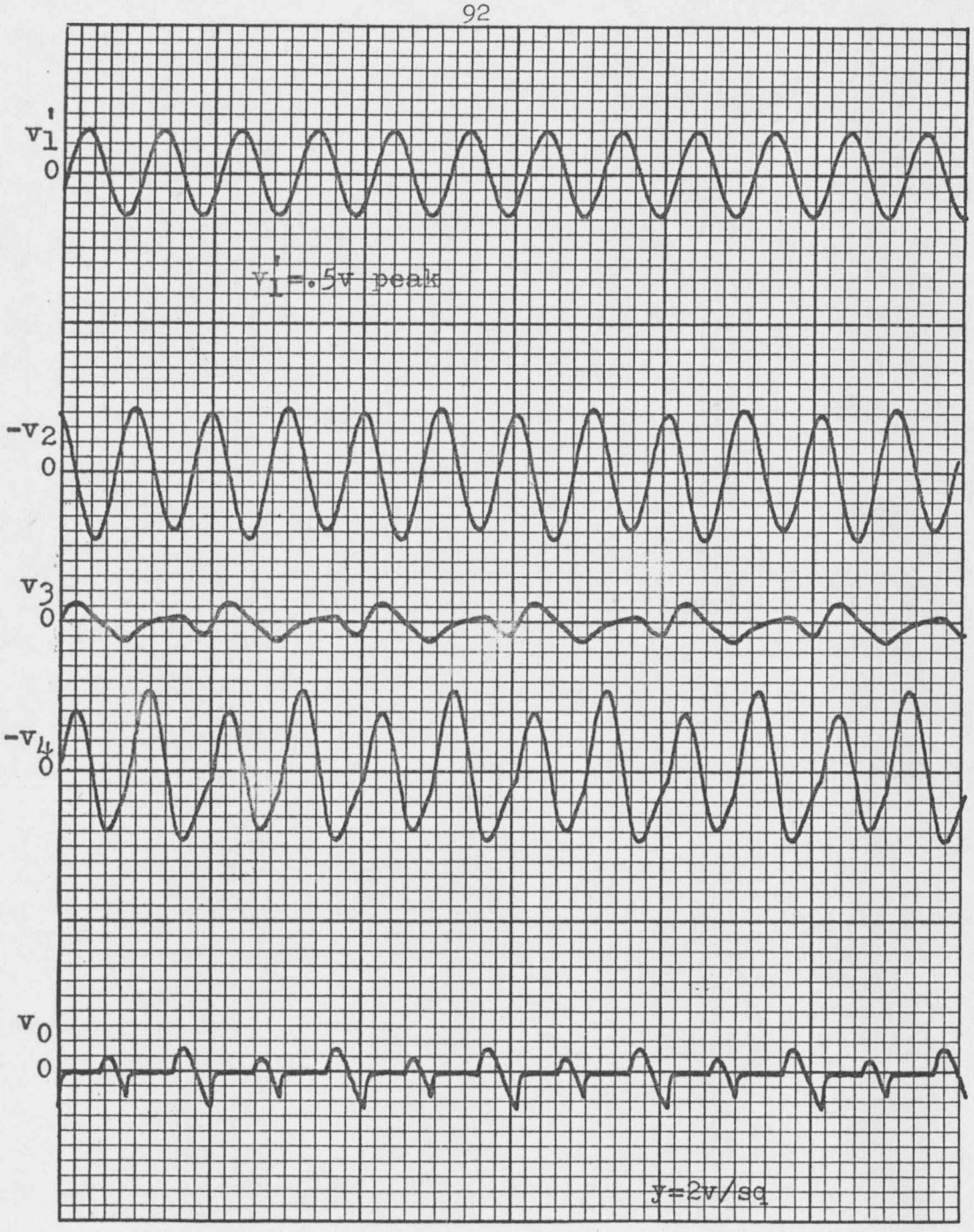


Fig. 4-41. DIVIDER WAVEFORMS - 750 MHz

POWER - FREQUENCY CHARACTERISTICS.



Input Power 8 dbm

Fig. 4-42. DIVIDER WAVEFORMS 1000 MHz OPERATION.



Fig. 4-43. DIVIDER WAVEFORMS - 1000 MHz POWER - FREQUENCY CHARACTERISTICS.

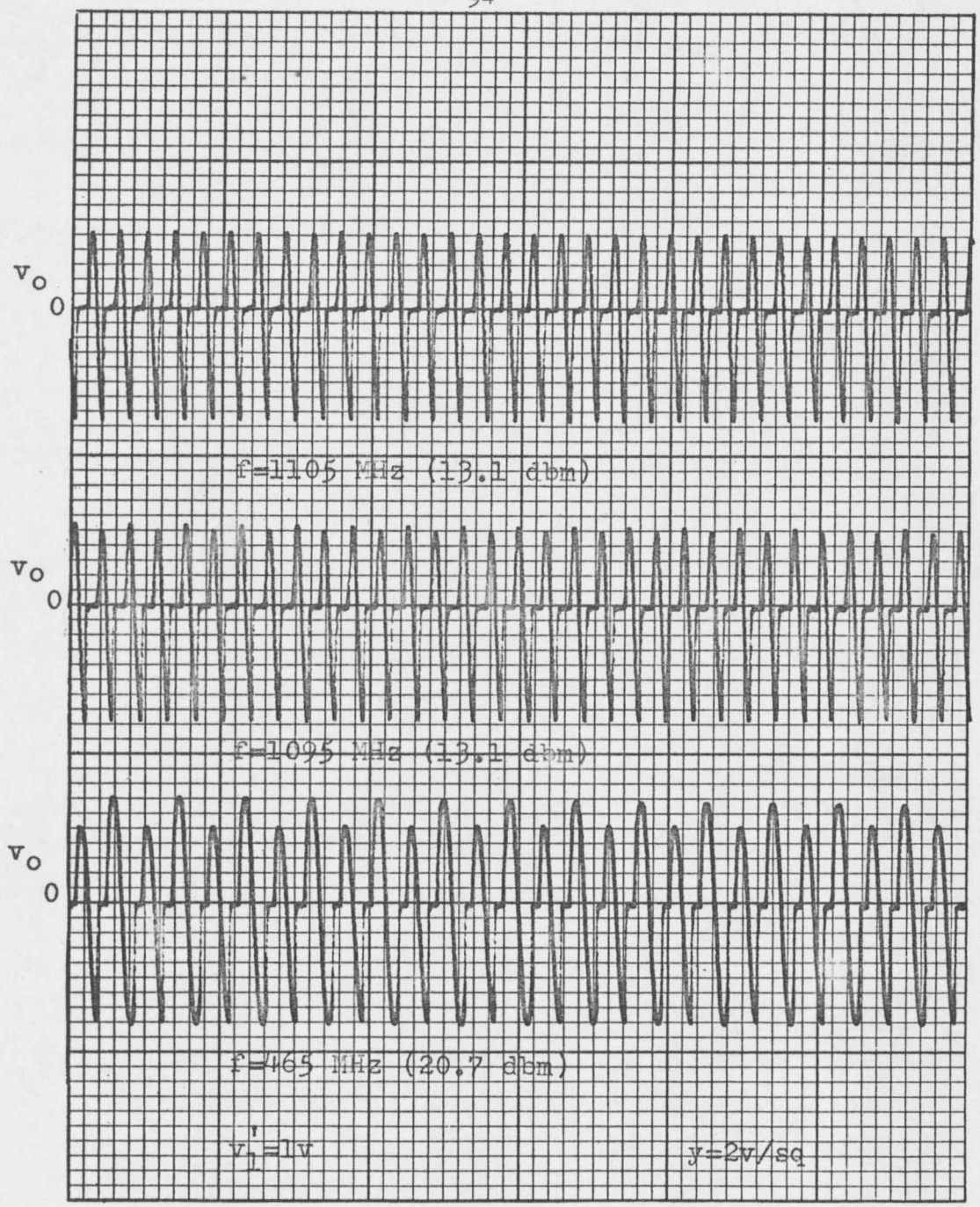


Fig. 4-44. DIVIDER FREQUENCY CHARACTERISTICS.

In all cases for the waveforms presented, the circuit was considered to be in a steady state condition while executing the subharmonic oscillation of order 1/2. The determination of the steady state condition was determined by visual monitoring of the computer output. In some cases, especially at the end limit frequencies, 15 to 50 cycles of the driving wave form were required before synchronism was established. Fig. 4-45 shows the operational power level range for two bias conditions. Power levels for proper divider action consist of the area between the two curves for a given bias condition.

In the design of a divider for a specific octave frequency range a method to determine the values of the two inductors and the input capacitor is required. The relationship used to determine the values of L and C are expressed as

$$L = \frac{1.41421\ R_g}{\omega_2}$$

$$C = \frac{1.41421}{\omega_2 R_g}\ , \qquad (4\text{-}10)$$

where ω_2 is the upper frequency of the octave range desired. The designer familiar with normalized filter coefficients will recognize the relationships of (4-10) as those of maximally flat low pass filter with equal resistance terminations.

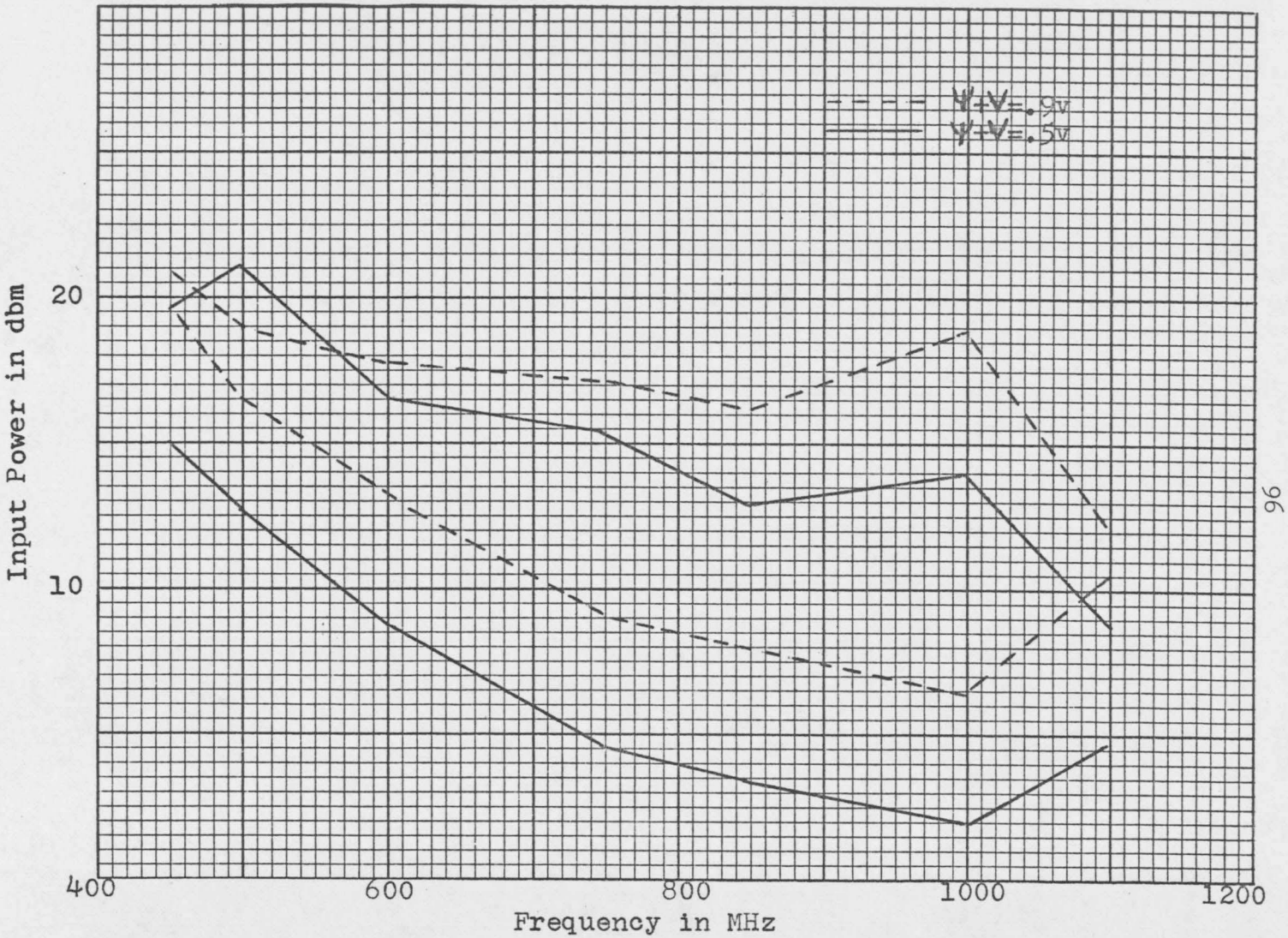


Fig. 4-45. DIVIDER OPERATIONAL POWER LEVEL.

4.4 TRANSLATION

In the case of frequency translation the isolation of the signal and translating frequencies in the mixer output may be adequately provided by means of filters to separate these unwanted signals from the desired signal. For the case requiring isolation of either or both of these frequencies, the singly and double balanced mixer are a means of easily providing the required rejection. The advantages of using the double balanced mixer were discussed in Chapter 3.

4.4.1 BROADBAND DOUBLE BALANCED MODULATOR.

The double balanced modulator performance was analyzed in the mixer performance discussions of section 3.2.4. The analysis presented in 3.2.4 pointed out the superior spurious component generation characteristics of this type of mixer over the common diode mixer and the singly balanced mixer. The characteristics of the double balanced modulator can be realized with many different combinations of transformers and diodes. The configuration shown in Fig. 3.4 for the modulator realization is one of the simplest forms.

The superior spurious level performance of this modulator relies on several factors. If the signal voltage unequally varies the current in the diode sets then unbalance will occur. If the translating signal is not a symmetrical waveform, an unequal current-time relationship will be introduced causing distortion products

even though the translating frequency remains balanced. The transformers used must have a high degree of balance, and this balance relies heavily on the physical symmetry of the transformers. The physical layout of the transformer becomes very important for high frequency operation. Balance of the diodes employed must be maintained over the entire forward conduction characteristic required. The modulator power-handling specification will dictate the magnitude of this range. Diodes used are of the rectifier type with minimum conduction storage characteristics.

The conversion loss for this double-balanced modulator is calculated in Appendix G. The calculation is made assuming a balanced circuit, ideal rectifier diodes and a square wave switching voltage. A conversion loss of 3.92 db is calculated for either of the desired sum or difference frequency products. This value will be used in comparing the performance of the modulators presented in Chapter 5.

5.0 EXPERIMENTAL RESULTS

The implementation and testing of the techniques of Chapter 4 was carried out to determine the practibility and repeatability of these techniques. It should be kept in mind that the combinations of the signal operations used in a synthesis scheme for one application will not necessarily be those employed for another, even though the frequency range of operation may be essentially the same. For example, in one system the efficiency of the rectifier diode harmonic generator (as inefficient as this method is) may be sufficient for the frequency multiplication requirements. In another system the efficiency required may dictate the uses of the harmonic generator with a resonant load which is either made up of switched filters of different center frequencies or one electronically tunable filter.

As will become apparent from the performance data presented, the frequency range of operation of the circuits tested is from 10 MHz through 2 GHz with the input circuit having maximum operational bandwidth. The reasoning behind this requirement is that broadband input circuitry eliminates operational tuning over a specified frequency range.

The diodes used in the construction of the rectifier harmonic generators and the full lattice modulator were of the hp 2900 type which employ a metal-silicon barrier junction and utilize electrons for majority carrier conduction. The low capacitance (C_o = 1.2 pf)

and short minority carrier lifetime allow the use of this diode from low frequencies through the UHF range.

The characteristics of the step recovery diodes used in the various multipliers and dividers are given in Table 5-1. The diode parameters tabulated are capacitance (C_o), effective minority carrier lifetime (τ), and transition time (t_t). The capacitance, C_o, is measured with zero applied voltage and a frequency of 1 MHz. The minority carrier lifetime is not a constant but is dependent upon both drive level and temperature. From the diode specifications this may increase 50% in the circuit investigated.

5.1 MULTIPLICATION.

In this section the experimental work that was performed with the various methods of obtaining frequency multiplication discussed in Chapter 4 are presented.

In order to obtain a very broadband coupling circuit, considerable effort was expended on development of a low-power transformer. Many different ferrite materials were investigated along with a variety of toroid dimensions and winding configurations. The material finally used was the 3E2A Ferrite material manufactured by Ferrocube. The large initial permeability (5000 at 25°C) of the 3E2A material requires fewer turns for a given low frequency response. Windings investigated consisted of a twisted pair of Formex wire for

Table 5-1

DIODE PARAMETERS

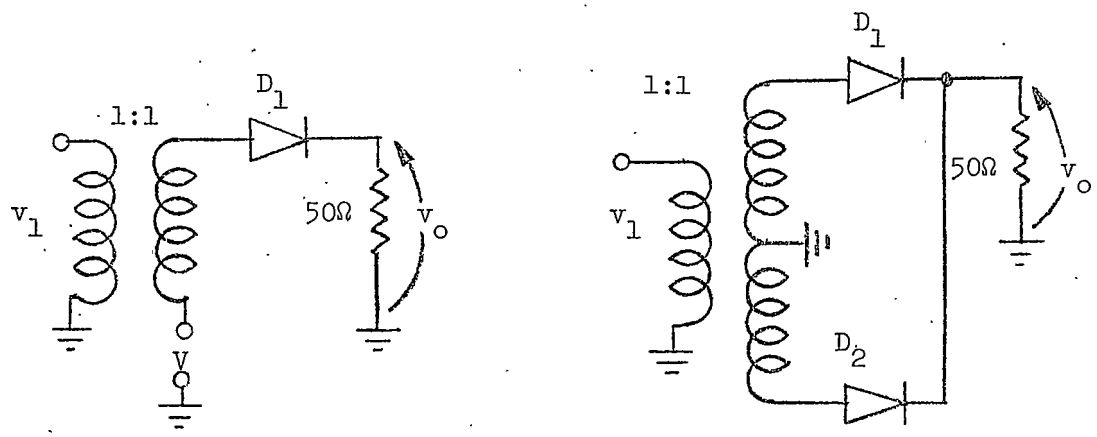
Type	C_o pf	τns(min)	t_t ns (max)
0102	20	100	2
0103	20	250	5
0112	3	50	0.3
0114	10	125	0.4
0151	1.6	20	0.15

the single primary-single secondary transformers and of twisted three-strand and parallel three-strand (fastened together in a triangular configuration) for the unbalanced-to-balanced transformers.

The parallel three-strand Formex #40 wire windings on a .190 outside diameter 3E2A toroid core gave the best results. For frequencies of operation below 10 MHz and up to several hundred MHz, 7 to 10 turns was found to provide the necessary coupling for efficient operation. For operation above 10 MHz, 3 to 4 turns was found to be sufficient.

5.1.1 RECTIFIER DIODE HARMONIC GENERATOR.

The two braodband rectifier diode harmonic generators constructed are shown schematically in Fig. 5-1. The diodes employed in these generators were the type hp 2900.



(a) Clipped Sine Wave Generator (b) Full Wave Rectifier Generator

Fig. 5-1. RECTIFIER DIODE HARMONIC GENERATOR CIRCUITS.

Data obtained for the clipped sine wave generator employing a 4-turn and 7-turn transformer are presented in Fig. 5-2 and 5-3, respectively, for an input power level of 20 dbm. The solid curves are drawn for the zero bias condition (V = 0). Comparison of these two data sets will show the high frequency superiority of the 4-turn transformer circuit over the 7-turn. The deviation of 4-8 db of the data presented in Fig. 5-2 from that predicted in Section 4.2.1 can be accounted for by considering transformer losses, circuit and diode capacitance and finite diode impedance under forward conduction.

The dashed curves were obtained by adjusting the bias voltage, V, to obtain optimum output at the harmonic being measured. Again the 4-8 db deviation from the predicted levels can be observed.

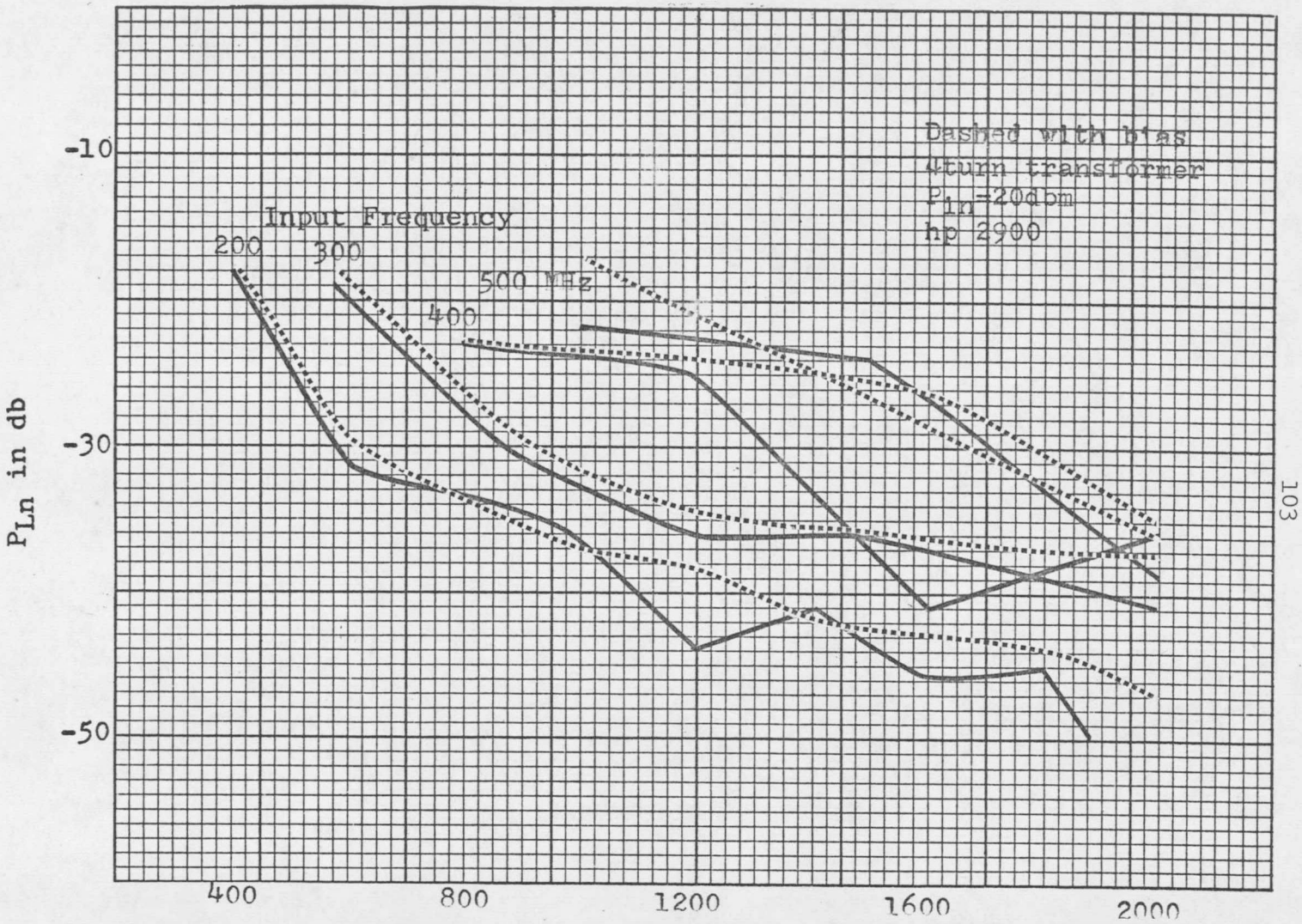


Fig. 5-2. CLIPPED SINE WAVE HARMONIC GENERATOR OUTPUT.

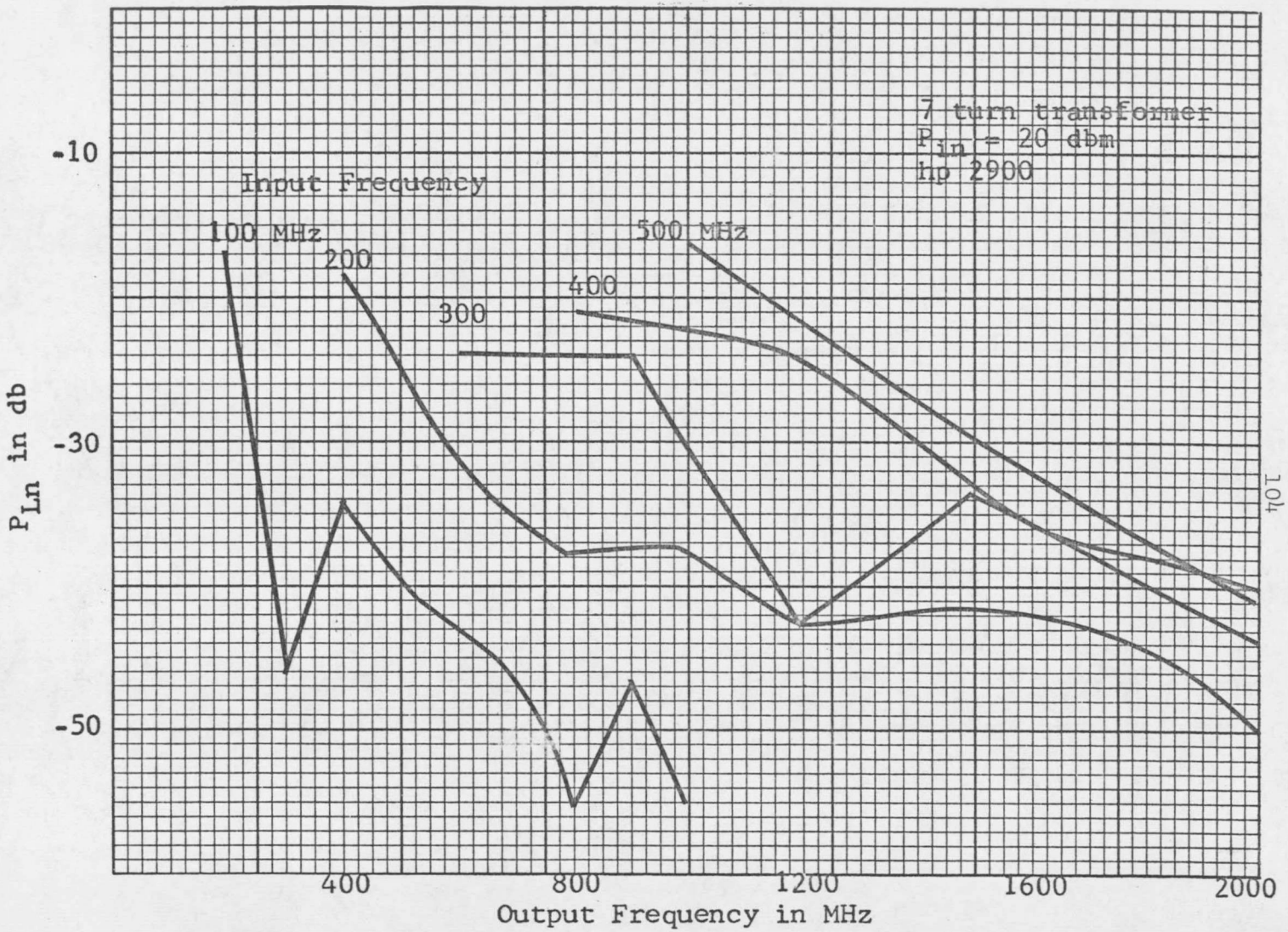


Fig. 5-3. CLIPPED SINE WAVE HARMONIC GENERATOR OUTPUT.

For the measurements made on this generator and in general for all the various experimental circuits tested refer to Fig. 5-4.

The desired power level from the signal source is adjusted by monitoring the voltage across the 50 ohm load. With the desired maximum available level set, the signal is applied to the device under test. The output is then monitored on either a spectrum analyzer or a sampling oscilloscope. The two attenuators are used to insure that the output impedance of the generator and the terminating impedance are both approximately 50 ohms.

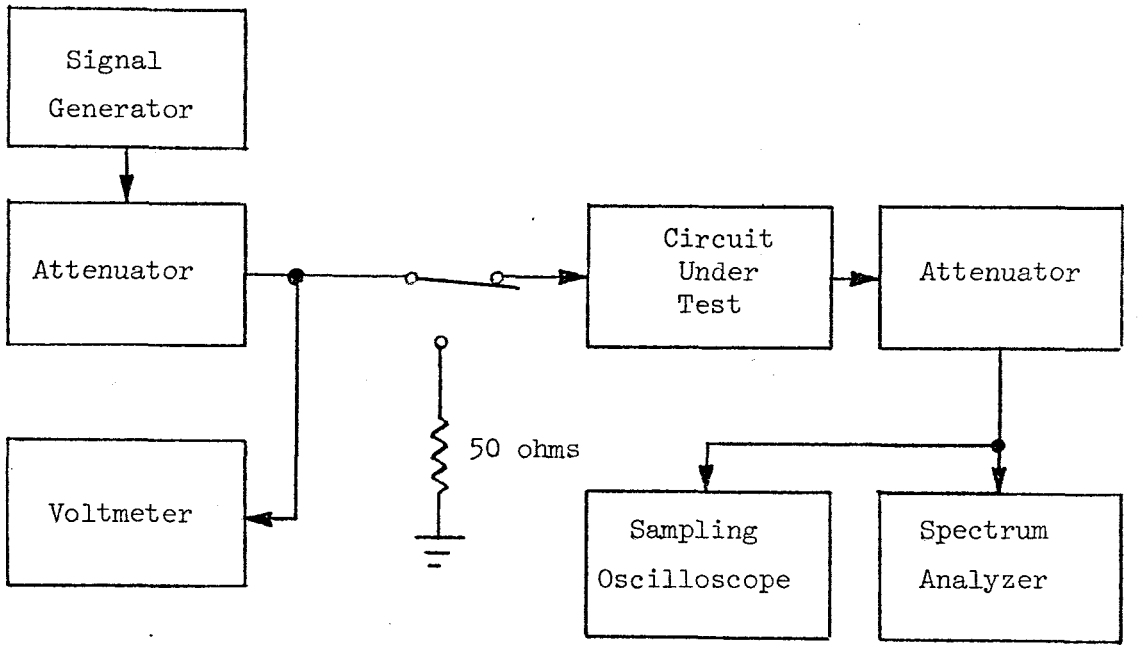


Fig. 5-4. MEASUREMENT DIAGRAM.

Data obtained for the full wave rectifier generator is presented in Fig. 5-5 and Fig. 5-6 for 8-turn and 3-turn transformer windings respectively. From the data presented the second harmonic conversion loss is typically 15 db or less for input frequencies through 700 MHz. The suppression of the fundamental and third harmonic are at least 18 db and 25 db below the output power level respectively.

The output level available over the efficient doubling range approximately 5 to 6 db from the 8 db loss predicted in section 4.2.1. This deviation can be accounted for in the same way as the clipped sine wave case.

The effect of the input impedance variation for the full wave rectifier generator is shown in Fig. 5-7. The curves present the variation of the input level as measured at the input to the full wave circuit for three power levels. The reference levels (dashed curves) were set with a 50 ohm termination.

Both of the rectifier diode harmonic generator types constructed produce usable output spectrums through at least 1 GHz with reasonable agreement with the ideal prediction. Several different diodes or diode pairs were used to obtain the data presented along with interchange of transformers. The diode pairs were matched to less than 10 mv deviation from each other over a current range of 0-30 ma.

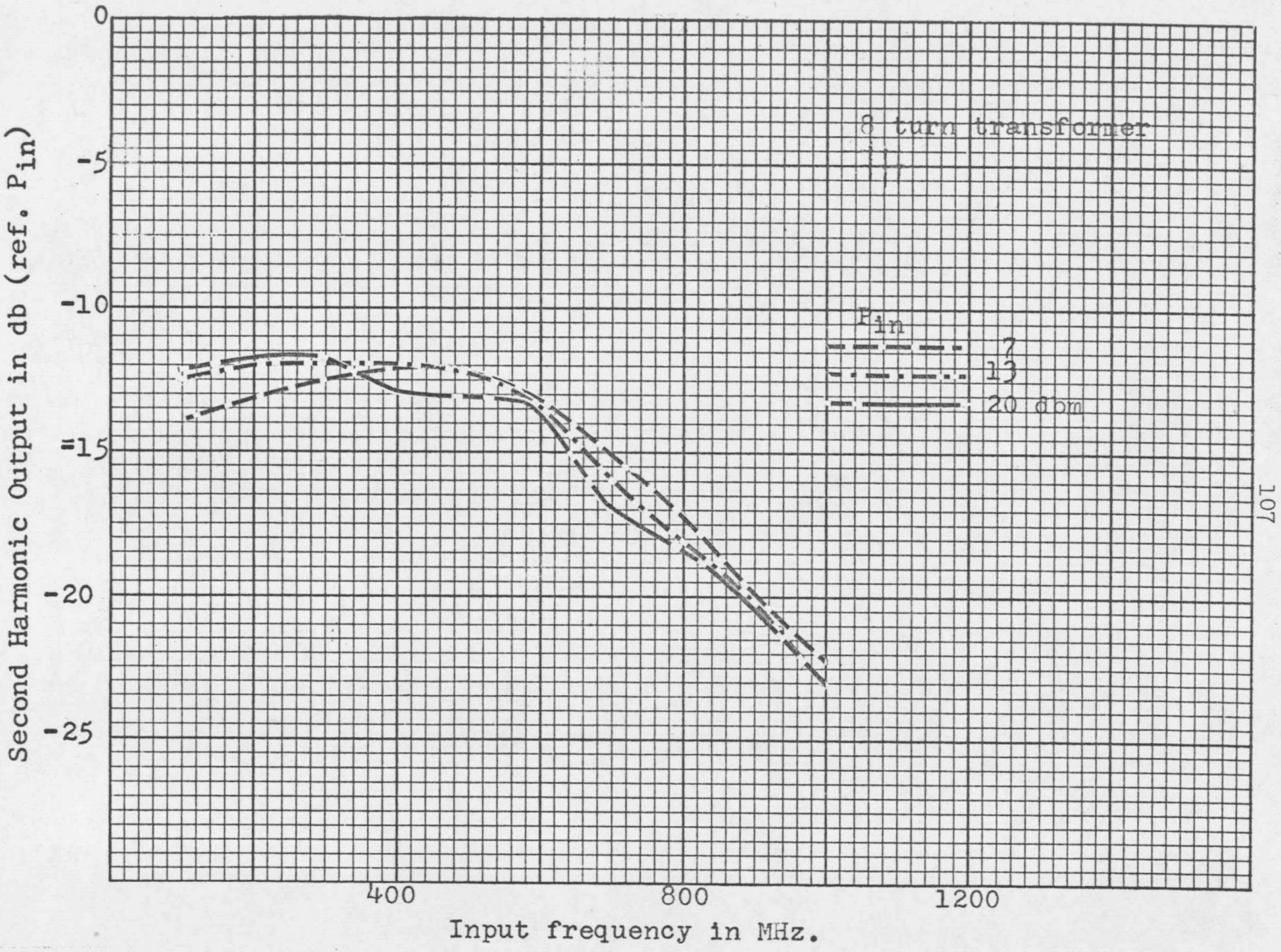


Fig. 5-5. FULL WAVE HARMONIC GENERATOR OUTPUT.

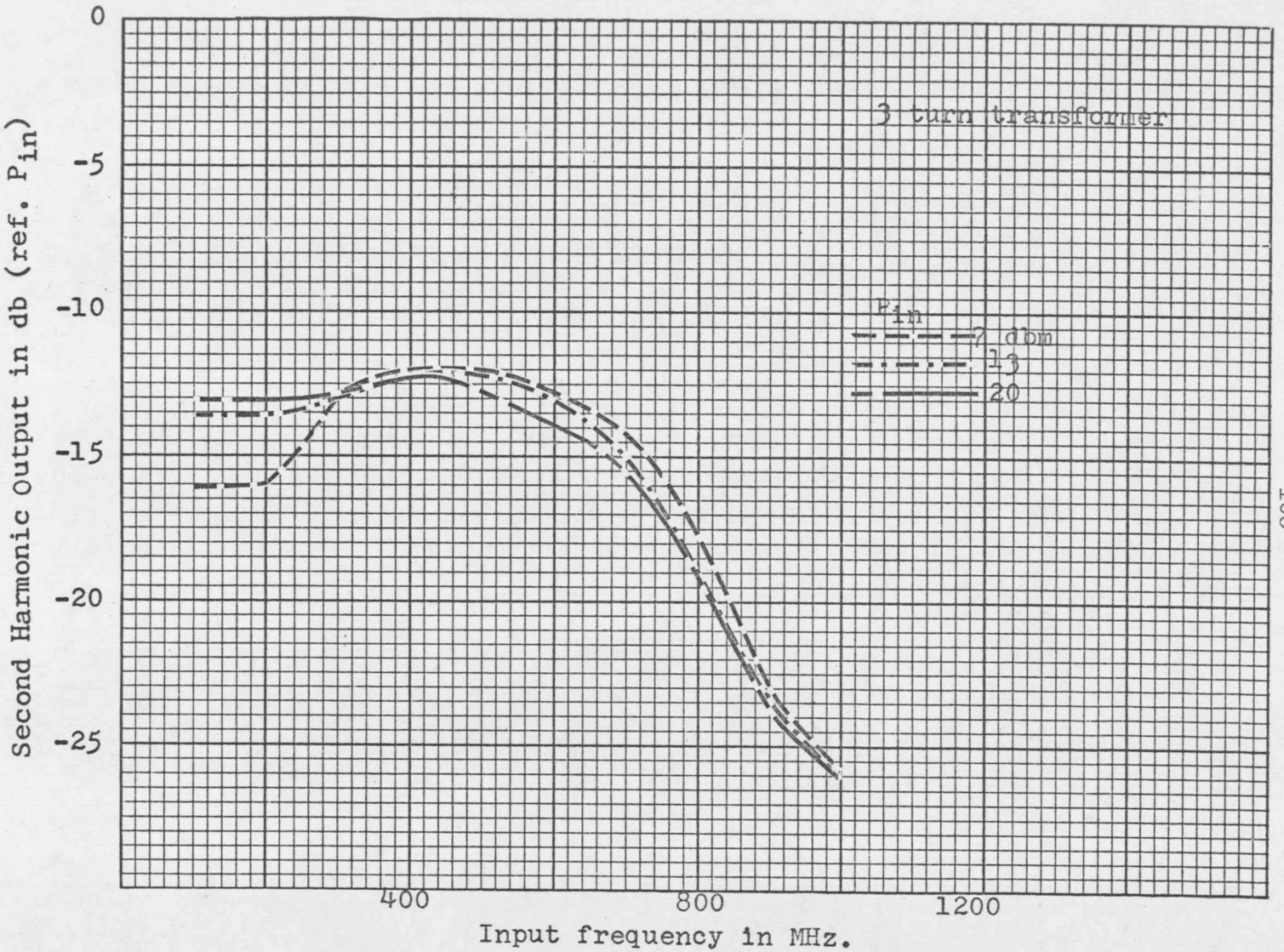


Fig. 5-6. FULL WAVE HARMONIC GENERATOR OUTPUT.

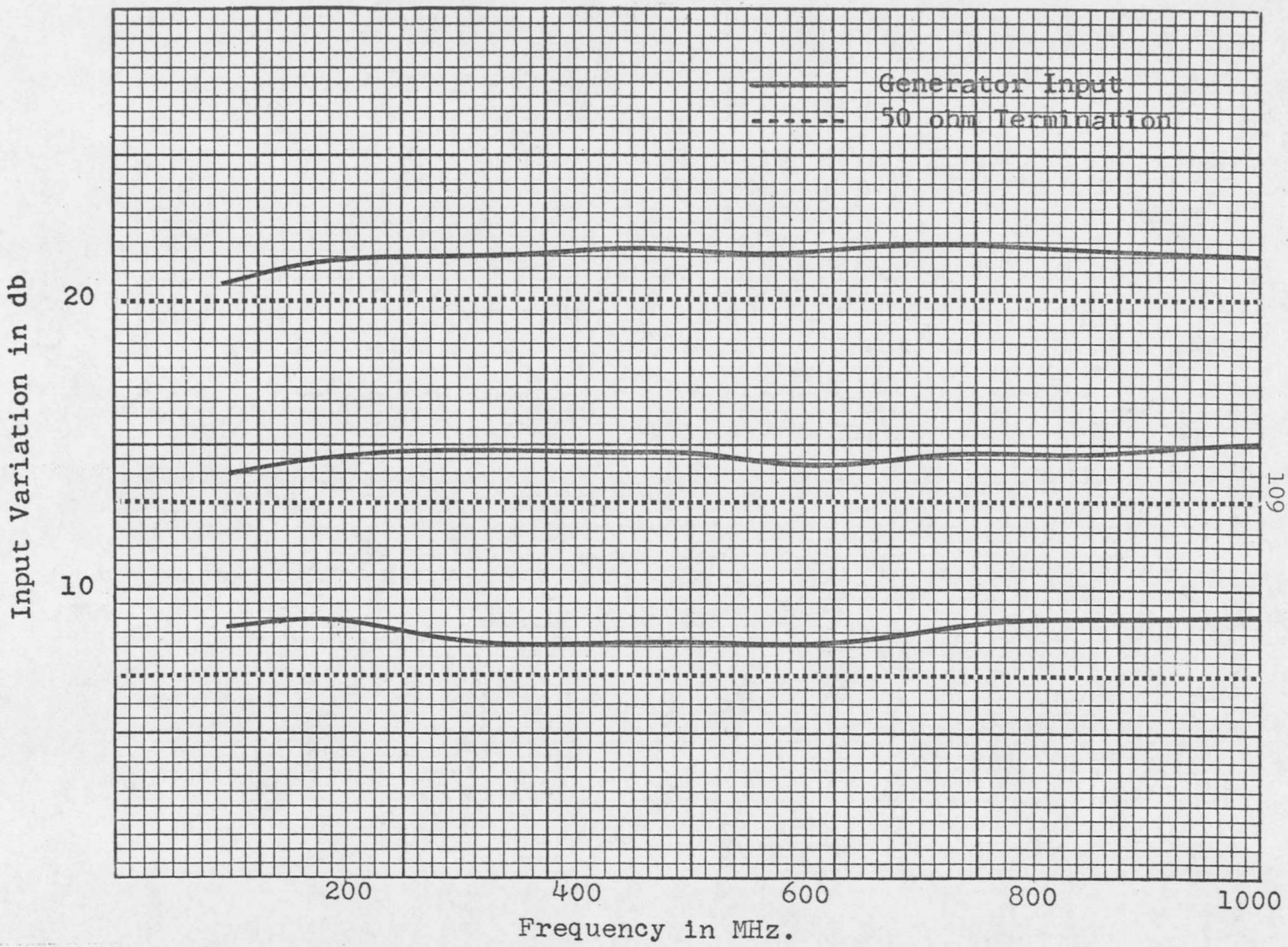


Fig. 5-7 INPUT LEVEL VARIATION - FULL WAVE GENERATOR.

5.1.2 BROADBAND SRD GENERATORS.

The various curves in the analysis of the broadband Step Receiving Diode (SRD) generator of Section 4.2.3 were obtained by assuming that the diode discontinuity was instantaneous. This is not the case with practical diodes. The actual transition time associated with each diode used is given in Table 5-1, and this finite transition time will result in an attenuation of the harmonic content. Using a single-pole approximation to account for a 10 to 90 per cent transition time t_t, the harmonic frequency at which a 6 db degradation will occur is $f = 0.35/t_t$ and will continue at approximately 6 db for each octave as higher harmonics are considered. The correction curves of Fig. 5-8 were generated to account for this degradation of the expected output harmonic spectra. A set of curves for multiplier input frequencies of 100, 200, 300, and 400 MHz are presented for the diode transition time of 2.0, 1.0, 0.5, and 0.3 ns.

The variation of the minority carrier lifetime (τ) due to temperature can be offset by the choice of the diode to be employed. If the $\omega\tau$ product is maintained at 10 or greater the effect of the lifetime variation can be minimized (see Fig. 4-25).

Several broad-band SRD harmonic generators were constructed as shown in Fig. 5-9. The transformer used was of the type previously discussed and had 4-turn windings. The harmonic spectrum obtained

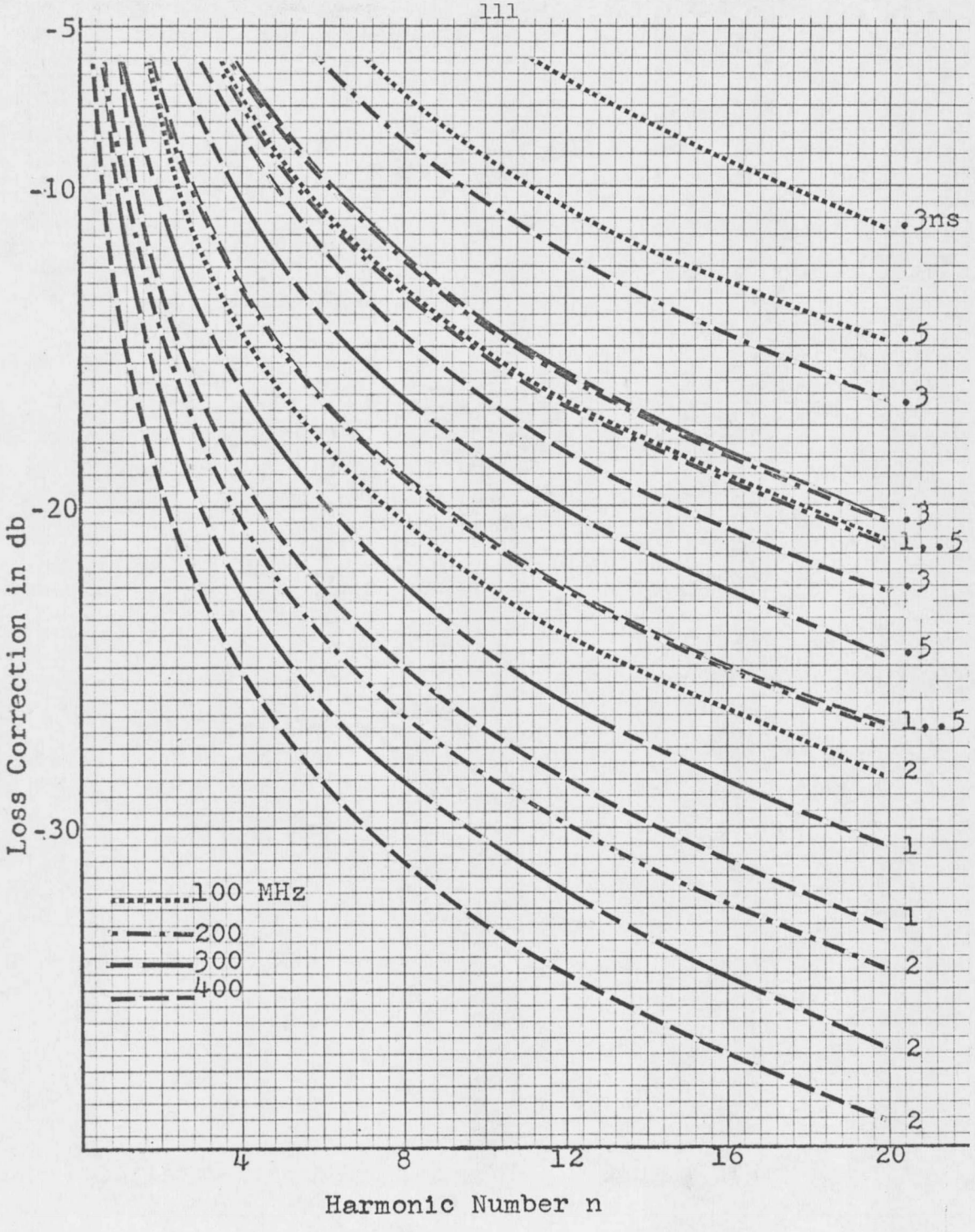


Fig. 5-8. CORRECTION CURVES FOR SRD MULTIPLIERS.

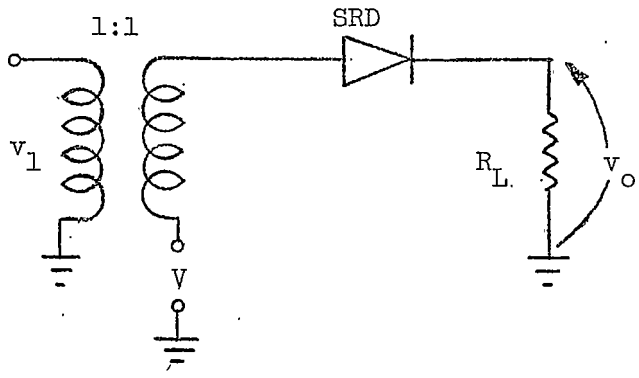


Fig. 5-9. BROADBAND SRD GENERATOR CIRCUIT.

from the experimental multipliers are presented in Fig. 5-10 through Fig. 5-14 for five different diodes. The various multipliers were driven at a nominal power level of +10 dbm. Measurements were obtained by a test circuit connected as shown in Fig. 5-2.

Considering finite diode transition time and transformer losses yields reasonable agreement between the various harmonic specturms obtained and the theoretical spectra of Section 4.2.3.

The diode conduction interval, ϕ, of the multiplier varied from approximately 220° for the hp 0112 and hp 0151 diodes to 260° for the hp 0102 and hp 0103 diodes. This conduction interval measurement was obtained from a sampling oscilloscope waveform.

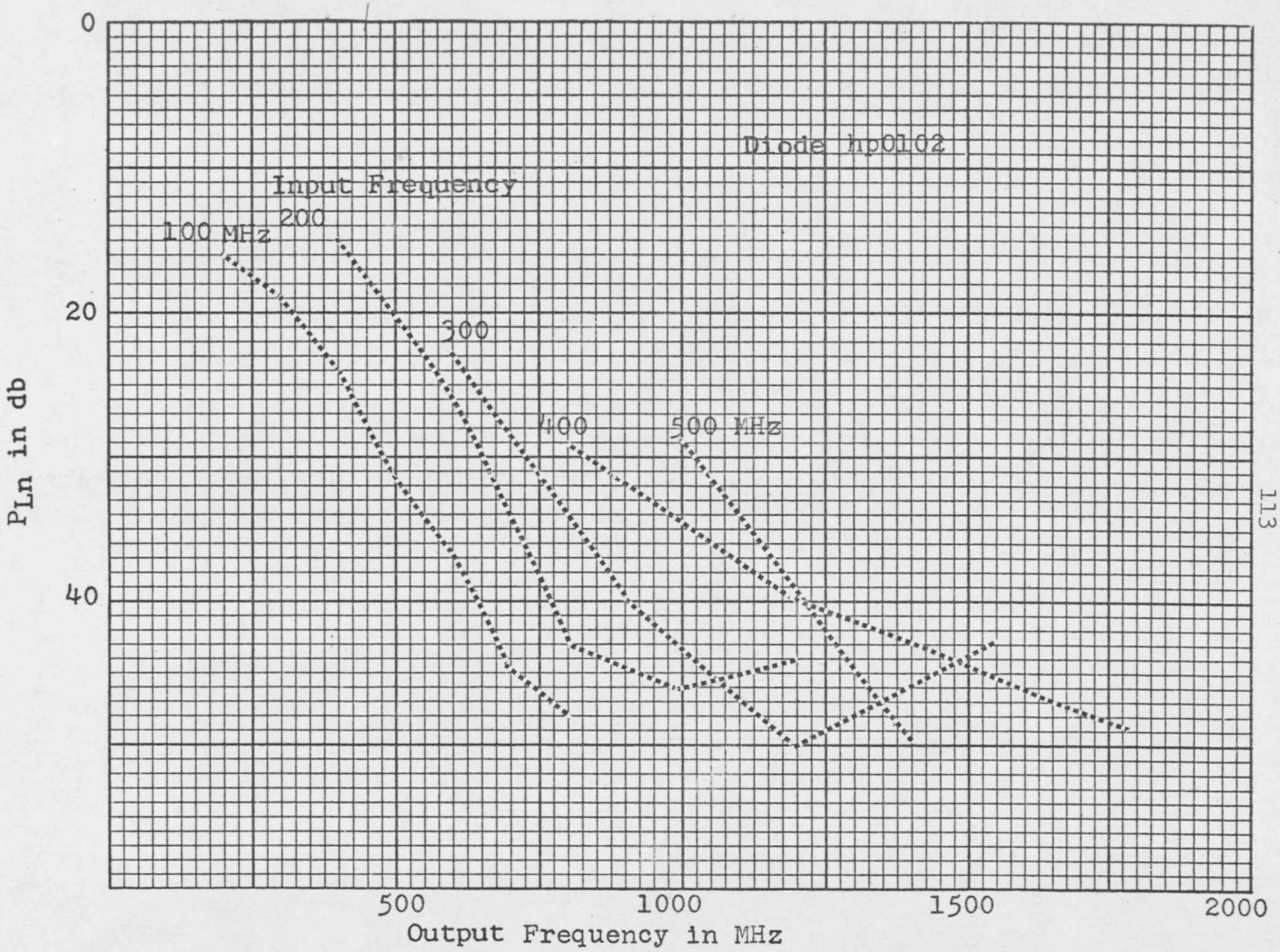


Fig. 5-10. BROADBAND SRD GENERATOR OUTPUT.

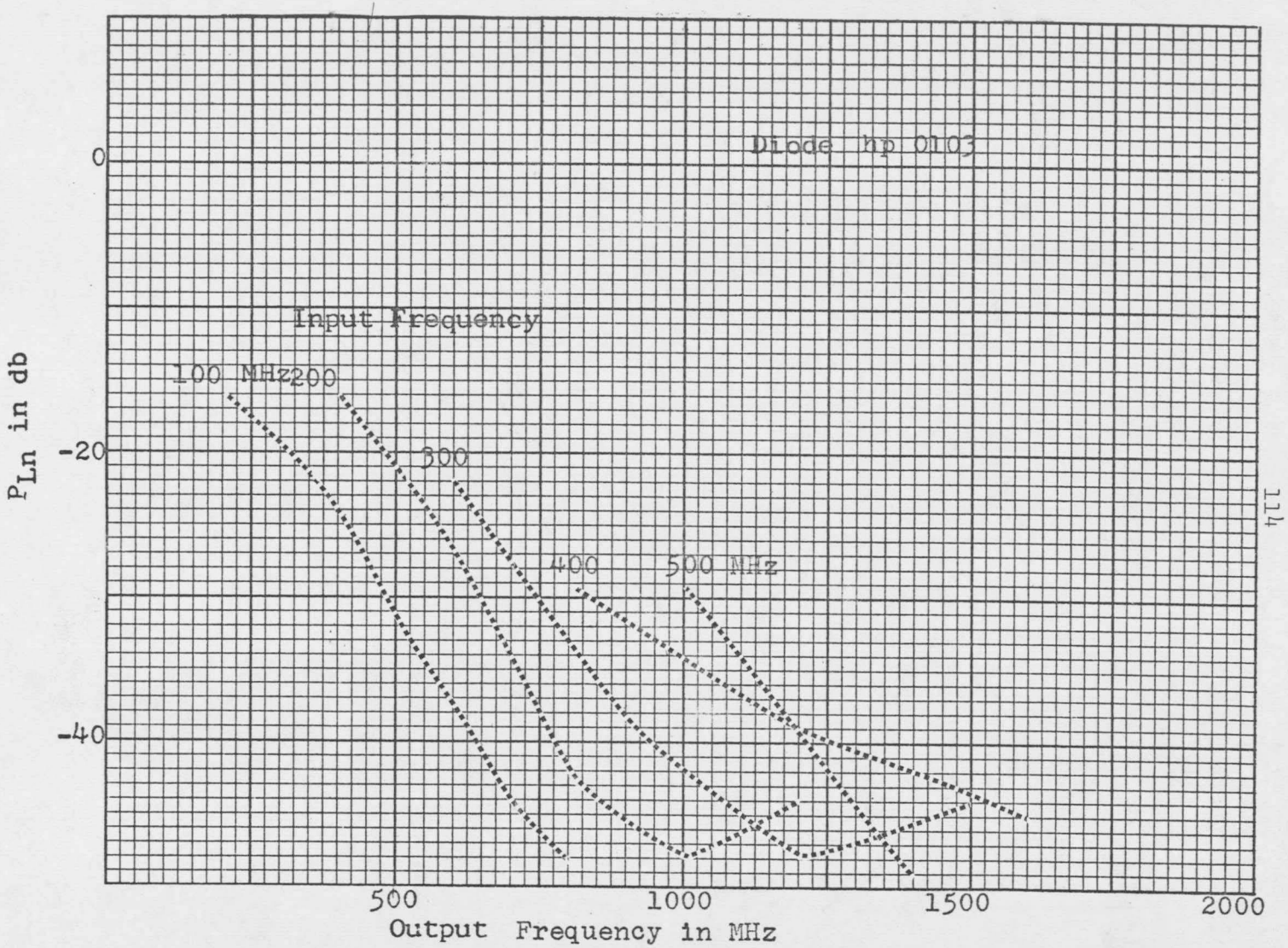


Fig. 5-11. BROADBAND SRD GENERATOR OUTPUT.

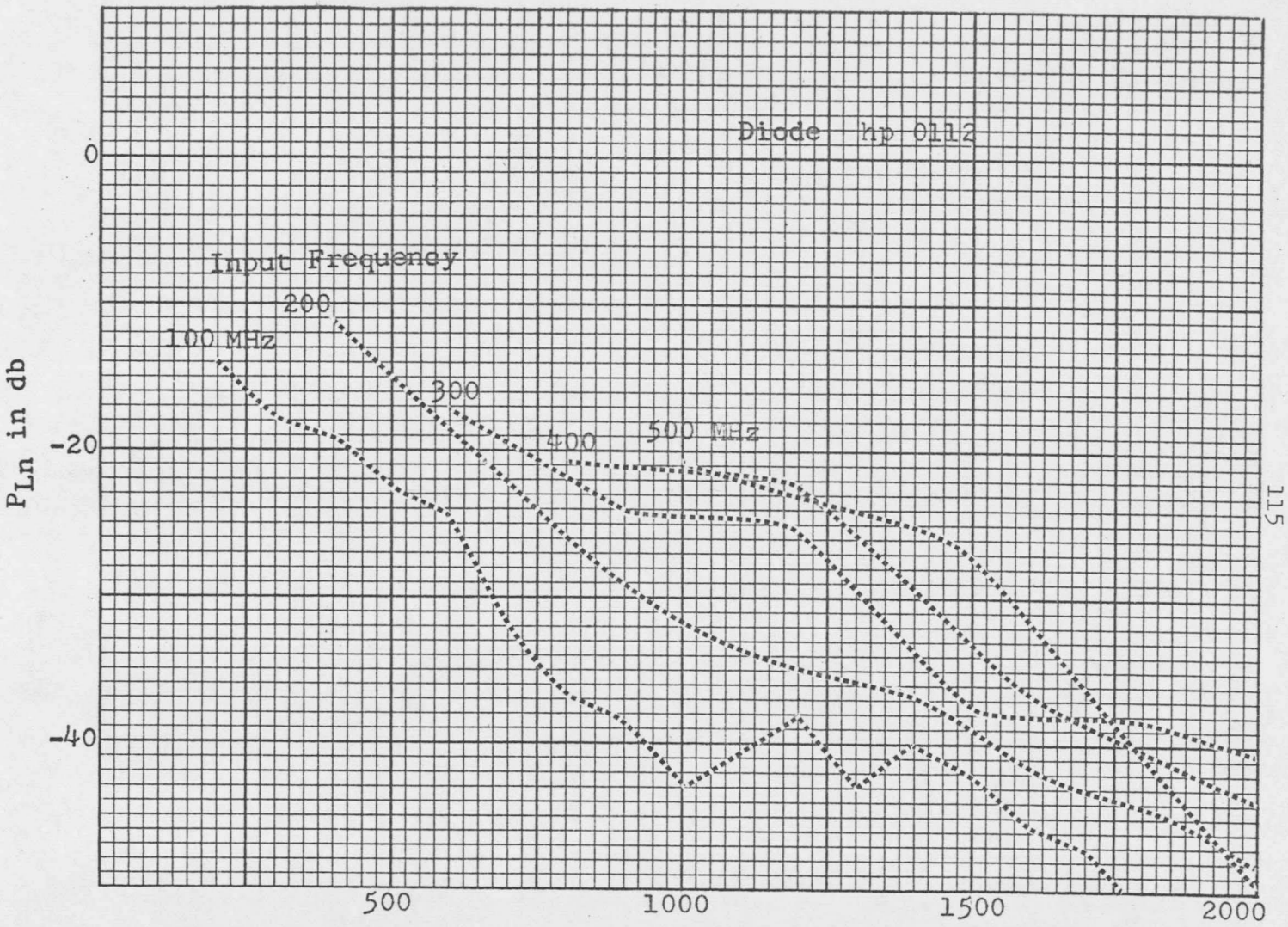


Fig. 5-12. BROADBAND SRD GENERATOR OUTPUT.

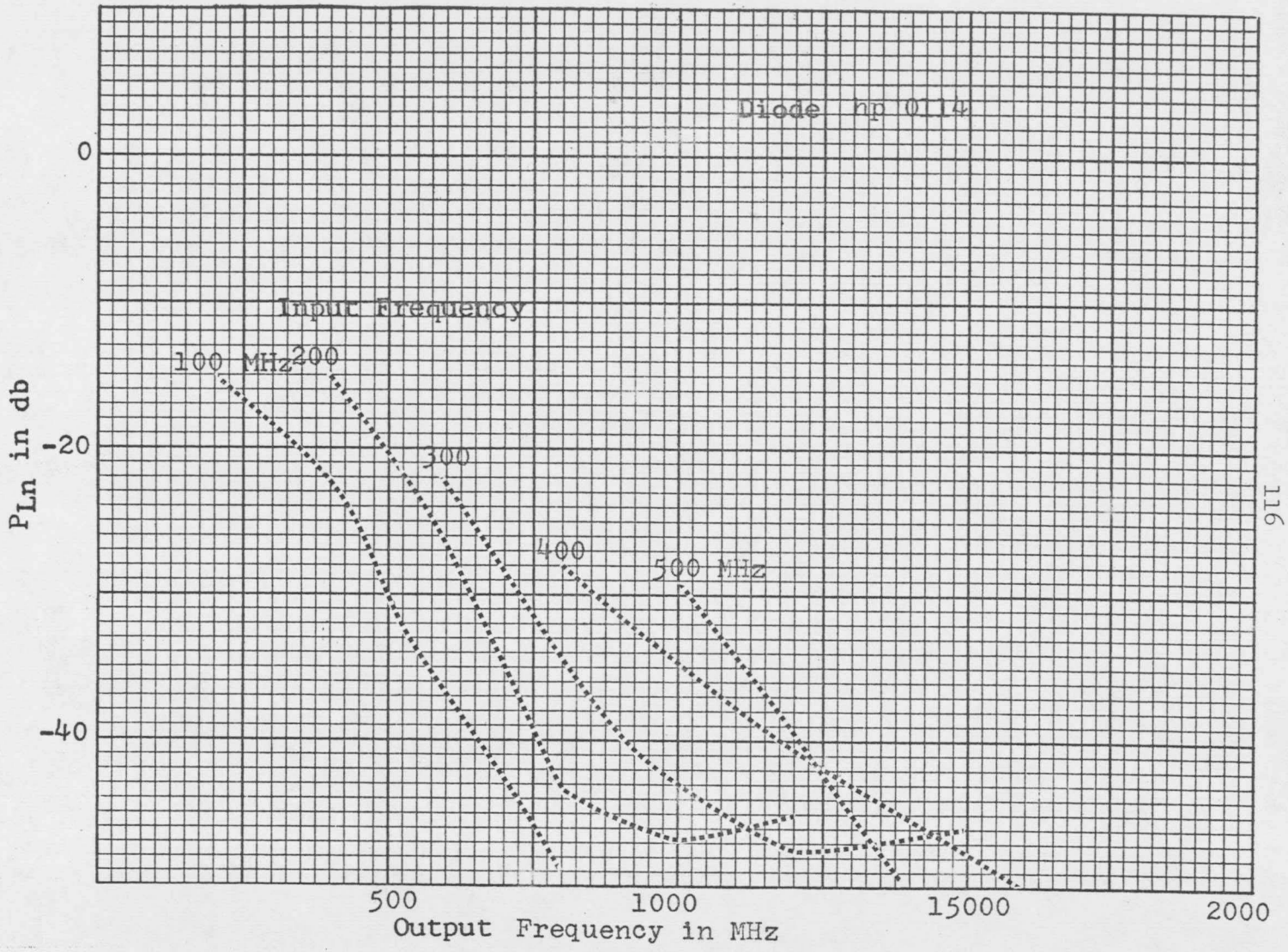


Fig. 5-13. BROADBAND SRD GENERATOR OUTPUT.

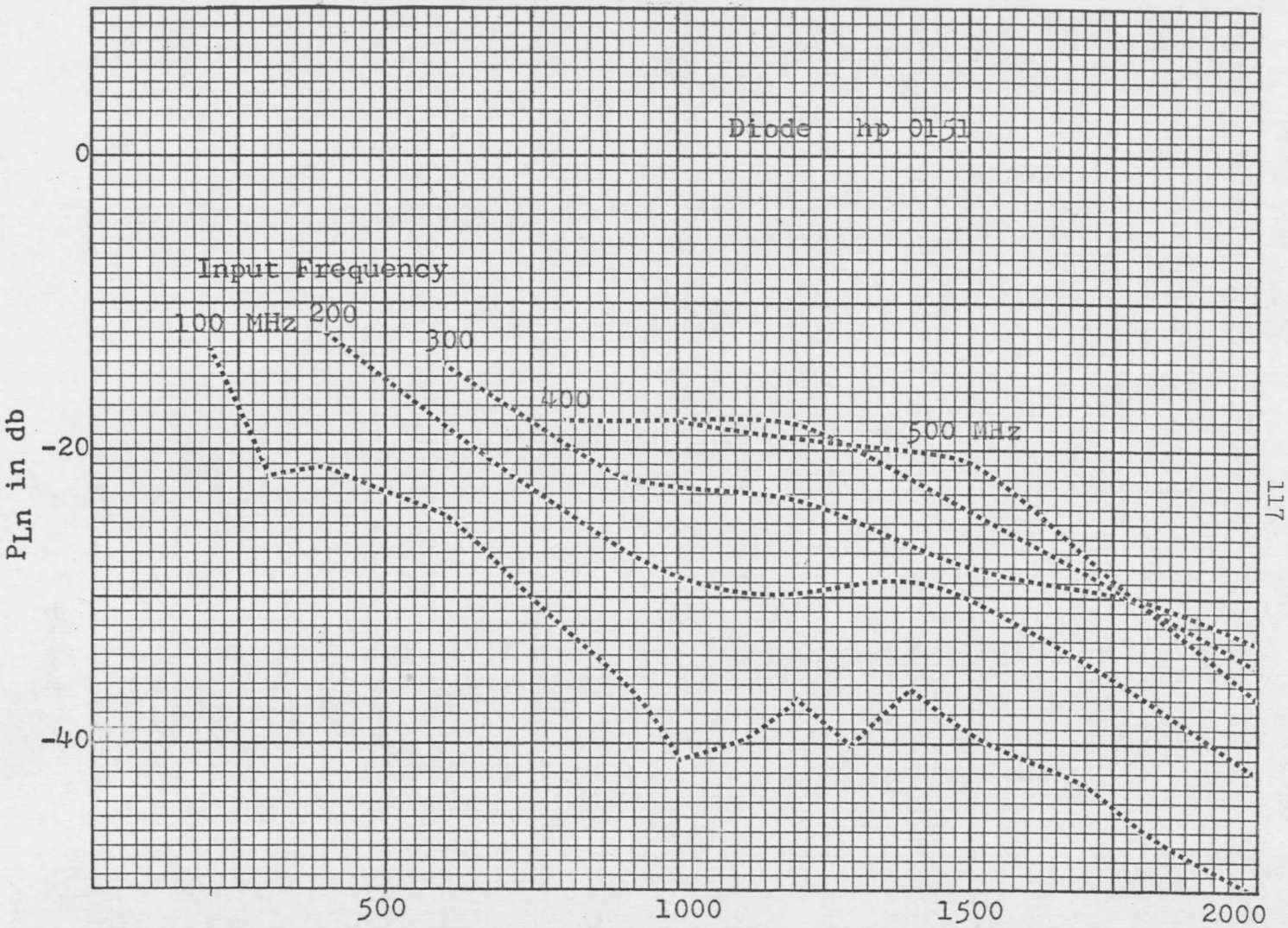


Fig. 5-14. BROADBAND SRD GENERATOR OUTPUT.

The input impedance of the multipliers tested varied approximately 2:1 over the input frequency range of 100 to 500 MHz.

The external vias voltage, V, was at zero volts for the data presented. This voltage was adjusted to optimize various harmonics as the multipliers were in operation. The variation of harmonic amplitudes was consistent with the expected variation presented in 4.2.3 as the bias voltage V was varied causing the conduction interval, ϕ, to change considerably.

The various multipliers constructed were operated over a -10° to 50°C temperature range with no apparent degradation in performance. The external bias voltage was held at zero volts for the temperature tests.

5.1.3 SRD RESONANT LOAD HARMONIC GENERATORS.

Several SRD resonant-load harmonic generators were constructed with transformer coupling as shown in Fig. 5-15. The input transformer used was of the type previously discussed and had 10-turn windings.

The harmonic spectrum obtained from several experimental multipliers are presented in Fig. 5-16. The fourth order spectrum of Fig. 5-16(A) was obtained from a multiplier constructed for 200 MHz output using a hp 0102 diode. The multiplier was operated with the bias voltage V at zero volts and the output coupling link

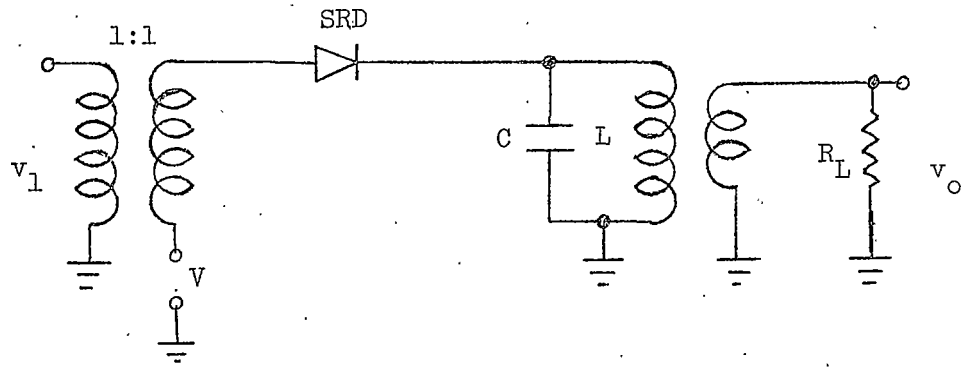


Fig. 5-15. RESONANT LOAD SRD HARMONIC GENERATOR CIRCUIT.

terminated in 50 ohms. The circuit values for this multiplier are as follows:

$L = .04$ μh

$C = 16$ pf

$Q_2/n = 5$

$Q_1 = .25$ (for $R_g = 50$ ohms)

Fifth and sixth order multiplier operation produced spectra containing the desired harmonic at -20 db (reference - P_{in} = 20 dbm) and all other components at -40 db or lower.

Fig. 5-16(B) shows the spectrum obtained from a multiplier using a hp 0103 diode and the following circuit values:

$L = .08$ μh

$C = 32$ pf

$Q_2/n = 1.75$

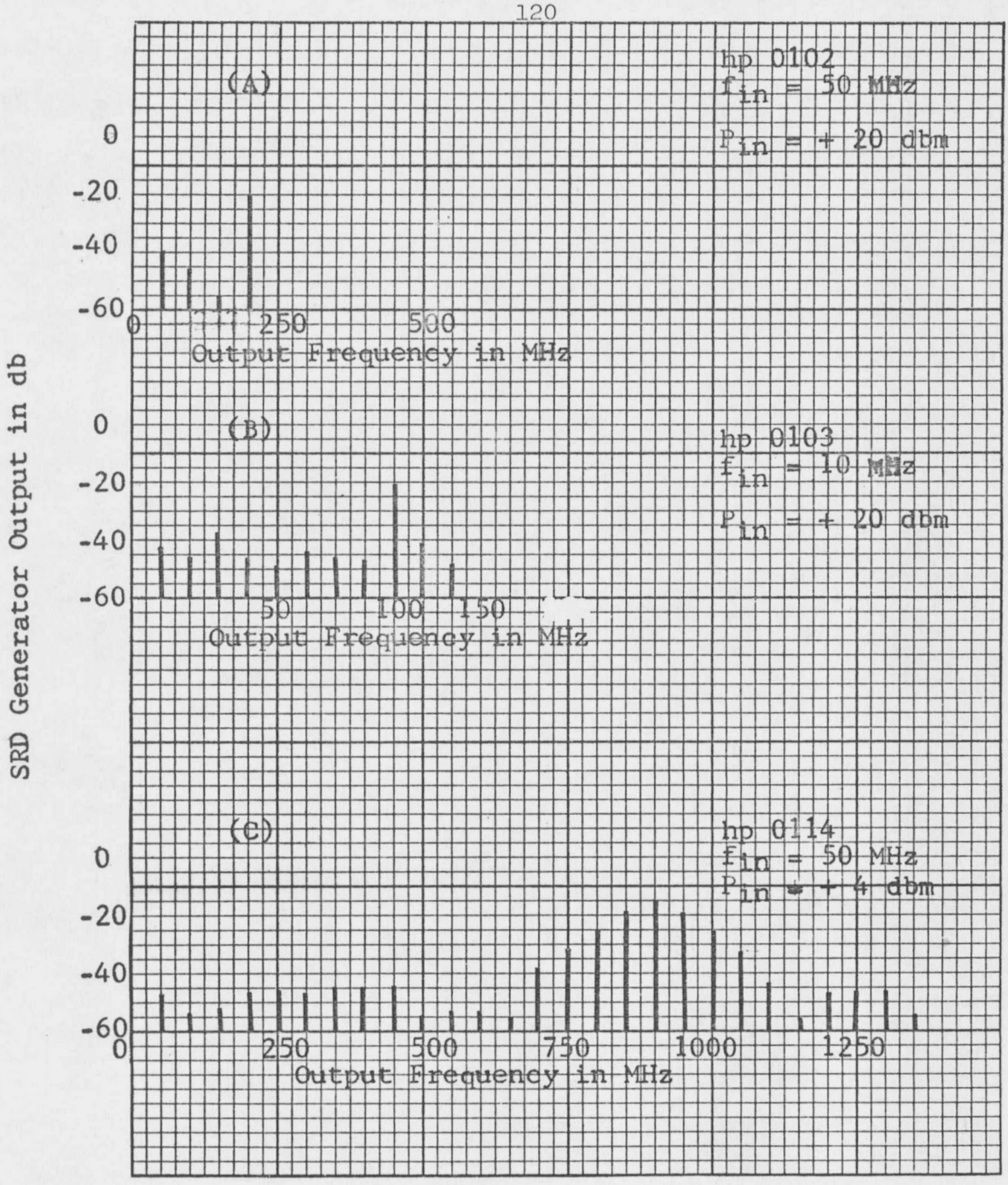


Fig. 5-16. SRD GENERATOR OUTPUT WITH TRANSFORMER INPUT AND RESONANT LOAD.

$Q_1 = .1$

The 9th order output was -20 db with undesired components -40 db or lower. Circuit adjustments were made for operation through the 17th order. Desired outputs of approximately -20 db and undesired outputs of -40 db or lower were obtained.

Another multiplier was constructed using a hp 0114 diode and a tunable cavity as the output circuit. For a 50 MHz input signal the multiplier could be adjusted for operation at the 15th through 20th harmonic. The spectrum shown in Fig. 5-16(C) was obtained with the cavity tuned for the 18th harmonic. This spectral distribution was typical for the range of operation observed. Desired harmonic levels were in the -15 to -20 db range.

The transformer input of the multipliers were replaced with LC impedance matching networks and self biasing circuitry. Typical output spectra obtained with the tuned inputs are shown in Fig. 5-17. The conversion loss obtained for harmonics of $n > 9$ was typically -n db.

Multiplier circuits were operated over the -10° to 50°C temperature range with no apparent degradation of the output harmonic energy.

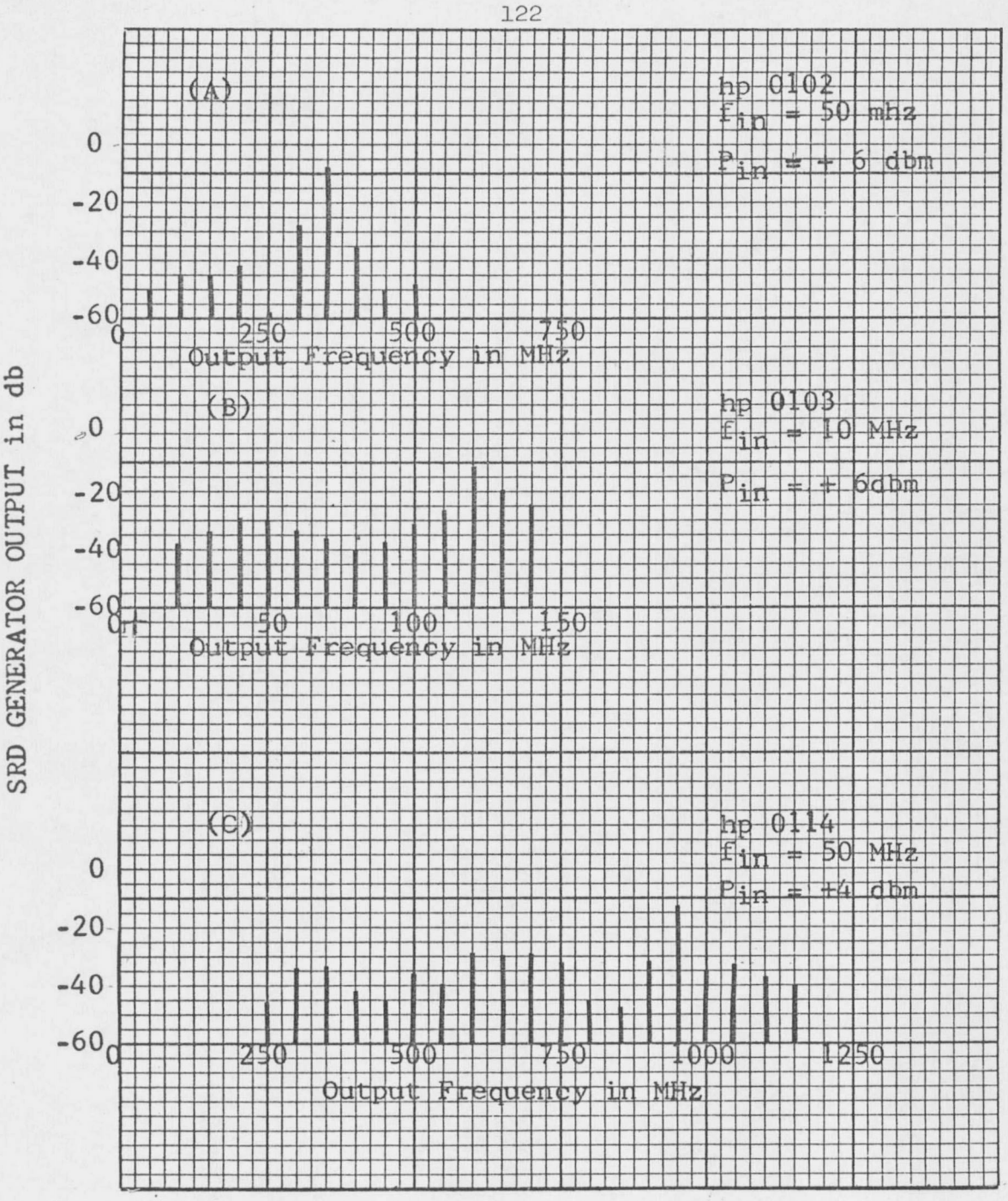


Fig. 5-17. SRD GENERATOR OUTPUT WITH TUNED INPUT AND RESONANT LOAD.

5.2 DIVISION.

In this section the experimental work that was performed with the frequency divider discussed in Section 4.3.1 is presented. Frequency dividers were designed for subharmonic operation of order 1/2 through the 100 MHz to 1 GHz frequency range with component placement as given in Fig. 4-36. The frequency ranges used in the experimentation are 100-200 MHz, 200-400 MHz, 350-700 MHz, and 500-1000 MHz. The values for the inductors L and the capacitor C were calculated using equation (4-10) for $R_g = R_L = 50$ ohms and are tabulated in Table 5-2.

Table 5-2

L AND C VALUES FOR FREQUENCY DIVIDERS

ω_o (MHz)	L(μh)	C(pf)
200	.056	22.6
400	.028	11.3
600	.02	8.0
700	.016	6.45
1000	.011	4.5

The experimental test circuit used for measurement of the divider operation is that of Fig. 5-2 with the divider as the unit under test.

Fig. 5-18 through 5-25 show the operational data obtained from the above design values and the four different step recovery diodes used. Fig. 5-18 and 5-19 present the required power level for the execution of the subharmonic oscillation of order 1/2 and the effect of input impedance variation respectively for the 100-200 MHz divider. The power levels for which the divider will execute a subharmonic oscillation consists of the area between the two threshold curves shown for each diode. Fig. 5-20 and 5-21 present the operational data for 200-400 MHz divider. The 350-700 MHz divider operation data is presented in Fig. 5-22 and 5-23, and the 500-1000 MHz divider data is shown in Fig. 5-24 and 5-25.

The effect of the diode parameters can be readily seen in Figures 5-18 and 5-20. In each case as a different diode was used the value of the input capacitor C was adjusted slightly to obtain as wide an operational frequency bandwidth as possible.

Proper divider action over the desired range of the 350-700 MHz and 500-1000 MHz dividers could be obtained with only the hp 0151 diode. The parameters of the hp 0112 are starting to have their effect on the divider operation as can be seen in Fig. 5-20.

The operational power level data obtained for the various experimental dividers, presented in Fig. 5-18, 20, 22, 24, all present the general shape predicted by Fig. 4-45. The data presented in Fig. 4-45 was calculated for a 500-1000 MHz divider circuit.

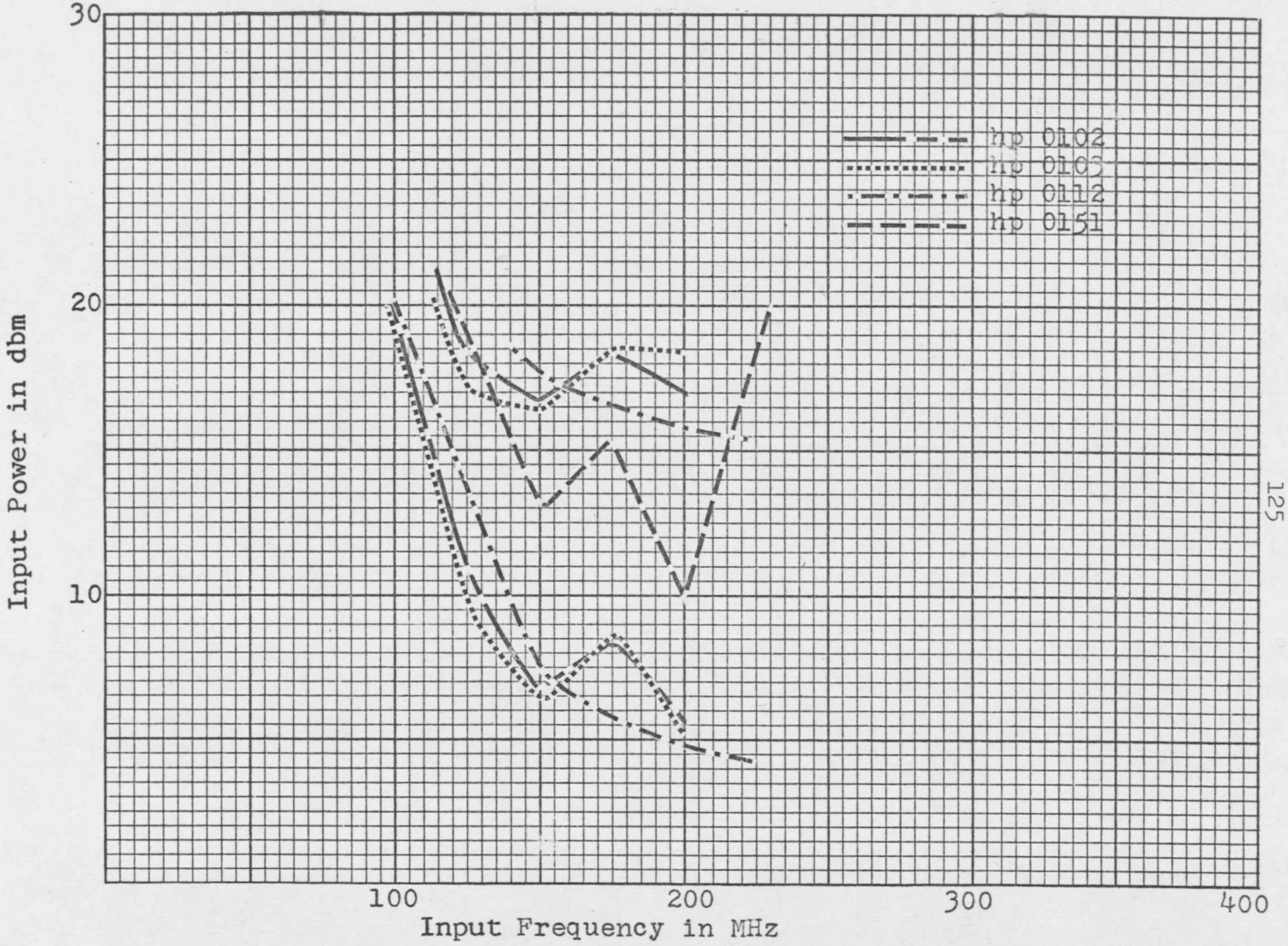


Fig. 5-18. DRIVE LEVEL 100-200 MHz DIVIDER.

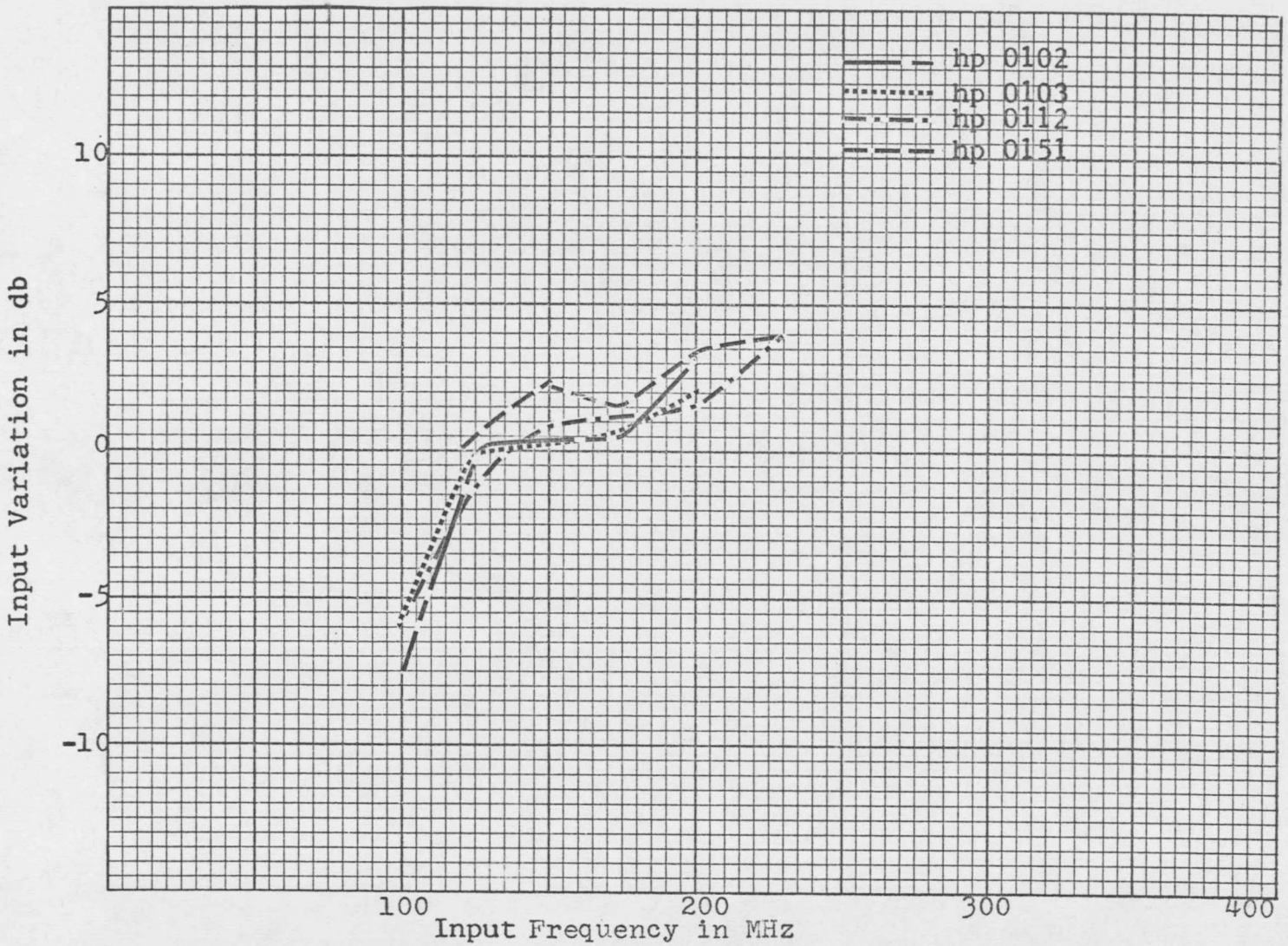


Fig. 5-19. EFFECT OF IMPEDANCE VARIATION 100-200 MHz DIVIDER.

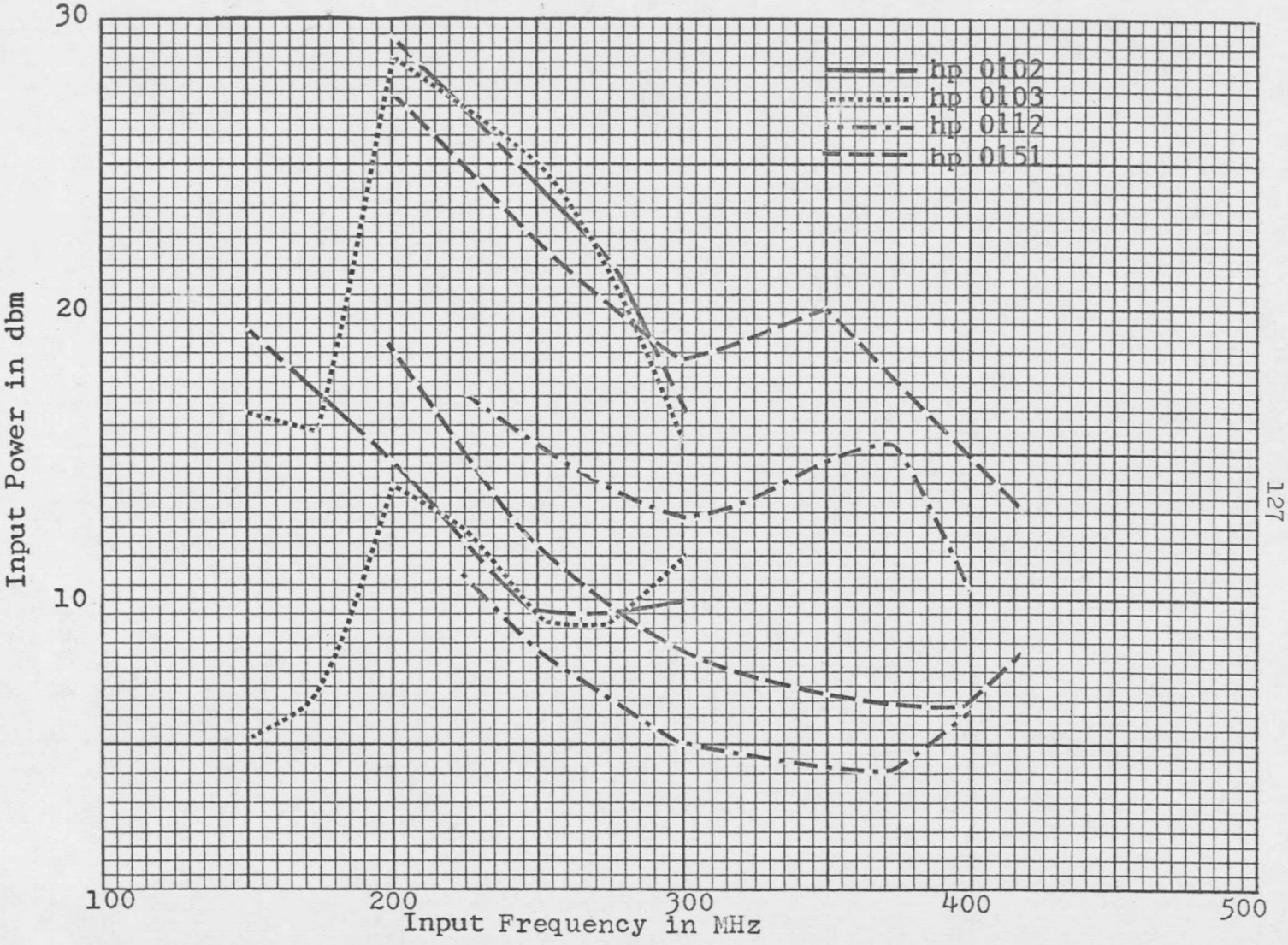


Fig. 5-20. DRIVE LEVEL 200-400 MHz DIVIDER.

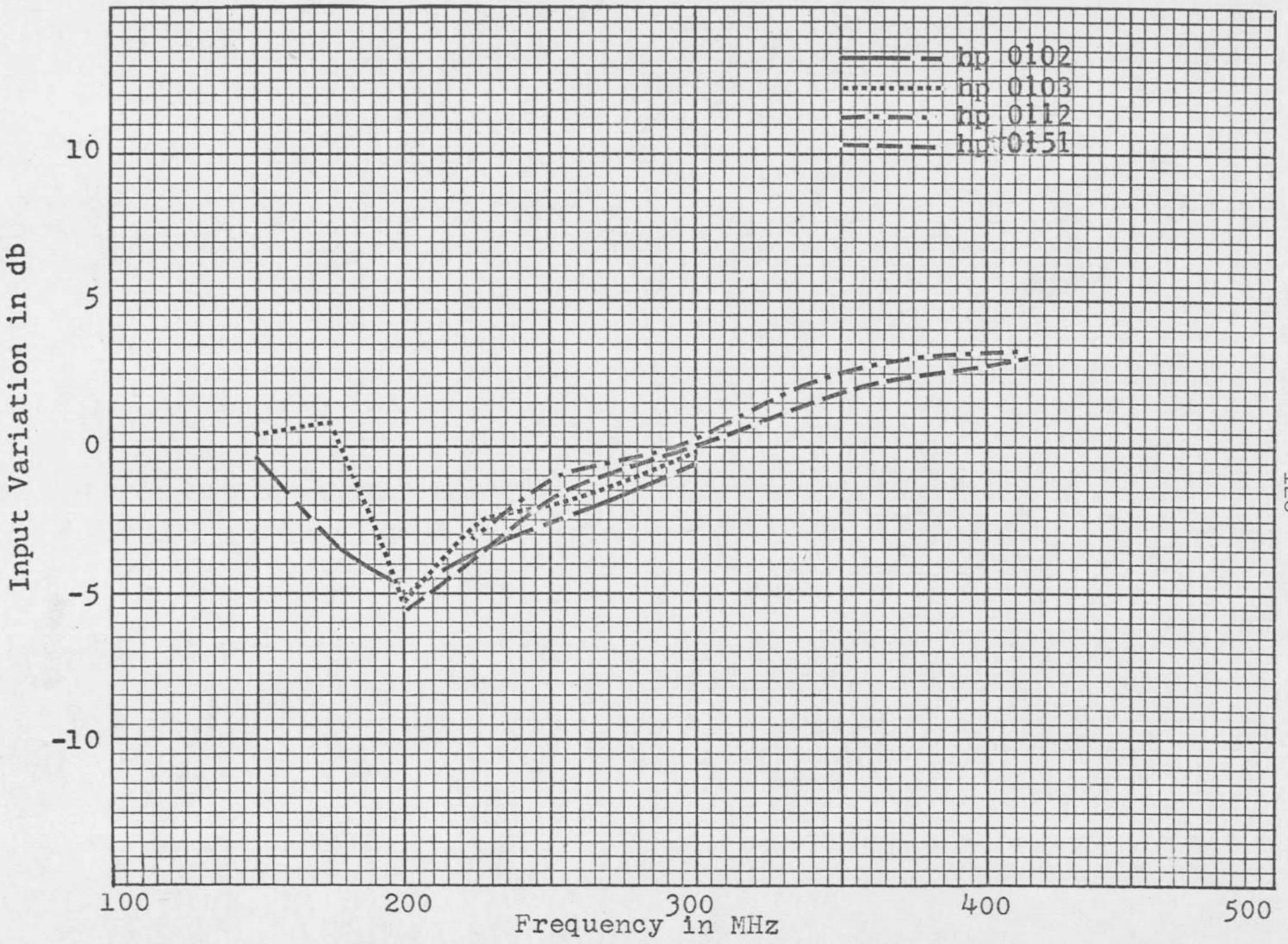


Fig. 5-21. EFFECT OF IMPEDANCE VARIATION 200-400 MHz DIVIDER.

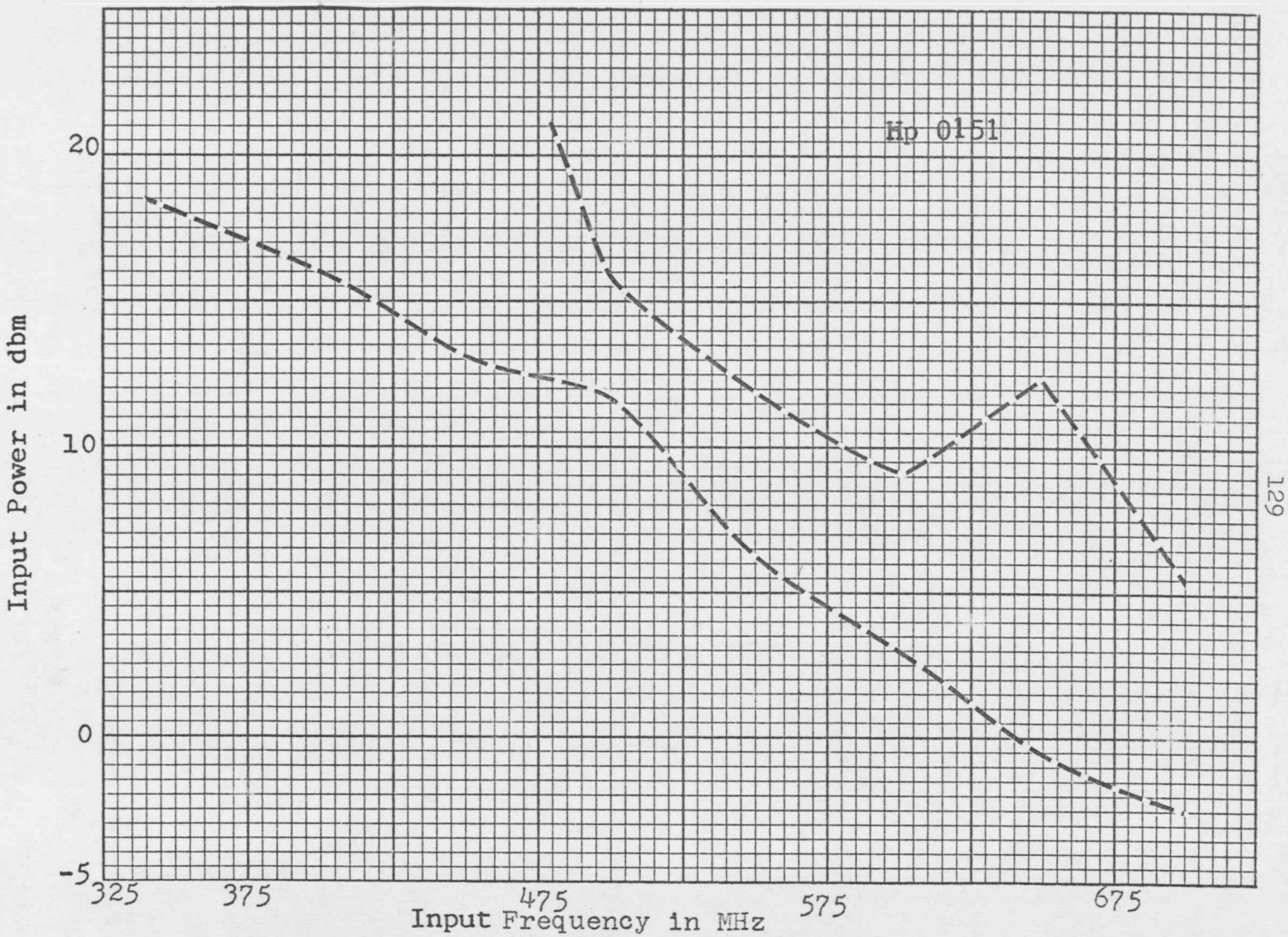


Fig. 5-22. DRIVE LEVEL 350-700 MHz DIVIDER.

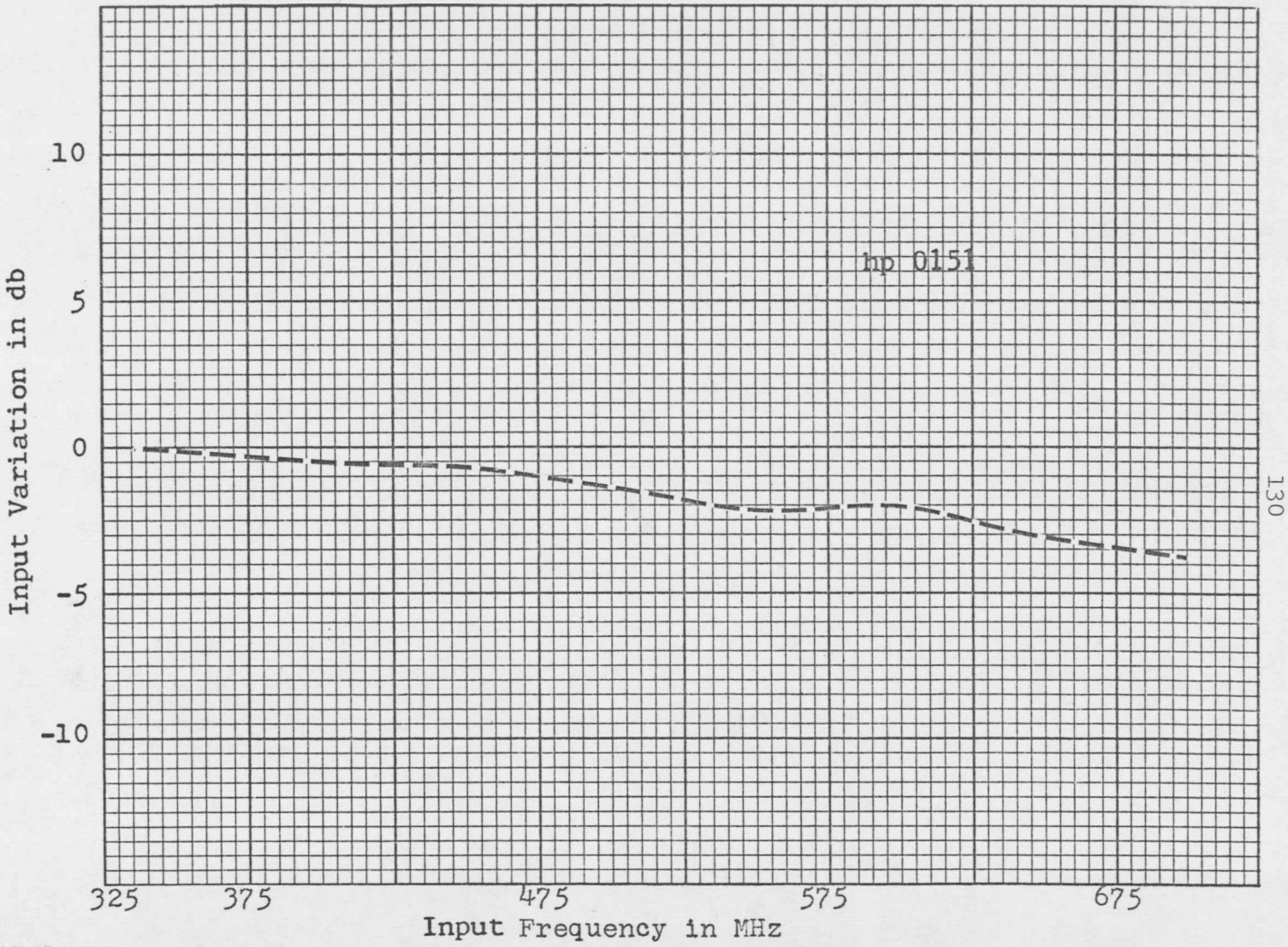


Fig. 5-23. EFFECT OF IMPEDANCE VARIATION 350-700 MHz DIVIDER.

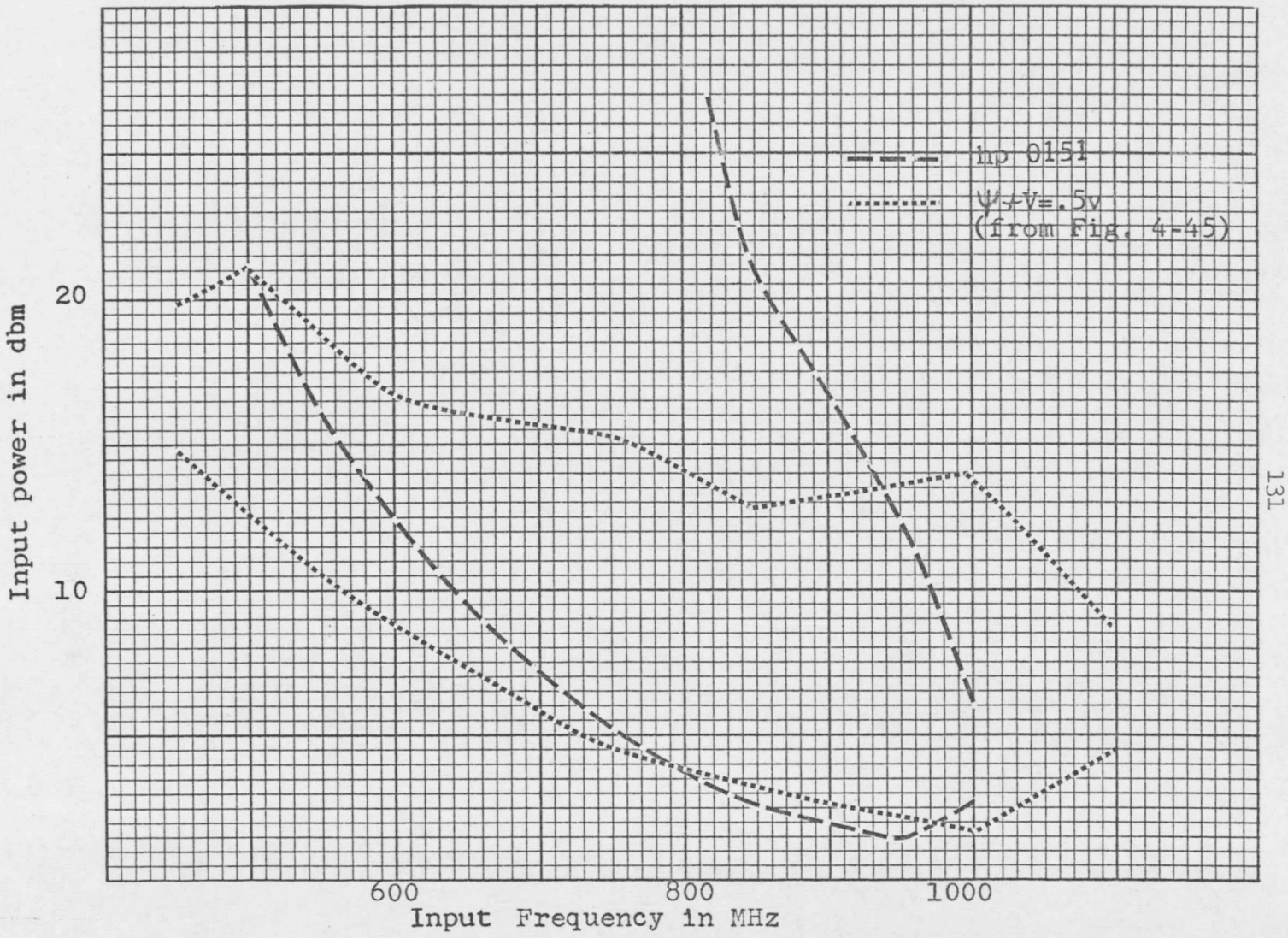


Fig. 5-24. DRIVE LEVEL 500-1000 MHz DIVIDER.

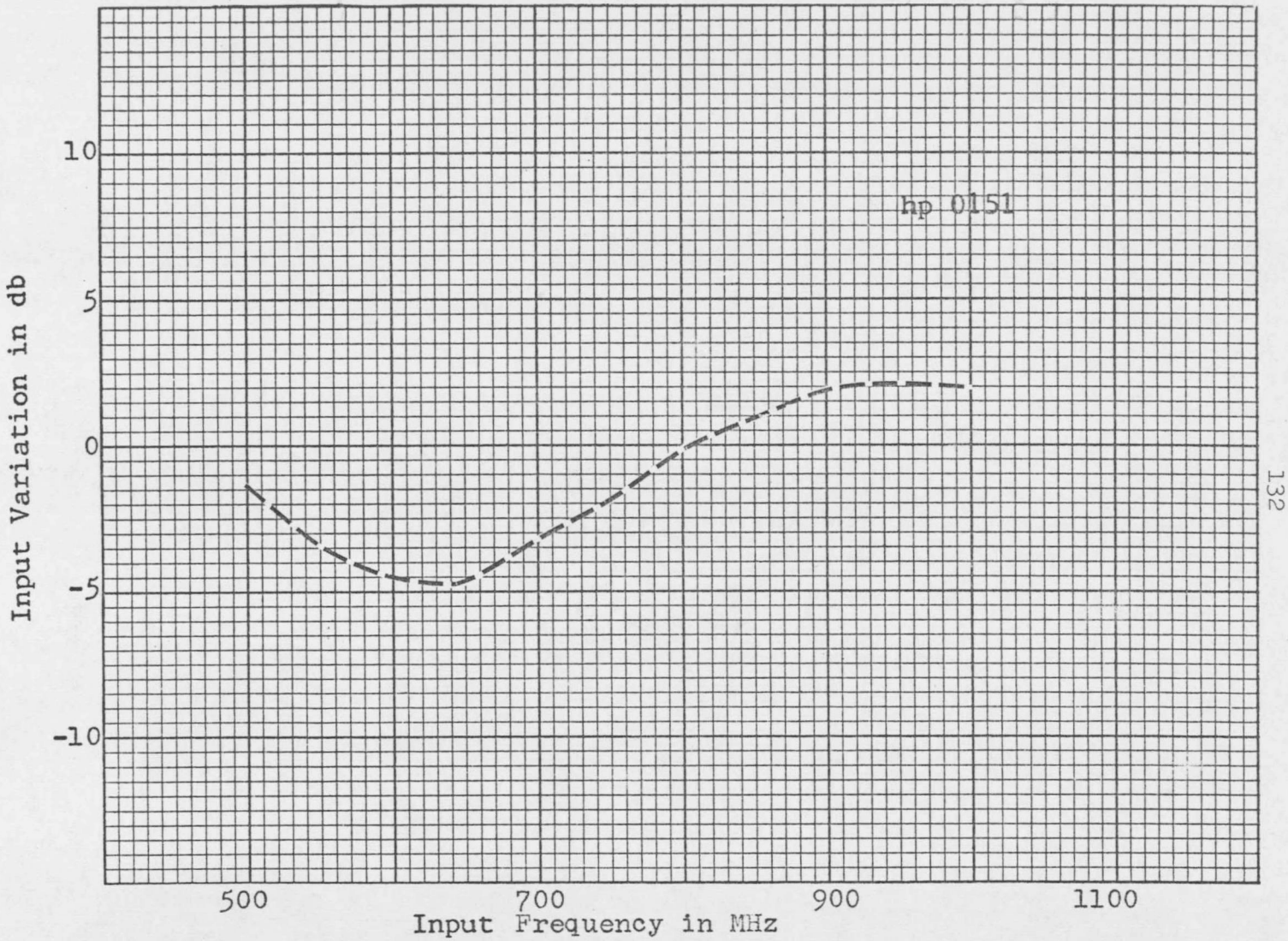


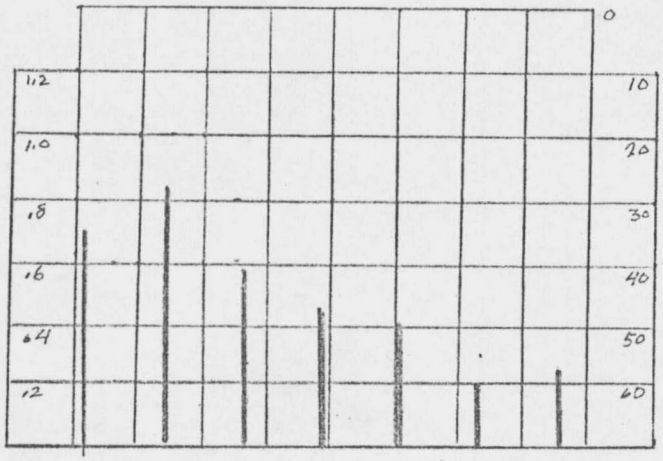
Fig. 5-25. EFFECT OF IMPEDANCE VARIATION 500-1000 MHz DIVIDER.

Power curves of Fig. 5-24 were obtained from an experimental divider designed for this operational frequency range and comparison of these data sets indicates reasonable agreement between the theoretical and experimental data. The junction potential, ψ_o, of the hp 0151 diode used is approximately 0.7 v.

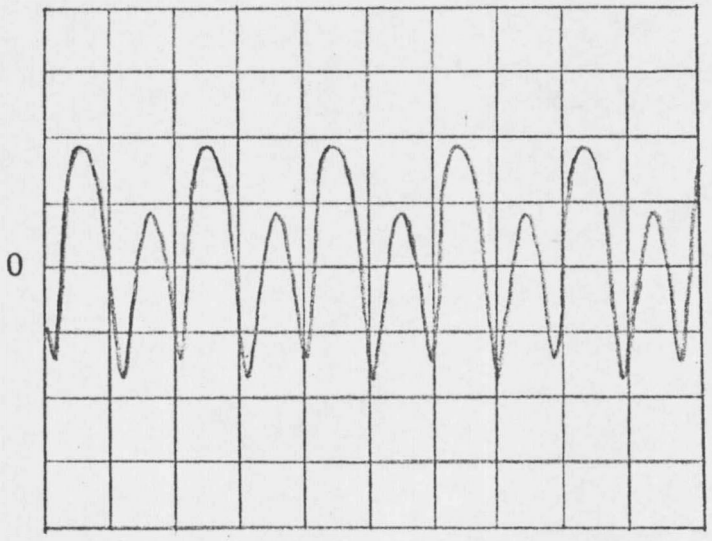
In the construction of the individual divider circuits, high Q air coils and good quality variable capacitors were used along with layout minimizing lead lengths and proximity effects.

From Fig. 5-19, 21, 23, 25 the input impedance variation can be determined for the individual dividers under circuit operation. The curves present the deviation in db as recorded from the voltmeter (see Fig. 5-2) between the voltage level across 50 ohms and the voltage level applied to the divider input terminals.

Several operational output waveforms and 1/2 order harmonic spectrums for the 500-1000 MHz, 200-400 and 100-200 dividers using the 0151 diode are shown in Figures 5-26 through 5-30. These output waveforms are of the general form obtained from the computer analysis presented in Fig. 4-43. The operational waveforms show that, as a function of input power level, the divider may operate with one conducting and one nonconducting interval or two sets of conduction and nonconduction as was predicted from the computer analysis and presented in Fig. 4-39, 41 and 42.

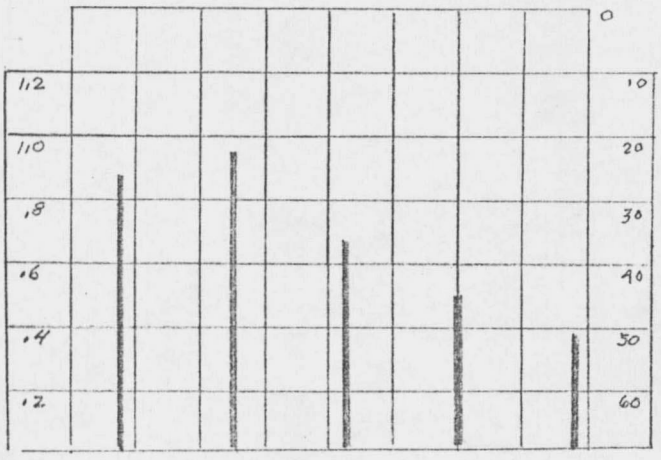


a) Spectrum: 200 MHz/cm; 1.0 = 20dbm

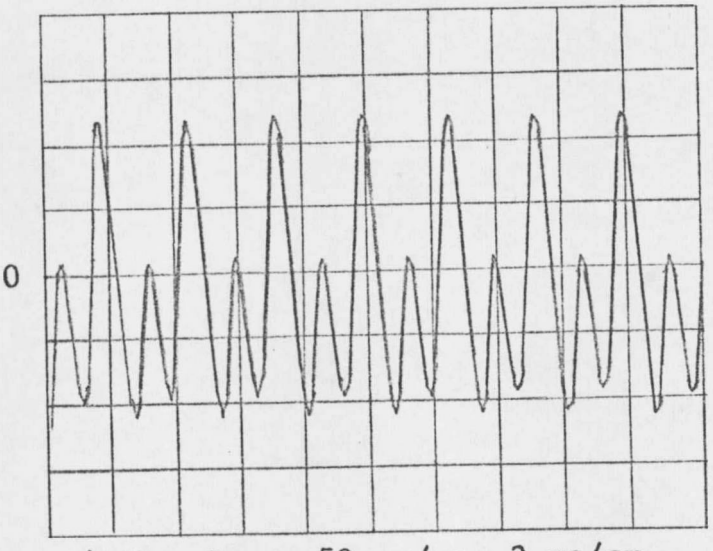


b) Waveform: 100mv/cm; 2 ns/cm

Fig. 5-26. OUTPUT SPECTRUM AND WAVEFORM 500-1000 MHz DIVIDER f_{in} = 520 MHz (P_{in} = 20 dbm).

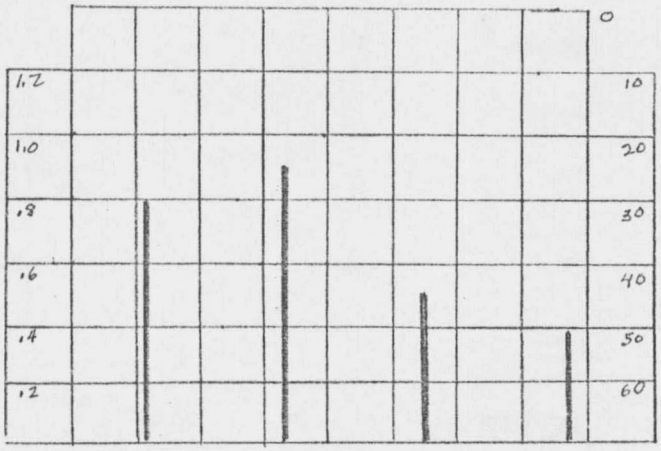


a) Spectrum: 200 MHz/cm; 1.0 = 10 dbm

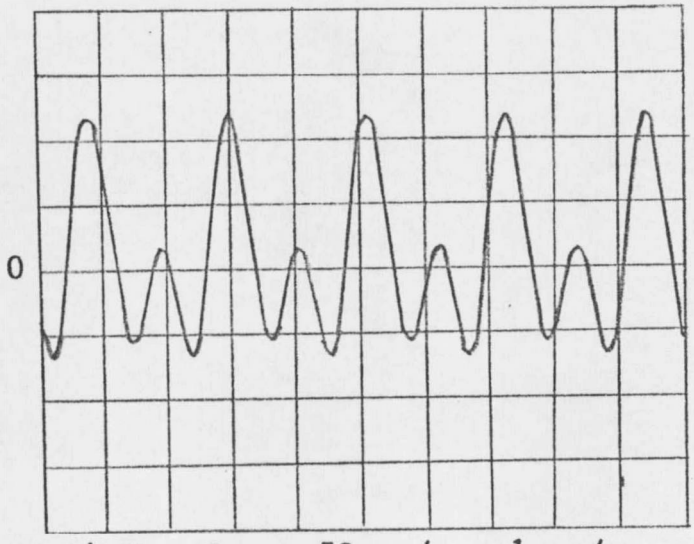


b) Waveform: 50 mv/cm; 2 ns/cm

Fig. 5-27. OUTPUT SPECTRUM AND WAVEFORM 500-1000 MHz DIVIDER f_{in} = 750 MHz (P_{in} = 10 dbm).



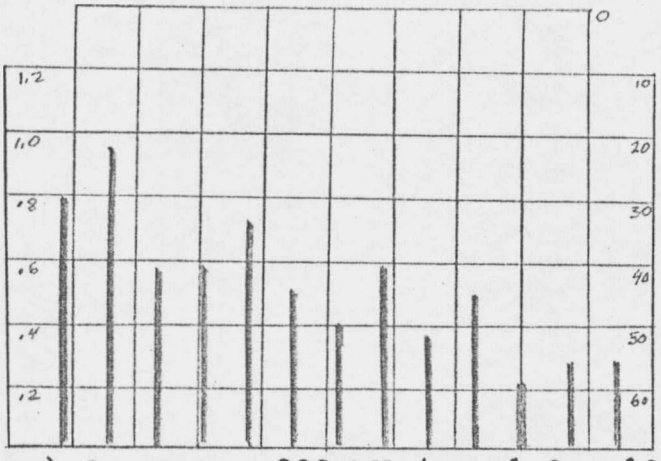
a) Spectrum: 200 MHz/cm; 1.0 = 11 dbm



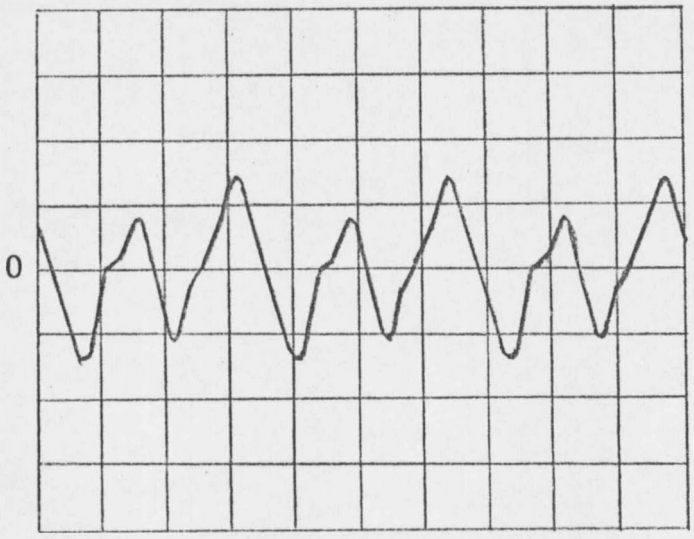
b) Waveform: 50 mv/cm; 1 ns/cm

Fig. 5-28. OUTPUT SPECTRUM AND WAVEFORM

500-1000 MHz DIVIDER f_{in} = 1000 MHz (P_{in} = 11 dbm).



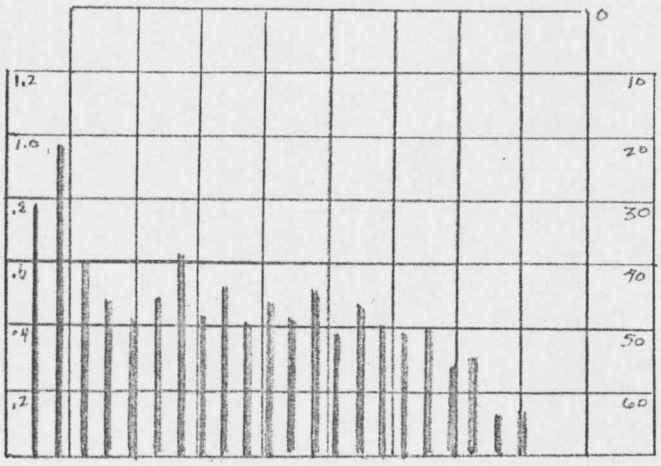
a) Spectrum: 200 MHz/cm; 1.0 = 10 dbm



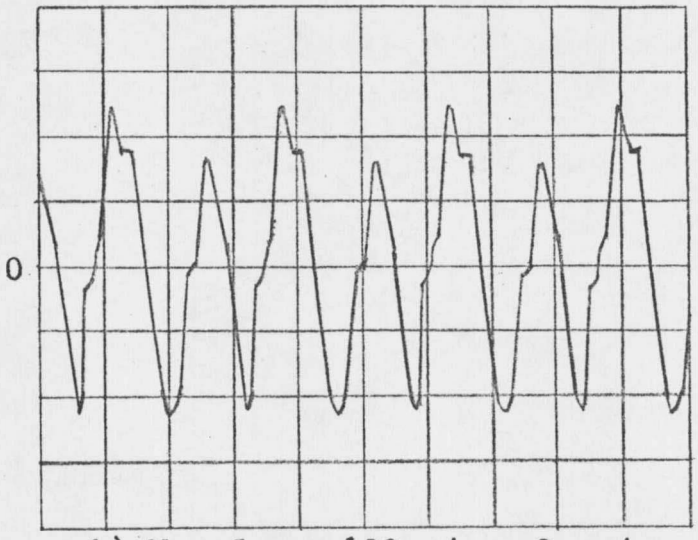
b) Waveform: 100mv/cm; 2 ns/cm

Fig. 5-29. OUTPUT SPECTRUM AND WAVEFORM

200-400 MHz DIVIDER f_{in} = 300 MHz (P_{in} = 10 dbm).



a) Spectrum: 200 MHz/cm; 1.0 = 17 dbm



b) Waveform: 100mv/cm; 2 ns/cm

Fig. 5-30. OUTPUT SPECTRUM AND WAVEFORM

100-200 MHz DIVIDER f_{in} = 150 MHz (P_{in} = 17 dbm).

When the input power level to the divider is varied between the operational thresholds the 1/2 subharmonic content ranges from -6 to -14 db which is a reasonable power level variation.

The various spectrum plots of Figures 5-26 to 5-30 indicate that a usable m/2 harmonic spectrum, for m > 1, is also available. It appears that this spectrum follows the output predicted for the broadband step recovery diode multiplier. In order to determine this analytically, the solution of the system of equations defining the divider operation are required. This has not been done.

The various dividers constructed were operated over a 0° to 50°C temperature range with no apparent degradation in performance.

5.3 TRANSLATION.

In this section the experimental work that was performed using the ring modulator discussed in Section 3.2.4 is presented. The modulators were designed to operate over as large a frequency range as possible, and are schematically represented as shown in Fig. 5-31.

The balanced transformers used in the modulator were equivalent to those discussed in Section 5.2. Various diode quads were chosen to have dc characteristics which were matched to less than 10 my deviation from each other over a current range of 0-30 ma.

Conversion loss characteristics for two different sets of transformer windings are given in Fig. 5-32 and Fig. 5-33.

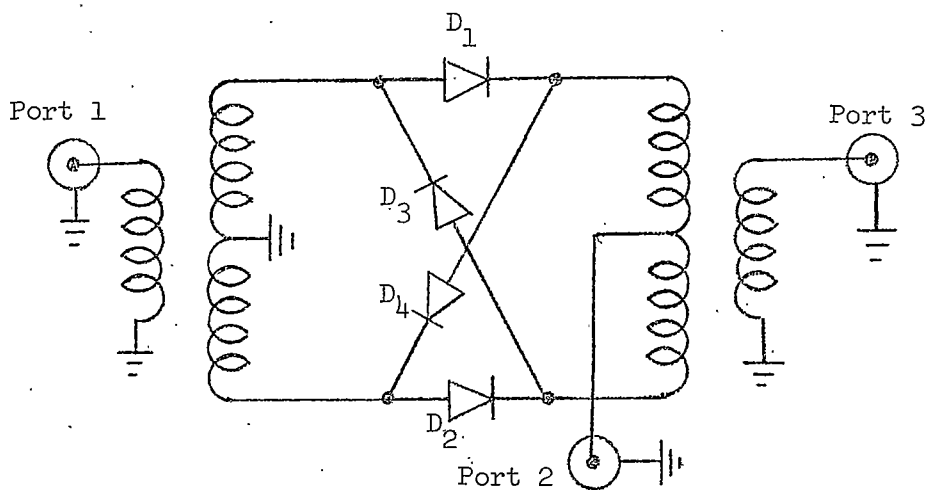


Fig. 5-31. RING MODULATOR CIRCUIT.

The 10-turn transformer had its trifilar winding equally spaced around the periphery of a toroid core. The 3-turn transformer windings were laid in as close as possible to each other. Each of the sets of characteristics are the averages of data taken for several different transformers and several different diode quads.

For the data presented the translating (switching) signal was applied to port 2 at +7 dbm and the signal to be translated applied to port 1. Power levels of -10 dbm and -20 dbm were used as the drive level at port 1. From Fig. 5-32, 33 it can be seen that the modulator with 10-turn transformers yield superior performance over the lower frequency range of 10 to 400 MHz, whereas, for the frequency range extending on up to 1 GHz the modulator with fewer turns provides more acceptable performance characteristics.

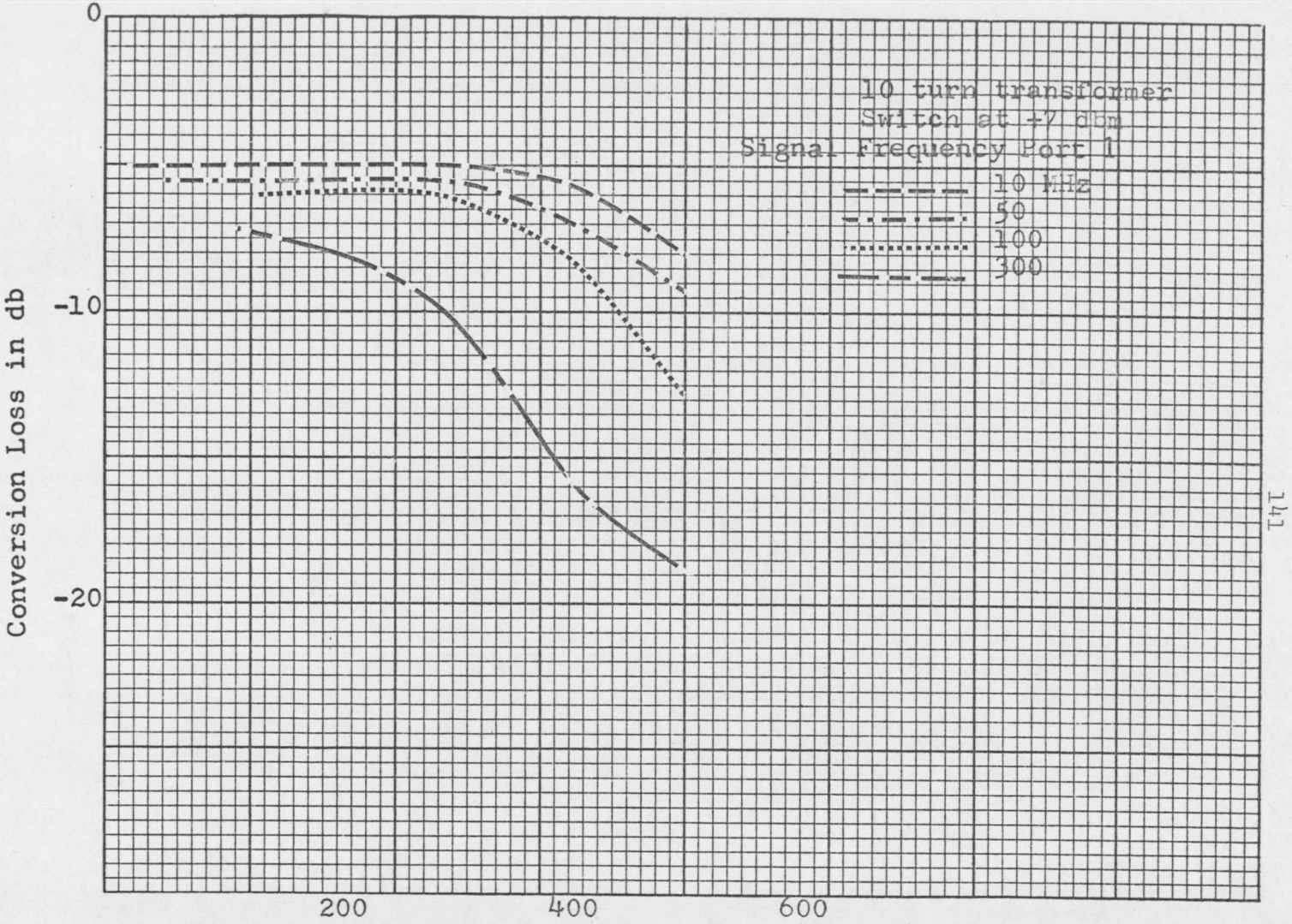


Fig. 5-32. FULL LATTICE MODULATOR CONVERSION LOSS.

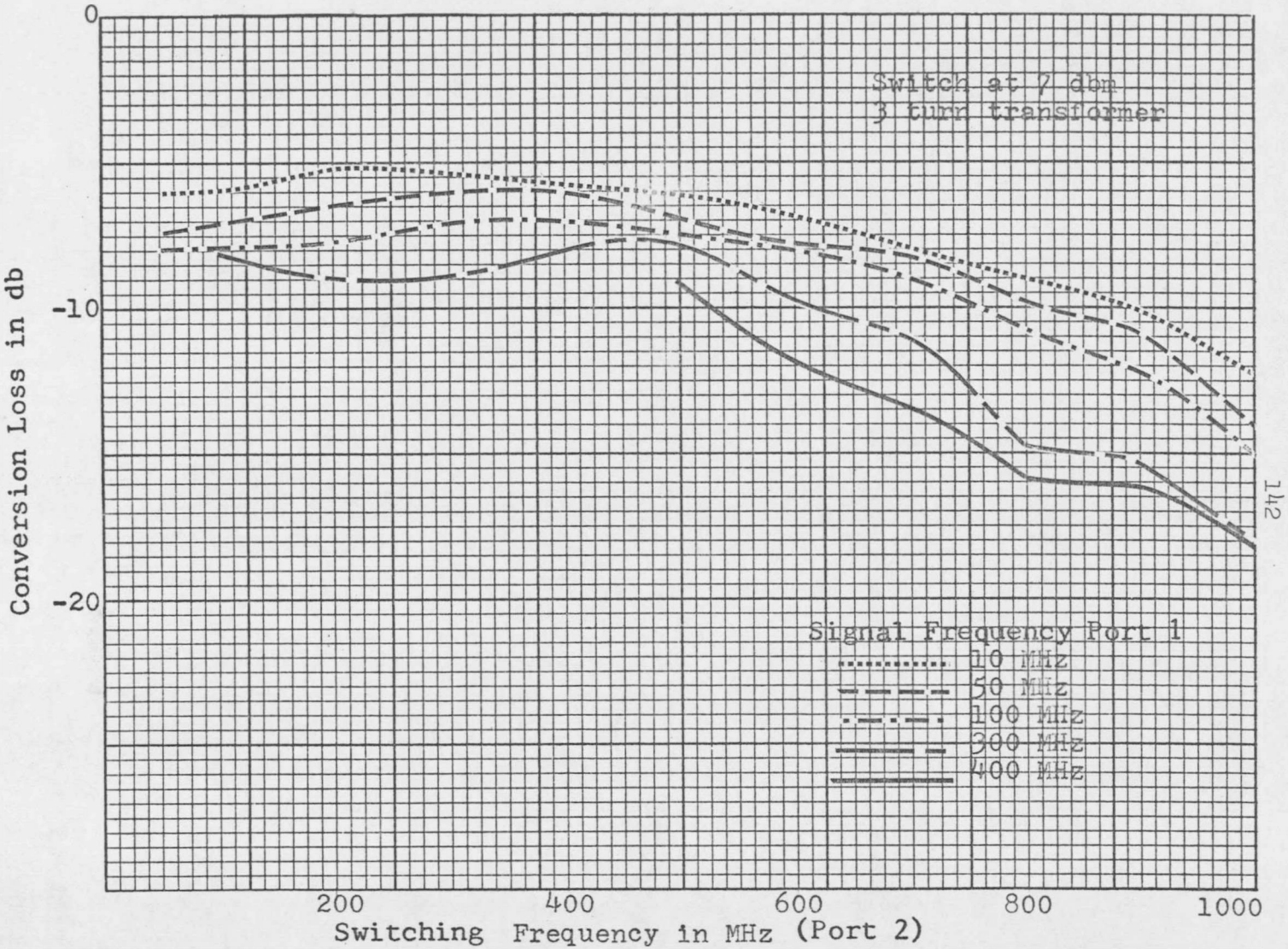


Fig. 5-33. FULL LATTICE MODULATOR CONVERSION LOSS.

The carrier rejection curves of Fig. 5-34 indicate the relative balance presented to the circuit by the transformers and diodes quads. The carrier rejection labeled "forward" was measured across a 50 ohm load at port 3 with port 2 terminated in 50 ohm and a drive signal of +7 dbm at port 1. The reverse rejection was measured with port 1 and 3 interchanged. The rejection presented by the modulators using 3-turn transformers is much more acceptable than the 10-turn transformer modulators. This is as expected since the matching of lead lengths and uniformity of winding spacing between turns is easier to control.

From Fig. 5-35 the effect of the input impedance variation of the modulator is shown. The curves present the deviation in db as recorded from a voltmeter (see Fig. 5-2) between the voltage level across 50 ohms and the voltage level applied to port 1 with ports 2 and 3 terminated in 50 ohms.

Typical impedance characteristics (R_p, X_p, Z) for the two transformers used are presented in Fig. 5-36. The data was obtained from rf bridge measurements with the transformer center tap grounded and a load of 200 ohms across the secondary windings.

The mixer balance from port 1 to port 3 is relatively the same as the forward rejection to port 3. Port 3 to port 2 is typically 5-10 db less than the reverse rejection measured at port 1. The balance measured from port 2 to port 1 is typically 5 db less than

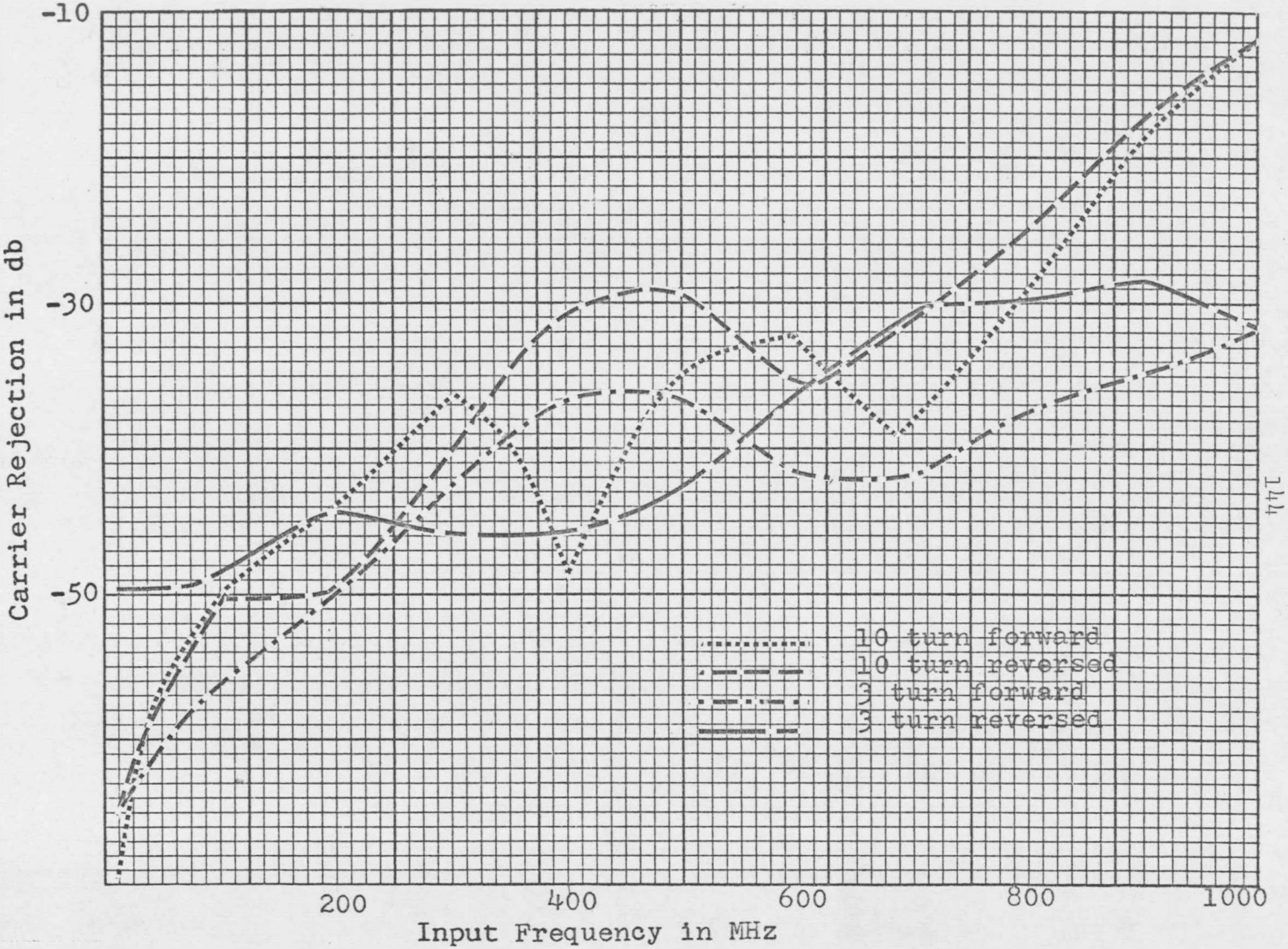


Fig. 5-34. FULL LATTICE CARRIER REJECTION.

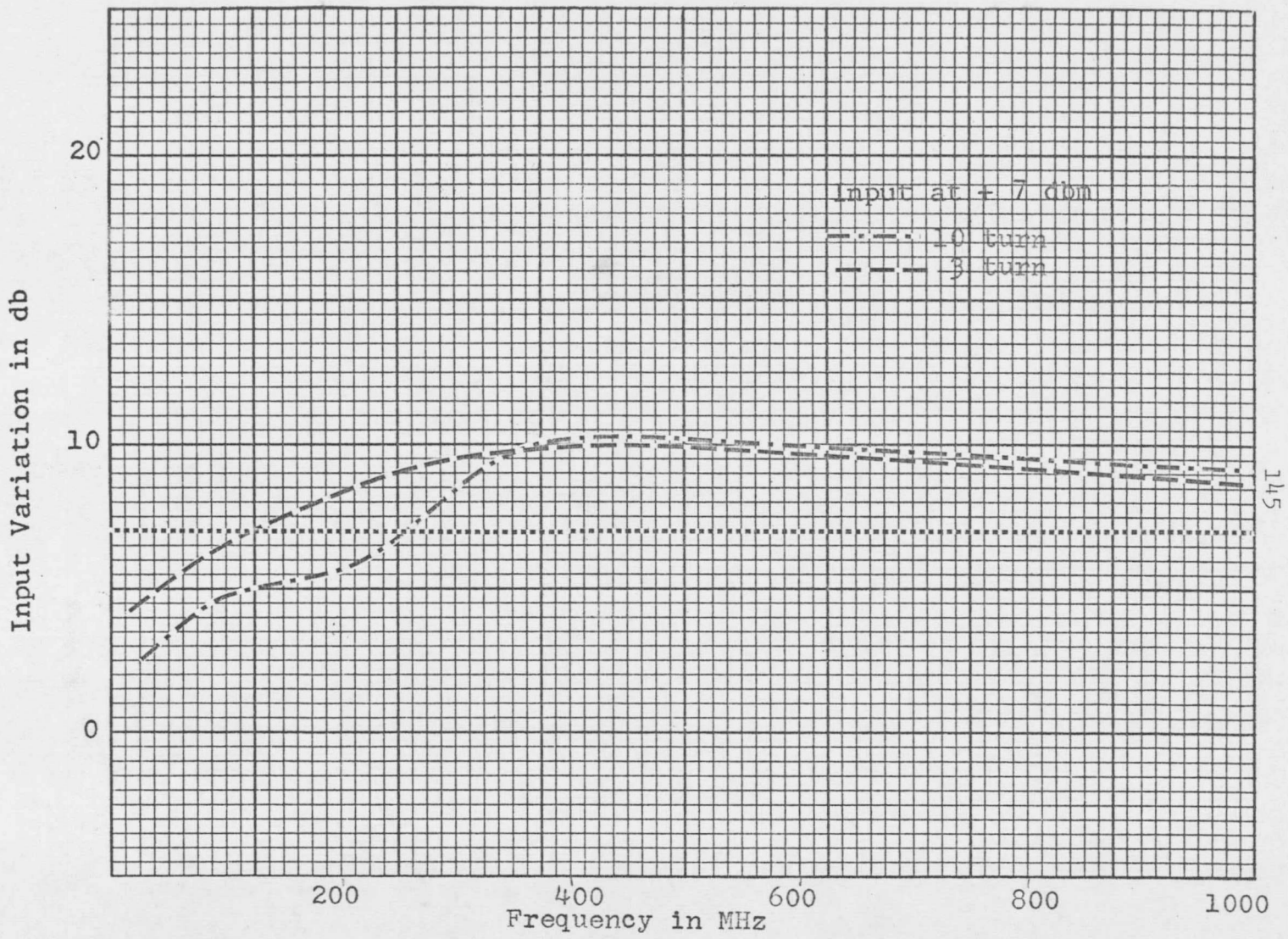


Fig. 5-35. EFFECT OF FULL LATTICE INPUT IMPEDANCE VARIATION.

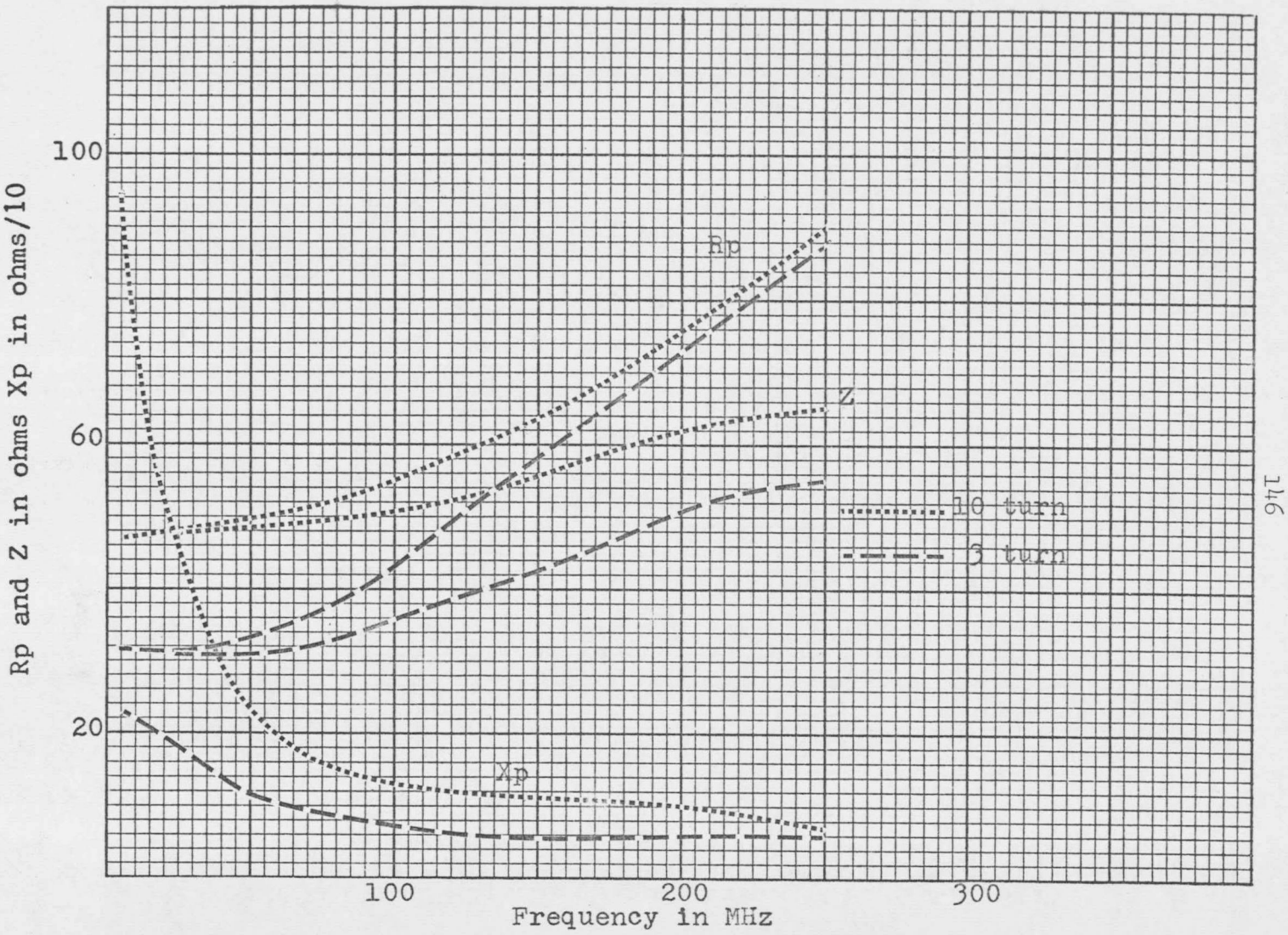


Fig. 5-36. BALANCED TRANSFORMER DATA.

the forward rejection. The balance from port 2 to port 3 is approximately 10 db less than the reverse rejection.

The mixer intermodulation products are typically less than 45 db (referred to switching level of port 2) under the drive conditions for which data has been presented.

These mixers have been operated over the temperature range of 0° to 50°C with no apparent degradation in performance.

6.0 SUMMARY AND CONCLUSIONS

In the preceding chapters it has been demonstrated that effective use can be made of several recently developed semiconductor diodes in wide-band techniques for the synthesis of precision frequencies over wide frequency ranges at VHF and UFH frequencies. The application of these devices was examined in detail under the operating conditions associated with frequency translation, multiplication and division.

6.1 SUMMARY OF RESULTS.

As a result of this research effort the performance level of the various signal operations investigated can be reasonably anticipated.

The diode harmonic generator constructed produced usable outputs beyond 1 GHz within 8 db of the predicted values. Both of these circuits have applications where frequency doubling is desired.

The performance of broadband SRD multipliers with resistive loads can be predicted by using the conversion curves of Fig. 4-25 and the diode transition curves of Fig. 5-8. In applications requiring harmonics of the third to the sixth, a diode can be selected that will provide usable output levels. Holding the bias voltage of the diode at zero volts will not seriously degrade the multiplier performance while eliminating any temperature dependence of the output on the biasing circuitry.

The output of a broadband SRD generator with a resonant load can be predicted by using the curves of Fig. 4-34 or Fig. 4-35 and Fig. 5-8. To use these curves circuit Q's must be known or estimated. The spectral output of this multiplier peaks at the desired harmonic with a better conversion efficiency than that of the resistive load generator. However, the frequency range of operation is limited by the resonant-load characteristics.

The realization of a broadband divider circuit can be obtained from the calculated values for the various circuit elements given by the relationship of equations (4-10). Proper subharmonic spectrum generation of the order 1/2 was obtained through 1 GHz employing the hp 0151 diode. Other diodes used were useful over various frequency ranges depending upon their capacitance, minority carrier lifetime and transition time. The hp 0151 diode had the smallest values for all three of the above mentioned parameters. The dividers tested generated a m/2 spectrum which appears to follow the broadband SRD generator characteristics.

The various circuits discussed above all have outputs that contain a number of other harmonics along with the desired one. Additional filtering must be provided in applications where the output must contain a single frequency. If the various analyses are to be used, the additional bandpass circuitry must be isolated from the circuit outputs under discussion by either an amplifier with a

resistive input impedance or by a resistive attenuator. A voltage-tunable narrow-band filter could be used in applications where filtering is required over a certain frequency range.

Ring modulators to perform the frequency translation function can be implemented using carefully constructed trifilar transformers and matched diode quads that have a very broad operating frequency range. The 10-turn transformer configuration provides an operational frequency range of 10 to 400 MHz and the 3-turn configuration has a usable range extending to 1 GHz. Carrier rejection of -30 db can be maintained with a conversion loss of 5-10 db for switching levels of +7 dbm and drive levels of -20 to -10 dbm.

6.2 SUGGESTIONS FOR FURTHER RESEARCH.

It is suggested that further analysis be done in the following areas:

(1) Further analysis associated with the prediction of the 1/2 order harmonic spectrum energy of the frequency division technique discussed is recommended.

(2) To date, the analysis of the step recovery diode circuit operation has been limited to fixed bias operation. It is suggested that an investigation of allowing the bias to be varied by a low frequency signal be undertaken. With further investigation it might be possible to employ this technique

to produce phase control over the output signal.

APPENDIX

APPENDIX A

DERIVATION OF SHORT-TERM FREQUENCY STABILITY

In this section a relationship between short-term frequency stability of a signal and the signal-to-noise ratio is presented which can be used in determing the effects of signal operations on the basic stability of an oscillator system by considering the degradation of the signal-to-noise ratio. The analysis presented here can be obtained from references [21] and [22].

Short-term frequency stability is expressed as the ratio of the rms frequency deviation in the measuring interval τ to the nominal frequency of operation, where the frequency deviation is due to random noise effects. Long-term effects of aging and temperature changes along with initial startup transient effects are not considered.

For this discussion the output signal characteristics of the signal source (oscillator) are of interest and not the oscillator model which would present the mechanisms which produce the output signal and noise. The noise effects in the output of a signal source are classified into two types. Type I noise is considered to be generated within the oscillator. A noise pulse within causes a permanent phase change that cannot be corrected. Type I noise effects cause a cumulative phase error as additional pulses appear. Type II noise includes the noise which is external to the basic oscillator and does not have an effect on the basic oscillator.

Type II noise results in a phase error which is not cumulative. The effects of Type II noise are only instantaneous. Therefore, Type I is classed as an infinite memory and Type II is zero memory.

Consider the oscillator signal designated as

$$s(t) = A \cos \omega_o t \tag{A-1}$$

with the noise expressed as

$$v_n(t) = v_c \cos \omega_o t + v_s \sin \omega_o t \tag{A-2}$$

where ω_o is the midband angular frequency and v_c and v_s are uncorrelated functions of time which vary slowly and randomly as narrow-band random processes.

The signal of interest is expressed as

$$\begin{aligned} v_1(t) &= s(t) + v_n(t) \\ &= (v_c+A) \cos \omega_o t + v_s \sin \omega_o t. \end{aligned} \tag{A-3}$$

An equivalent form for (A-3) is expressed as

$$v_1(t) = \rho(t) \cos [\omega_o t + \phi(t)] \tag{A-4}$$

where

$$\rho^2(t) = [v_c + A]^2 + v_s^2 \tag{A-5}$$

$$\tan \phi (t) = \frac{v_s}{v_c+A} \tag{A-6}$$

The function $\rho(t)$ is called the envelope of the wave and $\phi(t)$ is called the phase of the wave. With large signal-to-noise

ratios

$$\phi(t) \cong v_s/A \tag{A-7}$$

From (A-7) the cumulative phase error due to Type I noise for k pulses in the measuring time τ is given as

$$[v_1 + v_2 + \ldots v_k]/A = \frac{1}{A}\sum_{i=1}^{k} v_i \tag{A-8}$$

The number of independent noise pulses from the sampling theorem is

$$k_p = 2W_1\tau \tag{A-9}$$

where W_1 is the single-sided bandwidth of the noise. Since the phase error due to Type II noise pulses is not cumulative, the error due to this type of noise in the measuring interval is expressed as

$$\frac{1}{A}[V(\tau)-V(o)] \tag{A-10}$$

The total phase error is expressed as

$$\phi_e = \frac{1}{A}\left[\sum_{i=1}^{2W_1\tau} v_i + V(\tau) - V(o)\right] \tag{A-11}$$

The mean square phase deviation is given by

$$\overline{(\Delta\phi_\tau)^2} = \overline{[\phi_\tau-\omega_o\tau]^2} \tag{A-12}$$

where

$$\phi_\tau = \omega_o\tau + \phi_e$$

Since the noise pulses are independent, (A-11) and (A-12) give

$$\overline{(\Delta\phi_\tau)^2} = \frac{1}{A^2}\,\overline{[\Sigma v_i^{\,2} + V^2(\tau)+V^2(o)]} \qquad \text{(A-13)}$$

Now from (A-1) the signal power is $P = A^2/2$ and the noise power from (A-2) is

$$N = \frac{1}{2}\,(\overline{v_c^{\,2}} + \overline{v_s^{\,2}}). \qquad \text{(A-14)}$$

Since v_c and v_s are from independent random process with the same variance, (A-14) can be expressed as

$$N = \overline{v_c^{\,2}} = \overline{v_s^{\,2}} \qquad \text{(A-15)}$$

Using equation (A-8) and (A-15) yields

$$\overline{\Sigma_i v_i^{\,2}} = 2W_1\tau\,\overline{v_s^{\,2}} = 2W_1N_1\tau \qquad \text{(A-16)}$$

and the mean square phase deviation becomes

$$\overline{(\Delta\phi_\tau)^2} = \frac{W_1\tau N_1}{P} + \frac{N_2}{P} \qquad \text{(A-17)}$$

where N_1 and N_2 are the Type I and Type II noise powers respectively.

The mean square frequency deviation is expressed as

$$\overline{(\Delta\omega_\tau)^2} = \tau^{-2}\,\overline{(\Delta\phi_\tau)^2} = \frac{W_1N_1}{P\tau} + \frac{N_2}{P\tau^2} \qquad \text{(A-18)}$$

and the fractional frequency stability is

$$S_\tau = \left[\frac{(\Delta\omega_\tau)^2}{\omega_o}\right]^{1/2} = \left[\frac{W_1N_1}{P\omega_o^{\,2}\tau} + \frac{N_2}{P\omega_o^{\,2}\tau^2}\right]^{1/2} \qquad \text{(A-19)}$$

The signal-to-noise ratio for the noise can be expressed as

$$(SNR)_1 = \frac{P}{N_1}$$

$$(SNR)_2 = \frac{P}{N_2} \quad . \tag{A-20}$$

Using (A-20) in (A-19) yields

$$S_\tau = \frac{1}{\omega_o} \left[\frac{W_1}{(SNR)_1 \tau} + \frac{1}{(SNR)_2 \tau^2} \right]^{1/2} \tag{A-21}$$

Equation (A-21) is the principal result of this Appendix and shows the importance of both types of noise power, the Type I bandwidth, and the measuring interval.

APPENDIX B

NONLINEAR DEVICE ANALYSIS.

In this discussion the output relationship for a general non-linear device is determined from analyses presented in references [22] and [23]. The input-output relationship for the general non-linear device is given by

$$V_o = \sum_{j=1} a_j v_{in}^{\ j} \tag{B-1}$$

where v_o is the output function. Assume an input to the device of

$$v_{in} = (A + V_c) \cos \omega_o t + v_s \sin \omega_o t \tag{B-2}$$

where

$v_c \cos \omega_o t + V_s \sin \omega_o t$ is narrow-band noise of center frequency f_o. The m^{th} term of (B-1) will yield the following terms of interest

$$v_{in}^{\ m} = (A+v_c)^m \cos^m \omega_o t + mv_s(A+v_c)^m \cos^{m-1} \omega_o t \sin \omega_o t. \tag{B-3}$$

With large signal-to-noise ratios at the input to the device only the linear noise terms will be of importance and (B-3) becomes

$$v_{in}^{\ m} \cong [A^m+mA^{m-1}v_c] \cos^m \omega_o t + mA^{m-1}v_s \cos^{m-1}\omega_o t \sin \omega_o t. \tag{B-4}$$

After appropriate trigonometric substitutions and manipulation, the signals in $v_{in}^{\ m}$ at the k^{th} harmonic of the input frequency (for $k = m-2p$) are

$$(V_{in})_k^m = [A^m + mA^{m-1}v_c]\, 2^{1-m} \binom{m}{\frac{1}{2}(m-k)} \cos \omega_o t$$

$$+ 2^{1-m}\, kA^{m-1}v_s \binom{m}{\frac{1}{2}(m-k)} \sin k\omega_o t, \qquad \text{(B-5)}$$

where $\binom{n}{r}$ or ${}_nC_r$ denote the binomial coefficient.

Using the above relationships the output power at the desired k^{th} harmonic is

$$P_o = 2^{1-2k} A^{2k} \left[\sum_{p=0} \left(\frac{A}{2}\right)^{2p} \binom{k+2p}{p} a_{k+2p} \right]^2 \qquad \text{(B-6)}$$

Now, if the condition

$$\frac{a_{k+2p+2}}{a_{k+2p}} \frac{P_{in}}{2} [(k+2p+2)] \underset{p+1}{} \quad (k+2p)^{-1} \ll 1 \qquad \text{(B-7)}$$

where

$$P_{in} = \frac{A^2}{2}$$

then (B-6) can be approximated as

$$P_0 = 2^{1-k} P_{in}^{\,k} a_k^{\,2} \left[1 + (k+2)\, P_{in} \frac{a_{k+2}}{a_k}\right] \qquad \text{(B-8)}$$

If the condiiton of (B-7) holds the noise output power becomes

$$N_0 = 2^{1-k} P_{in}^{\,k-1} N_i k^2 a_k^{\,2} \left[1 + \frac{(k+2)(k+1)}{k} P_{in} \frac{a_{k+2}}{a_k}\right]. \qquad \text{(B-9)}$$

The output signal-to-noise ratio becomes

$$(SNR)_o = \frac{(SNR)_i}{k^2} \left[1 - \frac{(k+2)}{k} \frac{a_{k+2}}{a_k} P_{in}\right] \qquad \text{(B-10)}$$

thus, if $a_k + 2p$, for some $p > 0$, is not zero

the $$(SNR)_o < \frac{(SNR)_i}{k^2} \qquad \text{(B-11)}$$

and the m^{th} law device, with $m > k$, will yield a lower signal-to-noise ratio and therefore a decreased signal stability.

APPENDIX C

CALCULATION OF THE HARMONIC SPECTRUM OF A CLIPPED SINE WAVE

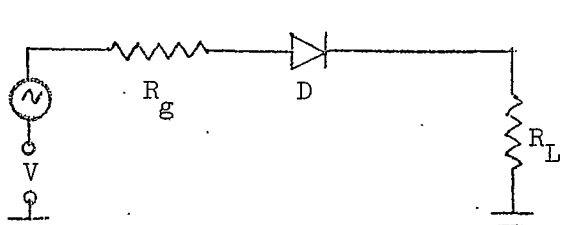


Fig. C-1. HARMONIC GENERATOR EQUIVALENT CIRCUIT.

Assuming the input voltage to be $V_m \cos \omega t$ the resulting output voltage across R_L for the interval $-\pi \leq \omega t \leq \pi$ is

$$v(t) = V'_m (\cos \omega t - \cos \theta) \quad \text{for } -\theta \leq \omega t \leq \theta$$
$$= 0 \quad \text{for } |\omega t| > \theta \qquad \text{(C-1)}$$

The output waveform is shown in Fig. C-2.

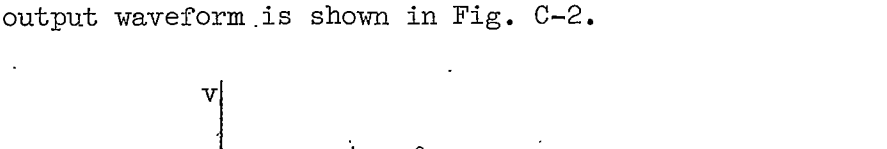


Fig. C-2. OUTPUT WAVEFORM FOR HARMONIC ANALYSIS OF THE CLIPPED SINE WAVE.

The output voltage, being an even function of time is representable by a cosine series. The normalized Fourier coefficients of cos nωt are

$$a_n = \frac{1}{\pi}\int_{-\theta}^{\theta}(\cos \omega t - \cos \theta)\cos n\omega t \; d\omega t$$

$$= \frac{1}{\pi}\left[\frac{\sin(n-1)\theta}{(n-1)} + \frac{\sin(n+1)\theta}{n+1} - \frac{2 \sin n\theta \cos \theta}{n}\right]. \qquad (C-2)$$

The conversion loss in db at the n^{th} harmonic is defined by

$$PL_n = 10 \log \frac{\text{Power available from generator}}{\text{Power output at } n^{th} \text{ harmonic}} \qquad (C-3)$$

For the assumed input voltage, the available power at the input is

$$P_{in} = \frac{V_m^2}{8R_g}. \qquad (C-4)$$

The output power at the n^{th} harmonic is

$$P_n = \frac{V_m^2 a_n^2 R_L}{2(R_g + R_L)^2}. \qquad (C-5)$$

Substituting (C-4) into (C-3), the conversion loss for the n^{th} harmonic is

$$P_{LN} = -10 \log a_n^2 \qquad \text{for } R_g = R_L \text{ (in db)}. \qquad (C-6)$$

The computer programs used to calculated the conversion loss as a function of θ can be found in the computer program Appendix.

APPENDIX D

NONLINEAR CAPACITOR ANALYSIS

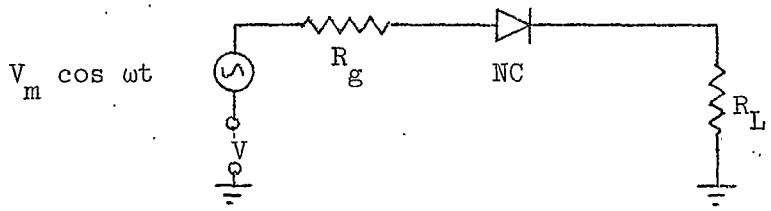


Fig. D-1. NONLINEAR CAPACITOR EQUIVALENT CIRCUIT.

Assuming the input voltage to be $V_m \cos \omega t$, the resulting output voltage across R_L for the interval $-\theta \leq \omega t \leq \phi$ is

$$v(t) = V_m' (\cos \omega t - \cos \theta) \quad -\theta < \omega t < \phi$$

$$= 0 \qquad \phi < \omega t < 2\pi - \theta \qquad \text{(D-1)}$$

The output waveform is shown in Fig. D-2.

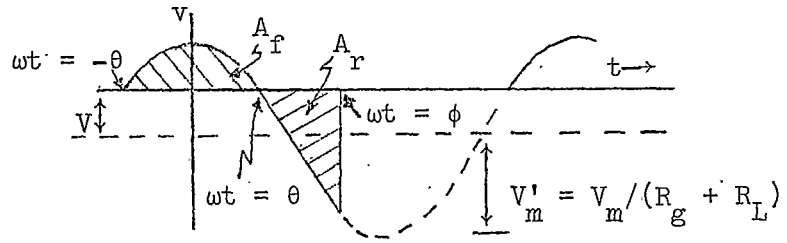


Fig. D-2. OUTPUT WAVEFORM FOR NONLINEAR CAPACITOR ANALYSIS.

When the net voltage across the nonlinear capacitor is in the forward direction, the capacitance for this state is very large. Since the capacitance is large, the current amplitude is determined by R_L and R_g. When the applied voltage is reversed, all the charge which was stored during the forward bias interval will be recovered. Referring to Fig. D-2, this requires area $A_f = A_r$. When $\omega t = \phi$

all the charge is recovered, the current returns abruptly to zero. The requirement between A_f and A_r is expressed as

$$A_f = \int_{-\theta}^{\theta} V_m' (\cos \omega t - \cos \theta)\, d\omega t$$

$$= 2V_m' (\sin \theta - \theta \cos \theta)$$

$$A_r = \int_{\theta}^{\phi} V_m' (\cos \omega t - \cos \theta)\, d\omega t$$

$$= V_m' (\sin \phi - \sin \theta - \phi \cos \theta + \theta \cos \theta) \qquad \text{(D-3)}$$

and from $A_f = -A_r$

$$\sin \phi - \phi \cos \theta = \theta \cos \theta - \sin \theta. \qquad \text{(D-4)}$$

The solution of this equation gives values of ϕ for corresponding specific values of θ. Numerical values for ϕ may be obtained from Fig. D-3.

The normalized Fourier coefficients of the expansion of (D-1) for $n \neq 1$ are given by

$$a_n = \frac{1}{\pi} \left[\frac{\sin(n-1)\phi}{2(n-1)} + \frac{\sin(n+1)\phi}{2(n+1)} - \frac{\cos\theta \sin n\phi}{n} \right.$$

$$\left. + \frac{\sin(n-1)\theta}{2(n-1)} + \frac{\sin(n+1)\theta}{2(n+1)} - \frac{\cos\theta \sin n\theta}{n} \right]$$

$$b_n = \frac{1}{\pi} \left[- \frac{\cos(n-1)\phi}{2(n-1)} - \frac{\cos(n+1)\phi}{2(n+1)} + \frac{\cos\theta \cos n\phi}{n} \right.$$

$$\left. + \frac{\cos(n-1)\theta}{2(n-1)} + \frac{\cos(n+1)\theta}{2(n+1)} - \frac{\cos\theta \cos n\theta}{n} \right]. \qquad \text{(D-5)}$$

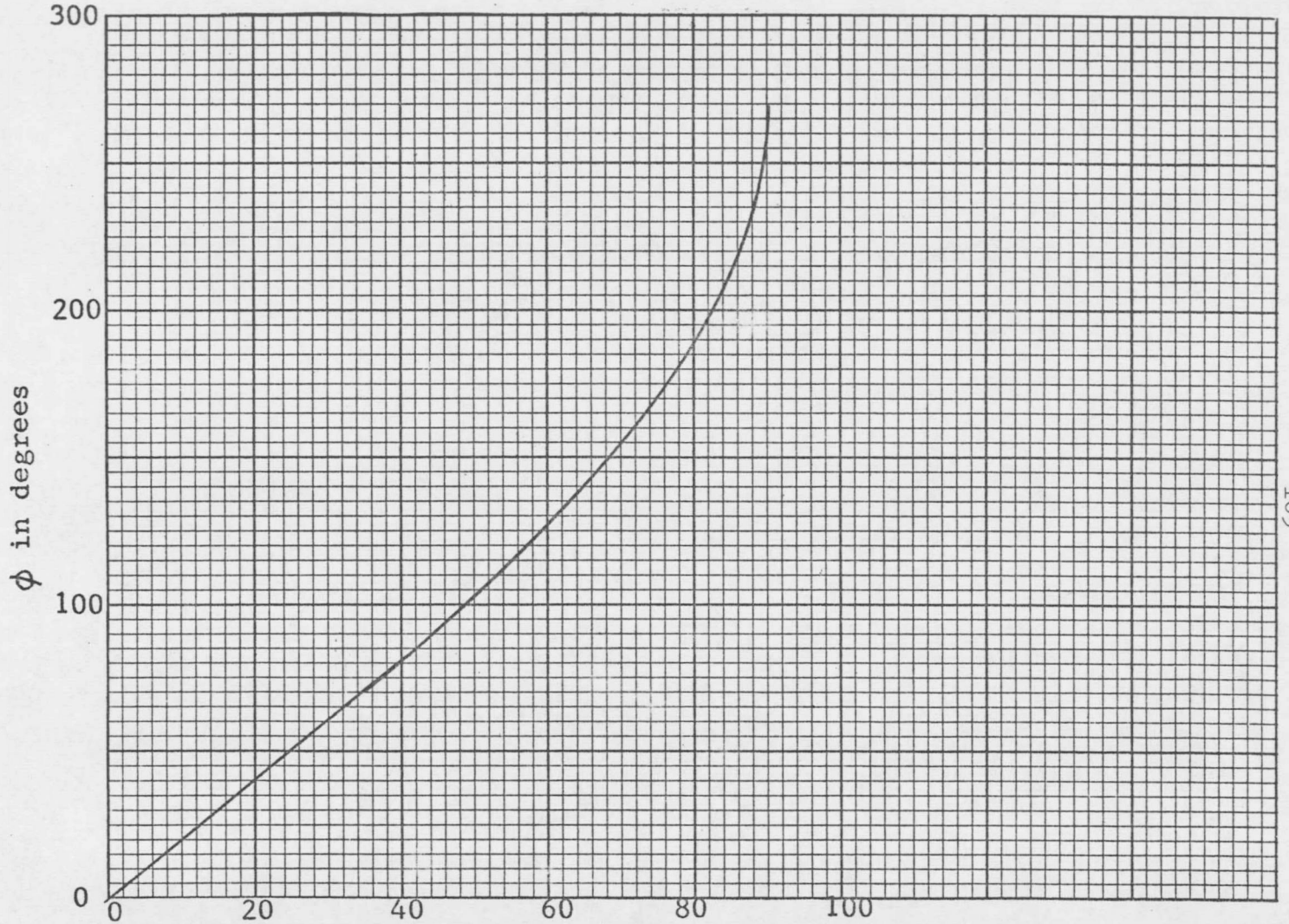


Fig. D-3 ϕ and Θ FOR NONLINEAR CAPACITOR ANALYSIS.

Here a_n and b_n are the coefficients of cos $n\omega t$ and sin $n\omega t$ respectively.

The output power at the n^{th} harmonic is

$$P_n = \frac{V_m^2 R_L}{2(R_g+R_L)^2} \quad (a_n^2 + b_n^2). \tag{D-6}$$

The conversion loss for the n^{th} harmonic is (for $R_L = R_g$)

$$P_{Ln} = -10 \log (a_n^2 + b_n^2) \quad \text{(in db)}. \tag{D-7}$$

The computer program used to calculate the conversion loss as a function of θ and ϕ can be found in the computer program appendix.

APPENDIX E

STEP RECOVERY DIODE ANALYSIS

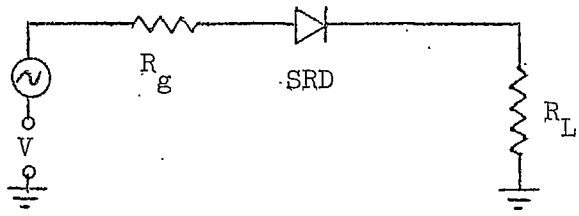


Fig. E-1. STEP RECOVERY DIODE GENERATOR EQUIVALENT CIRCUIT.

Assuming the input voltage to be $V_m \sin \omega t$ the resulting output voltage across R_L for the interval $-\theta \leq \omega t \leq \theta + \phi$ is

$$v(t) = V'_m [\sin(\omega t + \theta) - \sin \theta] \quad \theta \leq \omega t \leq \theta + \phi$$
$$= 0 \qquad \theta + \phi < \omega t < 2\pi + \theta \qquad \text{(E-1)}$$

The output waveform is shown in Fig. E-2.

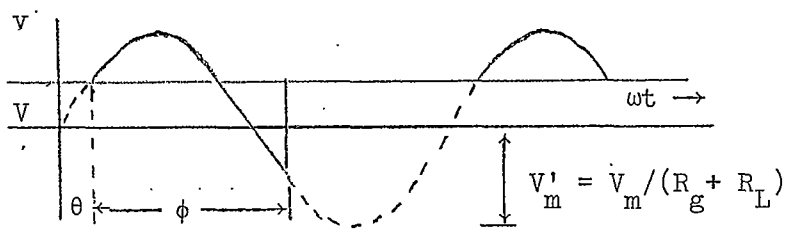


Fig. E-2. OUTPUT WAVEFORM FOR STEP RECOVERY DIODE CIRCUIT.

The steady-state condition for θ and ϕ are obtained by considering the continuity of charge (Q). The total stored charge is expressed as

$$\frac{dQ}{dt} + \frac{Q}{\tau} = i(t), \qquad \text{(E-2)}$$

where

$$i(t) = \frac{V_m}{R_g+R_L} [\sin(\omega t + \theta) - \sin\theta] \qquad \text{(E-3)}$$

and τ is the recombination lifetime.

The solution of equation (E-2) for Q is

$$Q = \frac{V_m}{R_g+R_L} \left(\frac{\omega}{\omega^2+\tau^{-2}} \right) [\omega\tau + \cos\theta)\, e^{\frac{-\omega t}{\omega\tau}} + \left(\frac{\cot\theta + 1}{\omega\tau} \right) \sin\omega t$$

$$+ \left(\frac{1}{\omega\tau} - \cot\theta \right) \cos\omega t - \left(\frac{1}{\omega\tau} + \omega\tau \right)] \qquad \text{(E-4)}$$

At $\omega t = \phi$ the charge (Q) is zero, substituting this condition into (E-4) gives the solution for θ in terms of $\omega\tau$ and ϕ as

$$\text{Tan}\,\theta = \frac{\sin\phi - \omega\tau\cos\phi + \omega\tau e^{\frac{-\phi}{\omega\tau}}}{-\omega\tau\sin\phi - \cos\phi + \omega^2\tau^2 (1-e^{-\phi/\omega\tau}) + 1} \qquad \text{(E-5)}$$

The computer programs used to calculate θ as a function of ϕ and $\omega\tau$ can be found in the computer program appendix.

The normalized Fourier coefficients of the expansion of (E-1) are given by

$$a_1 = \frac{1}{2\pi} [\sin(\theta + \phi) - \sin\theta]^2$$

for $n \neq 1$

$$a_n = \frac{1}{2\pi} \left[\frac{\cos(n-1)(\theta+\phi) - \cos(n-1)\theta}{(n-1)} - \frac{\cos(n+1)(\theta+\phi) - \cos(n+1)\theta}{(n+1)} \right.$$

$$\left. -2\,\frac{\sin\theta\sin n(\theta+\phi) - \sin\theta\sin n\theta}{n} \right]$$

$$b_1 = \frac{1}{2\pi}\left[\phi - \frac{1}{2}\sin 2(\theta+\phi) + 2\sin\theta\cos(\theta+\phi) - \sin\theta\cos\theta\right]$$

for $n \neq 1$

$$b_n = \frac{1}{2\pi}\left[\frac{\sin(n-1)(\theta+\phi) - \sin(n-1)\theta}{(n-1)} - \frac{\sin(n+1)(\theta+\phi) - \sin(n+1)\theta}{(n+1)} + 2\,\frac{\sin\theta\cos n(\theta+\phi) - \sin\theta\cos n\theta}{n}\right] \qquad \text{(E-6)}$$

Here a_n and b_n are the coefficients of $\cos n\omega t$ and $\sin n\omega t$ respectively.

The output power at the n^{th} harmonic is

$$P_n = \frac{V_m^2 R_L (a_n^2 + b_n^2)}{2(R_g + R_L)^2} \qquad \text{(E-7)}$$

The conversion loss for the n^{th} harmonic is (for $R_L = R_g$)

$$P_{Ln} = -10 \log (a_n^2 + b_n^2) \text{ (in db)}. \qquad \text{(E-8)}$$

The computer program used to calculate the conversion loss as a function of $\omega\tau$, θ, and ϕ can be found in the computer program appendix. Values used in the calculation for $\omega\tau$, θ, and ϕ were generated using the computer program for equation (E-5).

For the discussion that follows the load resistance R_L in the circuit of Fig. E-1 is replaced by a resonant circuit $R_L LC$. The harmonic power generation of this circuit is restricted to the following operation. When the applied voltage across the diode is

positive, diode conduction starts and current flows in the circuit until the charge that has passed through the diode becomes zero. At this time the diode switches off leaving the current I_o flowing in the inductance. The stored energy is dissipated in the load before the beginning of the start of the next conduction period. The results of the analysis will be the determination of the harmonic generating efficiency. The analysis considers two conversion losses and the overall total loss being the sum of two quantities.

The equivalent circuits associated with this manner of operation are shown in Fig. E-3 for the conducting and nonconducting states.

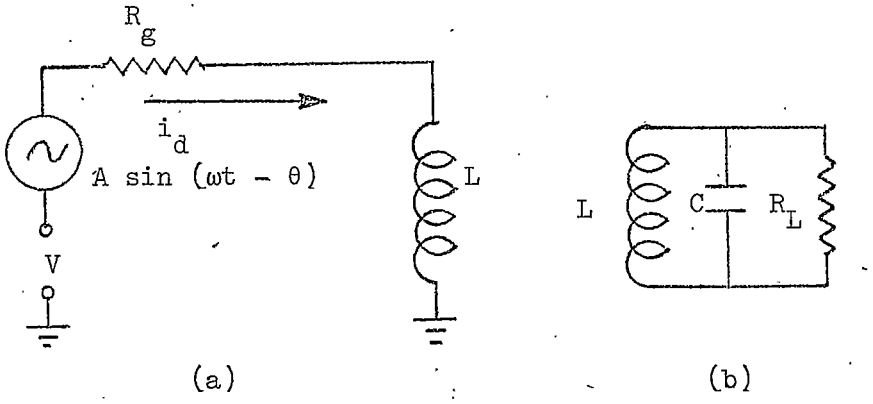


Fig. E-3. HARMONIC GENERATOR WITH RESONANT LOAD EQUIVALENT CIRCUIT.

(a) Conducting equivalent circuit.

(b) Nonconducting equivalent circuit.

The conducting state will be analyzed first. For convenience let V = kA. The circuit driving voltage v(t) is expressed as

$$v(t) = A\,[\sin(\omega t - \theta) + k] \tag{E-9}$$

where t is measured from the beginning of the conduction state.

For the circuit of Fig. E-3a, using the initial condition of i = o at t = o, the circuit current is expressed as

$$i_d = \frac{A}{R_g}\left[\sin\theta + \left[-\sin\theta + \frac{\sin\theta + Q_1\cos\theta}{1 + Q_1^2}\right] e^{-R_g t/L} + \frac{\sin(\omega t - \theta) - Q_1\cos(\omega t - \theta)}{1 + Q_1^2}\right] \tag{E-10}$$

Equation (E-10) can also be expressed as

$$i_d = \frac{A}{R_g}\left[\sin\theta + \frac{\sin(\omega t - \theta - \psi)}{(1 + Q_1^2)^{1/2}} + \left[-\sin\theta + \frac{\sin(\theta+\psi)}{(1+Q_1^2)^{1/2}}\right] \cdot e^{-R_g t/L}\right] \tag{E-11}$$

where

$$Q_1 = \frac{\omega L}{R_g}$$

and

$$\tan\psi = \frac{\omega L}{R_g}\,. \tag{E-12}$$

The charge (q) that has passed through the diode is expressed as

$$q = \int_o^t i_d\,dt. \tag{E-13}$$

From equation (E-13) the charge (q) is expressed as

$$q = \frac{A}{R_g}\left[t \sin\theta - \frac{\cos(\omega t - \theta - \psi) - \cos(\theta+\psi)}{\omega(1 + Q_1^2)^{1/2}}\right.$$

$$\left. - \frac{L}{R_g}\left[\sin\theta - \frac{\sin(\theta+\psi)}{(1 + Q_1^2)^{1/2}}\right](1 - e^{-R_g t/L})\right] \qquad \text{(E-14)}$$

If $\omega t = \phi$ when $q = o$, the diode ceases conduction and a relationship in terms of conduction constants θ and ϕ and the circuit parameter Q_1 is given by

$$\tan\theta = \frac{1 - \cos\phi - Q_1 \sin\phi + Q_1^2(1 - e^{-\phi/Q_1})}{Q_1 - Q_1\cos\phi + \sin\phi - (1+Q_1^2)\phi + Q_1^3(1 - e^{-\phi/Q_1})} \qquad \text{(E-15)}$$

The current in the coil at the end of the conduction state is obtained by substituting $\omega t = \phi$ into (E-10) which yields

$$I_o = \frac{A}{R_g}\left[\sin\theta + \left[\frac{Q_1\cos\theta - Q_1^2\sin\theta}{1 + Q_1^2}\right] e^{-\phi/Q_1}\right.$$

$$\left. + \frac{\sin(\phi-\theta) - Q_1\cos(\phi-\theta)}{1 + Q_1^2}\right]$$

and

$$I_o \triangleq \frac{A}{R_g} I \qquad \text{(E-16)}$$

The energy stored in the coil at $\omega t = \phi$ is

$$J = \frac{1}{2} L I_o^2 = \frac{1}{2}\frac{LA^2I^2}{R_g^2} \text{ joules.} \qquad \text{(E-17)}$$

The total harmonic power associated with (E-17) is expressed as

$$P_H = \frac{\omega}{2\pi}\left(\frac{LI_o^2}{2}\right) = \frac{\omega L A^2 I^2}{4\pi R_g^2} \text{ watts.} \qquad \text{(E-18)}$$

A conversion loss can now be defined associated with the conduction interval as

$$P_{L1} = 10 \log \left[\frac{\text{Available Power}}{P_H} \right] \qquad \text{(E-19)}$$

where

$$\text{Power Available} = A^2/8\, R_g \quad \text{for } V < o.$$

Substituting into (E-19), the conversion loss becomes

$$P_{L1} = 10 \log \left(\frac{\pi}{2Q_1 I^2} \right) \text{ db.} \qquad \text{(E-20)}$$

Numerical data for P_{L1} was obtained using equations (E-15) and (E-16) assuming values for ϕ and Q_1 by the digital computer. The program used in the computation is given in the computer program appendix.

Now attention will be turned to the nonconducting state with the equivalent circuit being that of Fig. E-3b. It will be assumed that the circuit is tuned to the n^{th} harmonic with a reasonable value for Q_2 and that the initial energy of the capacitor is negligible compared to that of the inductor. With these assumptions the voltage across the circuit for the nonconducting state is

expressed as

$$v(t) = -\rho L\omega_n e^{\frac{-\omega_n t}{2Q_2}} \sin \omega_n t$$

where

$$\rho = \frac{EI}{R_g}, \quad Q_2 = n\omega C/G_L \text{ and } \omega_n = \frac{1}{(LC)^{1/2}} = n\omega \qquad \text{(E-21)}$$

and t is defined to be zero at the start of the nonducting state.

Now V_n, the magnitude of the voltage across the circuit at the harmonic frequency $n\omega$ is expressed as

$$V_n = 2|v_n| \qquad \text{(E-22)}$$

where

$$v_n = \frac{1}{T}\int_o^{mT} v(t)^{-jn\omega t} dt \quad m \leq 1. \qquad \text{(E-23)}$$

In (E-23) mT is the nonconducting state duration and equal to $(2\pi - \phi)/\omega$ and $T = 2\pi/\omega$.

From (E-23)

$$v_n = \frac{-\rho L\omega_n Q_2}{2\pi n}\left[1-e^{-n(\pi-\phi/2)/Q_2} + \frac{-1+e^{-\frac{(\frac{n}{Q_2}+j4n)(\pi-\frac{\phi}{2})}}}{1 + j4Q_2}\right] \qquad \text{(E-24)}$$

Now provided that most of the power from the damped oscillation has been dissipated when it is terminated by the start of the next conduction interval, the exact point at which the waveform terminates is immaterial. Therefore, suppose that $4n(\pi-\phi/2)$ is a multiple of 2π and provided $4Q_2 >> 1$, the last term in the brackets can be neglected in comparison to unity. With these approximations

v_n is expressed as

$$v_n \cong \frac{-\rho L \omega_n Q_2}{2\pi n} [1-e^{-n/Q_2} (\pi - \phi/2)]. \qquad \text{(E-25)}$$

The second conversion loss P_{L2} can be defined as

$$P_{L2} = 10 \log \left[\frac{P_H}{\text{Power at } n\omega \text{ in } R_L} \right]. \qquad \text{(E-26)}$$

Therefore, P_{L2} can be expressed as

$$P_{L2} = 10 \log \left[\frac{2P_H}{V_n^2 G_L} \right] \text{ db}$$

$$= 1.961 - 10 \log \left[\frac{Q_2}{n} (1-e^{-n(\pi - \phi/2)^2/Q_2} \right]. \qquad \text{(E-27)}$$

Numerical data was obtained assuming values for ϕ and Q_2/n by the digital computer. The program used in the computation is given in the computer program appendix.

For a given conduction characteristic ϕ, the total conversion loss in generating the harmonic $n\omega$ is found by adding P_{L1} and P_{L2} calculated from the appropriate circuit constants.

It was assumed in the analysis that the energy was all dissipated during the nonconducting state. A limit of one tenth of the initial energy left at the next conduction starting was determined experimentally [17]. The analysis also ignored the effects due to the capacitor during the conduction state. It can be shown by appropriate computation that for operational condition removed from

the maximum inductive energy condition that this approximation is reasonable and improves at the rate of n^2. Therefore its effect on the conduction characteristic ϕ will be small.

APPENDIX F

STEP RECOVERY DIODE FREQUENCY DIVIDER ANALYSIS

In this discussion the ideal nonlinear capacitor characteristics will be assumed for the step recovery diode. This is justified for $\omega\tau > 10$ as was presented in Chapter 4.

The analog simulation of the circuit shown in Fig. F-1 will be considered first, as it will be used as a subportion of the overall analog simulation of the divider circuit. The circuit consists of an ac. generator, v(t), in series with a bias source, V_o, driving the SRD diode and the resistive load, R_L. The diode starts to conduct when the voltage across it is zero and continues in the

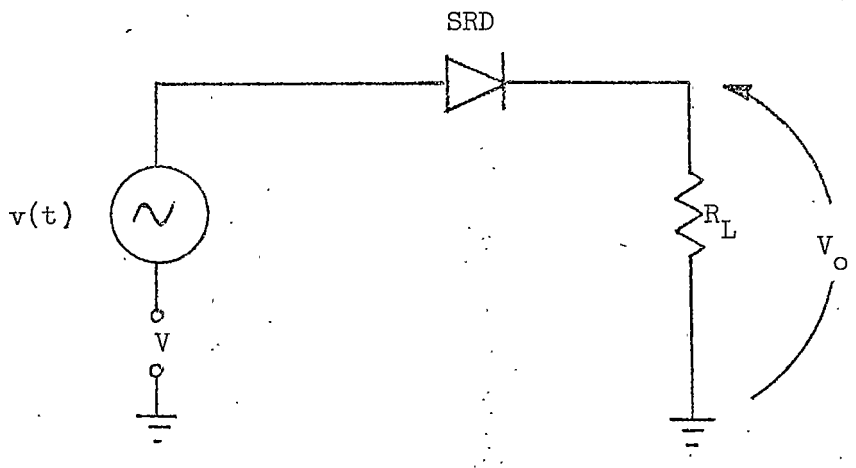


Fig. F-1. SERIES STEP RECOVERY DIODE AND RESISTANCE EQUIVALENT CIRCUIT.

conduction state until the net charge that has passed through it is zero. The diode stops conducting when the charge that has passed through it is zero and remains nonconducting until the voltage across it again becomes zero.

The analog simulation of this circuit is given in Fig. F-2. Fig. F-3 presents the input output relationships for the simulated circuit for a value of $\psi_o + V = -.5v$. The simulation presented is actually for a negative v(t) in with the output of amplifier 47 providing $v(t) - (\psi_o + V)$. These polarities are required in the overall simulation that follows for the complete divider.

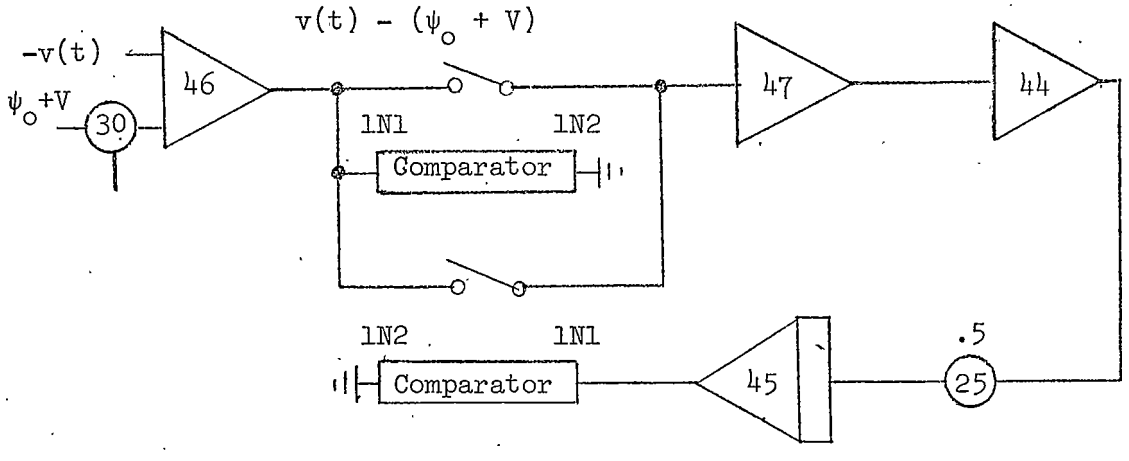


Fig. F-2. BLOCK DIAGRAM OF STEP RECOVERY DIODE IN SERIES WITH R_L SIMULATION.

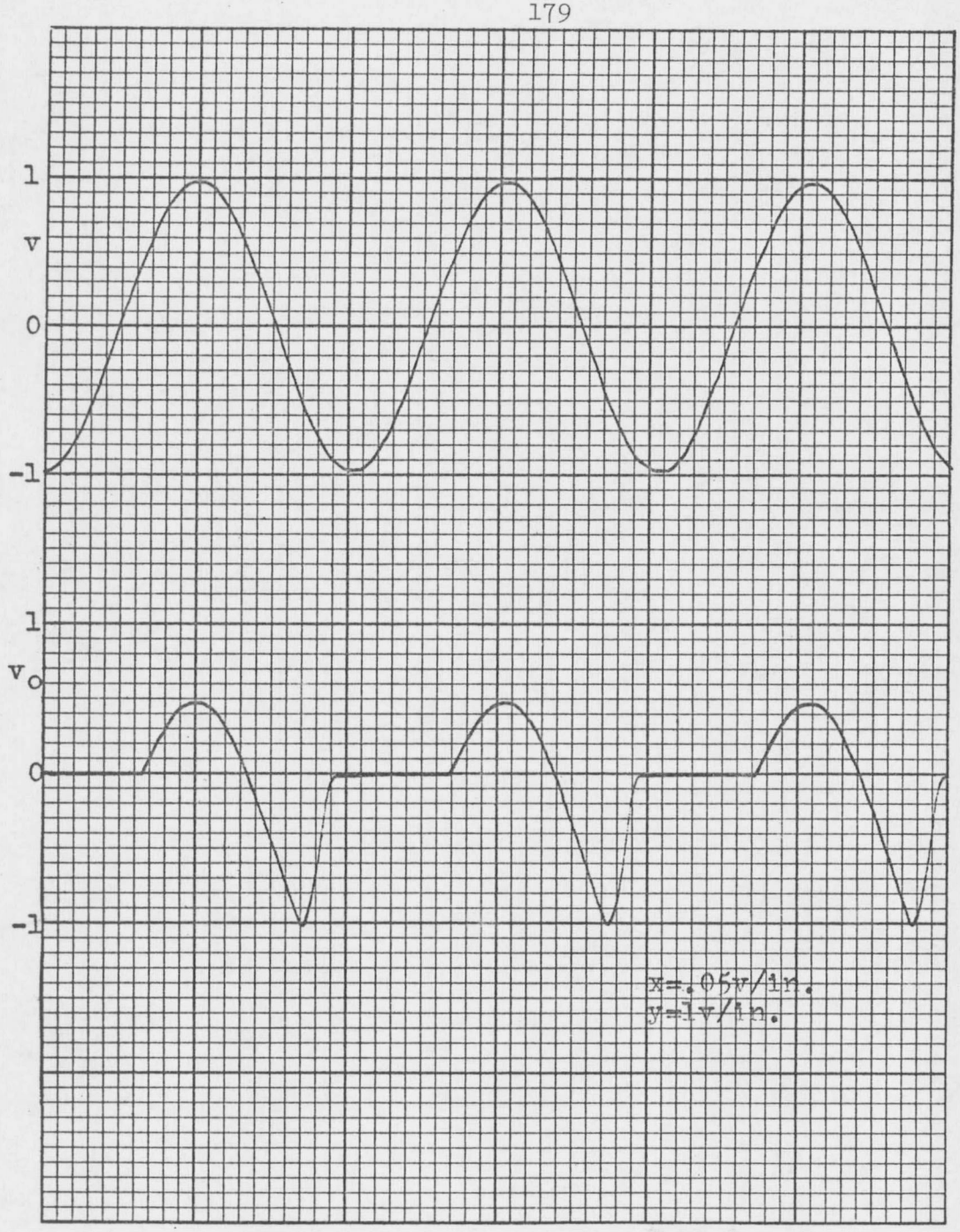


Fig. F-3 SIMULATED DIODE CHARACTERISTICS.

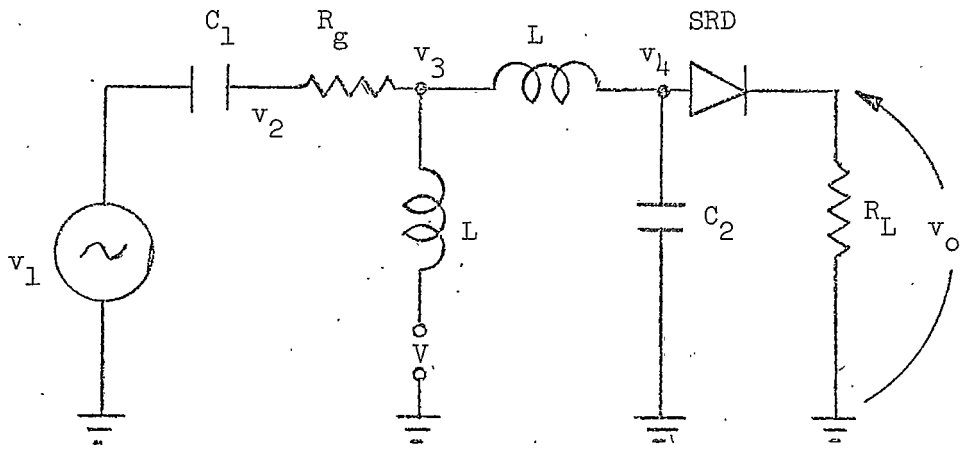


Fig. F-4. SRD DIVIDER EQUIVALENT CIRCUIT FOR SIMULATION.

The equivalent circuit of the divider is shown in Fig. F-4. The node analysis of this circuit yields the following set of equations:

$$(v_1-v_2)' C_1 = \frac{(v_2-v_3)}{R_g}$$

$$\frac{(v_2-v_3)}{R_g} = \frac{1}{L}\int v_3 dt + \frac{1}{L}\int (v_3 - v_4)\, dt$$

$$\frac{1}{L}\int (v_3-v_4)\, dt = C_2 v_4' + id. \qquad \text{(F-1)}$$

Rearranging (F-1) gives

$$v_2' = v_1' - \frac{v_2}{R_g C_1} + \frac{v_3}{R_g C_1}$$

$$v_3 = v_2 - \frac{2R_g}{L}\int v_3 dt + \frac{R_g}{L}\int v_4 dt$$

$$v_4' = \frac{1}{LC_2}\int v_3 dt - \frac{1}{LC_2}\int v_4 dt - \frac{id}{C_2} . \qquad \text{(F-2)}$$

The values to be used for simulation are

$R_L = 50$

$R_g = 50$

$L = .012\mu h$

$C_1 = 4.5pf$

$C_2 = 2.0pf$ (assumed stray capacity).

Using these values and time scaling $T = 10^{10}$ t equations (F-2) become

$$v_2' = v_1' - .444v_2 + .444v_3$$
$$v_3' = v_2 - .833\int v_3 dt + .417\int v_4 dt$$
$$v_4' = .417\int v_3 dt - .417\int v_4 dt - 50\, i_d \qquad \text{(F-3)}$$

Equations (F-3) were used in the analog simulation of the divider. The block diagram and computer connection scheme is presented in Fig. F-5.

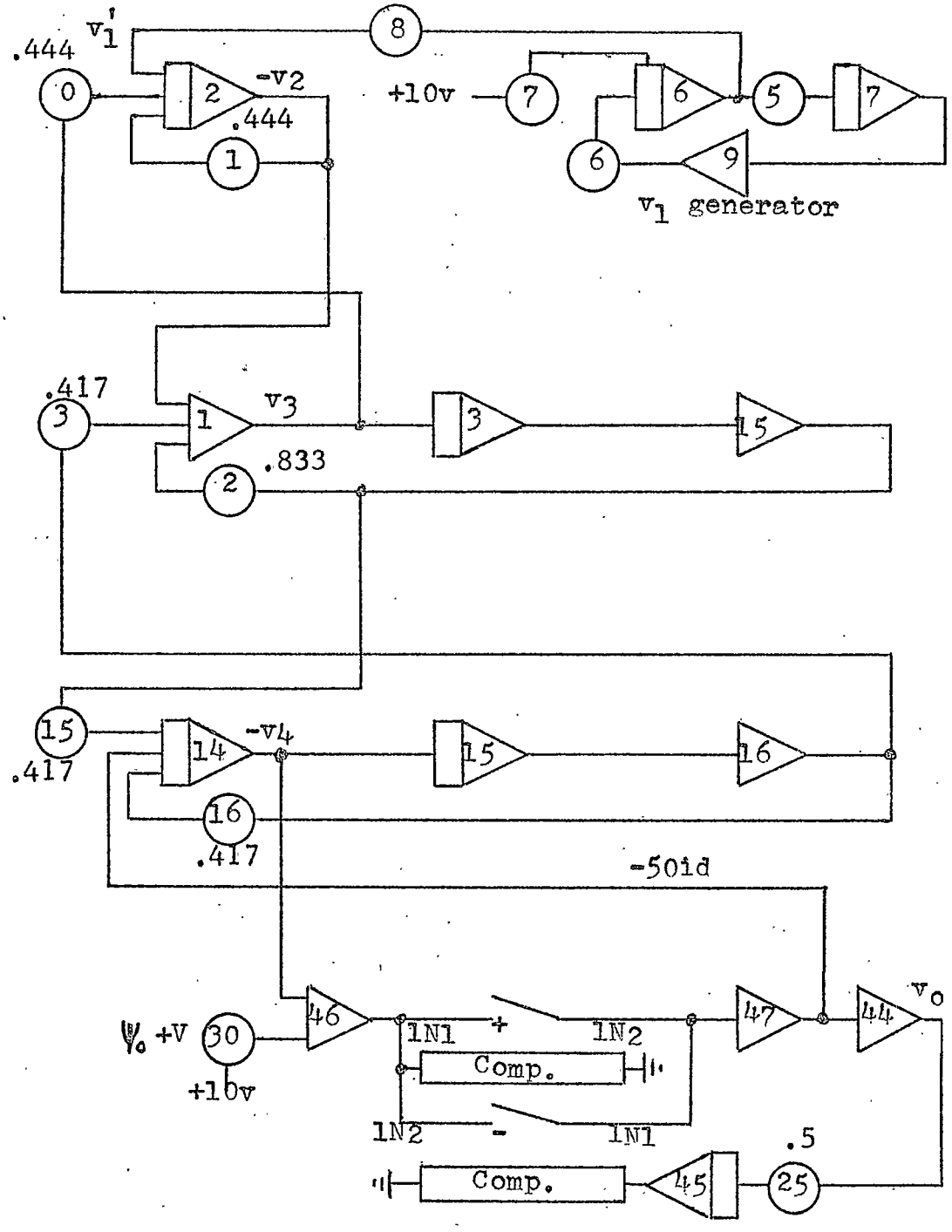


Fig. F-5 BLOCK DIAGRAM OF BROADBAND DIVIDER SIMULATION.

APPENDIX G

BALANCED MODULATOR ANALYSIS

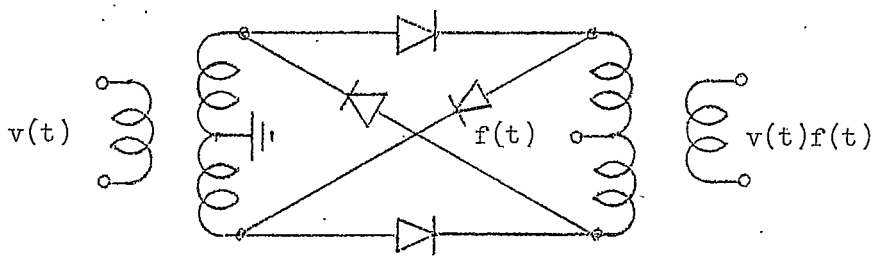


Fig. G-1. DOUBLE BALANCED RING MODULATOR.

A switching function, f(t), as represented in Fig. G-2 is assumed to calculate the minimum conversion loss of the type of modulator shown in Fig. G-1 with ideal rectifier diodes.

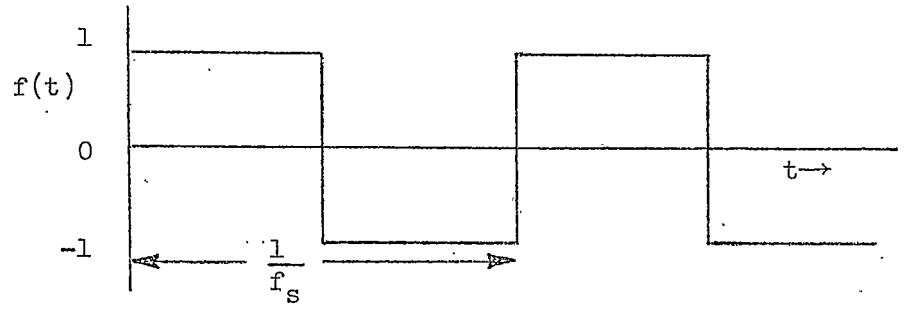


Fig. G-2. SWITCHING FUNCTION f(t)

The Fourier series for f(t) is

$$f(t) = \frac{4}{\pi}\left[\sin \omega_s t + \frac{1}{3}\sin 3\omega_s t + \ldots\right], \qquad \text{(G-1)}$$

where $b_n = \frac{4}{\pi n}$ for n odd.

For an input of $v(t) = A \sin \omega_o t$ the output, $e_o = v(t)\, f(t)$, is expressed as

$$e_o = \frac{4A}{\pi} \left[\sin \omega_o t \sin \omega_s t + \sin \omega_o t \frac{\sin 3\, \omega_s t}{3} + \sin \omega_o t \frac{\sin 5\, \omega_s t}{5} + \ldots \right] \qquad (G\text{-}2)$$

$$= \frac{4A}{\pi} \left[\frac{\cos (\omega_s - \omega_o)t}{2} - \frac{\cos (\omega_s + \omega_o)t}{2} + \frac{\cos (3\omega_s - \omega_o)t}{6} - \frac{\cos (3\omega_s + \omega_o)t}{6} + \ldots \right] \qquad (G\text{-}3)$$

The amplitude of the sum and difference frequency terms, $\omega_s - \omega_o$ and $\omega_s + \omega_o$, are the only coefficients pertinent to the conversion loss calculation.

The conversion loss (in db) at either the sum or difference frequency is given by

$$P_L = 20 \log \frac{A}{(2A)/\pi} = 20 \log \frac{\pi}{2} = 3.92 \text{ db.} \qquad (G\text{-}4)$$

APPENDIX H

DIGITAL COMPUTER PROGRAM LISTINGS

```
C       CLIPPED SINE WAVE ANALYSIS
        X=50.0*3.1416/180.0
        DO 40 MM=1,40
        M=1
        PRINT 100
  100   FORMAT(1H1,32H FOURIER COEF. CLIPPED SINE WAVE)
        PRINT 101,X
  101   FORMAT(1HO,3X,38 X=,2X,F10.6)
        PRINT 102
  102   FORMAT(1HO,3X,38  N,8X,3H VN)
        AX=2.0*X
        A11=(X+((SINF(AX))/2.0)-((SINF(X))*(COSF(X))*2.0))/3.1416
        PRINT 104,M,A11
  104   FORMAT(1H ,5X,13,3X,E10.4)
        DO 20 N=2,20
        B1=N-1
        B2=N+1
        B3=N
        B1X=B1*X
        B2X=B2*X
        B3X=B3*X
```

```
      A1=(SINF(B1))/B1
      A2=(SINF(B2X))/B2
      A3(2.0*((SINF(23X))*(COSF( X ))))/B3
      AN=(A1+A2-A3)/3.1416
      ANL=ABSF(AN)
      ANDB=20.0*(0.43429)*(LOGF(ANL))
      PRINT 103,N,AN,1NDB
  103 FORMAT(1H ,5X,13,3X,E10.4,3X,F10.4)
   20 CONTINUE
      X=X+(1.0*3.1416)/180.0
   40 CONTINUE
      CALL EXIT
      END
C     NONLINEAR CAPACITOR ANALYSIS
   10 READ 1, THETA, PHI,I
    1 FORMAT(2F10.4,13)
      PRINT 100
  100 FORMAT(1H1,3X,28H NONLINEAR CAP FOURIER COEF.)
      PRINT 10
  101 FORMAT(1HO,3X,2H N,8X,3H VN)
      M=1
      X=THETA*3.1416/180.0
      Y=PHI*3.1416/18.0
```

```
      X2=2.0*X
      Y2=2.0*Y
      A11=(0.5*Y)+(0.25*SINF(Y2))-(COSF(X)*SINF(Y))
      A12=(0.5*X)+(0.25*SINF(X2))-(COSF(X)*SINF(X))
      A1=(A11+A12)/3.1416
      B11=-(0.25*COSF-Y2))+(COSF(X)*COSF(Y))
      B12=-(COSF(X)*COSF(X))+(0.25*COSF(X2))
      B1=(B11+B12)/3.1416
      AB=(A1*A1)+(B1*B1)
      F1=SQRTF(AB)
      F1DB=20.0*(0.43429)*(LOGF(F1))
      PRINT 105,M,F1,F1DB
  105 FORMAT(1H ,3X,I2,4X,E10.4,3X,F10.4)
      DO 40 N=2,25
      B=N-1
      BB=N+1
      BBB=N
      XB=X*B
      XBB=X*BB
      XBBB=X*BBB
      YB=Y*B
      YBB=Y*BB
      YBBB=Y*BBB
```

```
      AN1=((SINF(YB))+(SINF(XB)))/(2.0*B)
      AN2=((SINF(YBB))+(SINF(XBB)))/(2.0*BB)
      AN3=-((COSF(X)*2INF(YBBB))+(COSF(X)*SINF(XBBB)))/BBB
      AN=(AN1+AN2+AN3)/3.1416
      BN1=(-(COSF(YB))+(COSF(XB)))/2.0*B)
      BN2=(-(COSF(YBB))+(COSF(XBB)))/(2.0*BB)
      BN3=((COSF(X)*COSF(YBBB))-(COSF(X)*COSF(XBBB)))/BBB
      BN=(BN1+BN2+BN3)/3.1416
      ABN=(AN*AN)+(BN*BN)
      FN=SQRTF(ABN)
      FNDB=20.0*(0.43429)*(LOGF(FN))
      PRINT 106,N,FN,FNDB
  106 FORMAT(1H ,3X,I2,4X,E10.4,3X,F10.4)
   40 CONTINUE
      IF(I) 10,10,300
  300 CALL EXIT
      END
C     THETA AND PHI FCNS OF WT= 1.0, TO 1,000,000
      W1T=1.0
      DO 10 I=1,7
      PRINT 100, W1T
  100 FORMAT(1H1,3X,5H WT =,2X,E10.4)
      PRINT 101
```

```
101 FORMAT(1HO,2X,4H PHI,6X,6H THETA)
    X=5.0*3.1416/180.0
    DO 20 N=1,72
    XW=-X/W1T
    VN=SINF(X)-W1T*COSF(X)+W1T*(2.71828**(XW))
    VD=-W1T*SINF(X)-COSF(X)-W1T*W1T*(2.71828**(XW))+W1T*W1T+1.0
    V=VN/VD
    THETA=ATANF(V)
    X1=X*180.0/3.1416
    THET1=THETA*180.0/3.1416
    PRINT 102,X,THETA,X1,THET1
102 FORMAT(2E10.4,2E10.4)
    PUNCH 103, X,THETA
103 FORMAT(2E10.4)
    X=X+5.0*3.1416/180.0
 20 CONTINUE
    Y=I
    W1T=10.0**Y
 10 CONTINUE
    CALL EXIT
    END
```

```
C     THETA AND PHI FCNS OF WT= .1, .3, 3
      W1T=0.1
      DO 10 I=1,3
      PRINT 100, W1T
  100 FORMAT(1H1,3X,5H WT =,2X,E10.4)
      PRINT 101
  101 FORMAT(1HO,2X,4H PHI,6X,6H THETA)
      X=5.0*3.1416/180.0
      DO 20 N=1,72
      XW=-X/W1T
      VN=SINF(X)-W1T*COSF(X)+W1T*(2.71828**(XW))
      VD=-W1T*SINF(X)+COSF(X)-W1T*W1T*(2.71828**(XW)) W1T*W1T+1.0
      V=VN/VD
      THETA=ATANF(V)
      X1=X*180.0/3.1416
      THET1=THETA*180.0/3.1416
      PRINT 102,X,THETA,X1,THET1
  102 FORMAT(2E10.4,2E10.4)
      PUNCH 103, X,THETA
  103 FORMAT(2E10.4)
      X=X+5.0*3.1416/180.0
   20 CONTINUE
      Y=I
```

```
      W1T=3.0*W1T+(Y-1.0)*2.1
   10 CONTINUE
      CALL EXIT
      END
C     FOURIER COEF  VAR  WT
  370 PRINT 101
  101 FORMAT(1H1,21H FOURIER COEF. VAR WT)
      READ 90,WT
   90 FORMAT(F10.1)
      PRINT 91,WT
   91 FORMAT(1HO,3X,5H WT =,F10.1)
   70 READ 10,PHI,THETA,NN,NEND
   10 FORMAT(2E10.4,I2,I2)
      PHI1=PHI*180.0/3.1416
      THET1= THETA*180.0/3.1416
      PRINT 102
  102 FORMAT(1HO,2X,4H PHI,6X,6H THETA)
      PRINT 103,PHI,THETA,PHI1,THET1
  103 FORMAT(2E10.4,2F10.4)
      PRINT 125
  125 FORMAT(1HO,3X,2H N,8X,3H VN)
      X=PHI+THETA
      Y=2.0*X
```

```
      VA1=(SINF(X)-SINF(THETA))*(SINF(X)-SINF(THETA))/6.2832
      VB1=(PHI-(SINF(Y)/2.0)+2.0*(SINF(THETA*COSF(X)))
      VB2=-SINF(THETA)*COSF(THETA)
      VB3=(VB1+VB2)/6.2832
      VAB=(VA1*VA1)+(VB3*VB3)
      V11-SQRTF(VAB)
      V11DB=20.0*0.43429*LOGF(V11)
      PRINT 111,V11,V11DB
  111 FORMAT(1HO,3X,28 1,5X,E10.4,3X,F10.4)
      DO 50 N=2,20
      A=N
      TN=THETA*A
      TN1=THETA*(A+1.0)
      TN2=THETA*(A-1.0)
      PTN=X*A
      PTN1=X*(A+1.0)
      PTN2=X*(A-1.0)
      A1=(COSF(PTN2)-COSF(TN2))/(A-1.0)
      A2=(COSF(PTN1)+COSF(TN1))/(A+1.0)
      A3=-2.0*(SINF(THETA)*SINF(PTN)-SINF(THETA)*SINF(TN))/A
      AN=(A1+A2+A3)/6=2832
      B1=(SINF(PTN2)-SINF(TN2))/(A-1.0)
      B2=-(SINF(PTN1) SINF(TN1))/(A+1.0)
```

```
      B3=2.0*(SINF(THETA)*COSF(PTN)-SINF(THETA)*COSF(TN))/A
      BN=(B1+B2+B3)/6=2832
      V=(AN*AN)+(BN*BN)
      CN=SQRTF(V)
      CNDB=20.0*0.43429*LOGF(CN)
      PRINT 110,N,CN,CNDB
  110 FORMAT(1H ,3X,I2,5X,E10.4,3X,F10.4)
   50 CONTINUE
      IF(NEND) 71,71,370
   71 IF(NN) 70,70,30
  300 CALL EXIT
      END
C     PULSE HARMONIC GENERATOR
      Q=0.1
      PHI=(5.0*3.1416)/180.0
      DO 11 I=1,16
      PRINT 100
  100 FORMAT(1H1,5X,38  Q,11X,4H PHI,9X,4H THE,9X,4H XI0,
     1 9X,5H XI02,9X,3H PL)
      DO 10 J=1,70
      PHIQ=PHI/Q
      TN1=(Q*Q)*(1.0-2.71828**(-PHIQ))
      TN2=1.0-COSF(PHI)-Q*(SINF(PHI)
```

```
      TD1=Q*TN1+Q-Q*COSF(PHI)
      TD2=SINF(PHI)-(1.0+Q*Q)*PHI
      TND=(TN1+TN2)/3D1+TD2)
      THE=ATANF(TND)
      XI1=(Q*COSF(THE)-Q*Q*SINF(THE))/(1.0+Q*Q)
      XI2=(SINF(PHI-THE)-Q*COSF(PHI-THE))/(1.0_Q*Q)
      XI0=XI1*(2.71828**(-PHIQ))+SINF(THE)+XI2
      XI02=XI0*XI0
      PL1=(2.0*XI02*Q)/3.1416
      PL=-10.0*(0.43429)*(LOGF(PL1))
      PHA=PHI*180.0/3.1416
      THA=THE*180.0/3.1416
      PRINT 103,Q,PHA,THA,XI0,XI02,PL
  103 FORMAT(1H ,3(3X,F10.4),2(3X,E10.4),3X,F10.4)
      PUNCH 500,PL
  500 FORMAT(F10.4)
      PHI=PHI+5.0*3.1416/180.0
   10 CONTINUE
      XI=I
      IF(I-10)301,301,302
  301 Q=0.2*XI
      GO TO 305
  302 Q=5.0*(2.0**(XI-11.0))
```

```
305 PHI=(5.0*3.1416)/180.0
 11 CONTINUE
    PAUSE
    QN=0.1
    PHI=(5.0*3.1416)/180.0
    DO 13 II=1,11
    PRINT 200
200 FORMAT(1H1,5X,38  Q,11X,4H PHI,9X,4H PL)
    DO 14 JJ=1,70
    X=(1.0/QN)*(3.1416-PHI/2.0)
    XX=1.0-2.71828**(-X)
    XXX=QN*XX*XX
    PLL=1.961-10.0*(0.43429)*LOGF(XXX)
    PHA=PHI*180.0/3.1416
    PRINT 201,QN,PHA,PLL
201 FORMAT(1H ,3X,F10.4,3X,F10.4,3X,F10.4)
    PUNCH 501,PLL
501 FORMAT(F10.4)
    PHI=PHI+5.0*3.1416/180.0
 14 CONTINUE
    XII=II
    QN=0.2*XII
    PHI=5.0*3.1416/180.0
```

```
   13 CONTINUE
      CALL EXIT
      END
C     PL+PLL
      DIMENSION PLL(11,70),PL(70),S(11)
      READ 100,N
  100 FORMAT(I3)
      DO 11 I=1,11
      DO 11 J=1,70
      READ 10,PLL(I,J)
   10 FORMAT(F10.4)
      11 CONTINUE
      DO 15 IN=1,N
      DO 16 JN=1,70
      READ 20,PL(JN)
   20 FORMAT(F10.4)
   16 CONTINUE
      PRINT 300,IN
  300 FORMAT(1H1,I5)
      DO 50 IR=1,70
      DO 70 IC=1,5
      S(IC)=PL(IR)+PLL(IC,IR)
   70 CONTINUE
```

```
      PRINT 151,(S(IP),IP=1,5)
  151 FORMAT(1H ,5(5X,F10.4))
   50 CONTINUE
      PRINT 301,IN
  301 FORMAT(1H1,I5)
      DO 60 IR=1,70
      DO 80 IC=6,11
      S(IC)=PL(IR)+PLL(IC,IR)
   80 CONTINUE
      PRINT 152,(S(IP),IP=6,11)
  152 FORMAT(1H ,6(5X,F10.4)
   60 CONTINUE
   15 CONTINUE
      CALL EXIT
      END
```

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