

PROCESS VOLTAGE TEMPERATURE COMPENSATED ON-CHIP CMOS ACTIVE
INDUCTORS FOR WILKINSON POWER DIVIDING APPLICATIONS

By

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TABLE OF CONTENTS

1. INTRODUCTION TO THE USE OF CMOS ACTIVE INDUCTORS IN AN RFIC APPLICATION	1
Introduction	1
Non-Idealities in Lumped Components	2
Distributed Versus Lumped Wilkinson Power Divider/Combiner	3
The Effect of Non-Idealities in the Lumped Wilkinson.....	5
Background	9
Actively Compensated Spiral Inductors.....	9
Active Inductor Circuits in RFIC Applications.....	12
Simple Cascoded Active Inductor	13
Basic SCAI Operation.....	15
The SCAI Transfer Function	16
CPLL SCAI Compensation Scheme:.....	21
The Regulated Active Inductor.....	25
Thesis Overview	27
2. BOBCAT_V0 HARDWARE MEASUREMENTS, PERFORMANCE AND MODEL TO HARDWARE CORRELATION	29
Introduction	29
Design Implementation Strategy	31
Hardware Measurements and Results.....	33
Test Setup	33
Critical Passive/Active Device Characterization	34
SCAI Characterization	50
Wilkinson Characterization	55
Hardware Based Conclusions.....	64
3. ACTIVE INDUCTOR/WILKINSON COMPENSATION SCHEME	65
Introduction	65
The Wilkinson Design Point	65
Optimizing the Control Loop Architecture	65
Avoiding Prior Issues with Control Systems	65
Minimizing Systematic Offsets Between Master & Slave Elements	66
Selecting the Measured Variable	67
The Wilkinson Phase Lock Loop	71

TABLE OF CONTENTS - CONTINUED

Using a Delay Lock Loop for a Phase/Time Reference.....	74
The Digital Phase Detector:.....	82
The Charge Pump:	86
The Loop Filter	89
DLL Transfer Function	90
System Level Considerations	92
Simultaneous Switching	92
Stability Analysis	96
The Master $\frac{1}{2}$ Wilkinson & 3dB Attenuator	99
The Operational Amplifier	103
The WPLL 3ns Slave Delay Line	105
The WPLL Frequency Divider	107
The WPLL Phase Detector.....	107
The WPLL Charge Pump.....	108
The WPLL Loop Filter.....	108
WPLL Transfer Function	109
System Level Considerations	110
WPLL & DLL Control System Analysis	110
$\frac{1}{2}$ Wilkinson Static Phase Variation	114
WPLL Loop Stability.....	115
Slave Performance	117
SCAI.....	118
Wilkinson	121
Wilkinson Stability Analysis	127
Wilkinson Input Power Limitations For A Compensated Wilkinson	131
Current Consumption.....	133
Physical Size.....	134
 4. CONCLUSION AND SUGGESTED FUTURE RESEARCH	 136
Summary	136
Potential Improvements to the Existing WPLL Compensation Scheme	139
Supporting Industry Standard PVT Specifications	140
Characterizing the Effect of Device-to-Device and Across Chip Variation	142
The SCAI and Noise	142
Power Supply Rejection Ration (PSRR).....	143
Improved WPLL Operational Amplifier.....	143

TABLE OF CONTENTS - CONTINUED

DLL & WPLL Lock Signals, Initialization and Reset Circuitry	143
WPLL Reference Signals	145
The DLL Reference Signal	145
The Master Wilkinson Reference Signal	145
Recommendations for Future work	146
The Modified Regulated AI & Compensation Scheme	146
REFERENCES CITED	147

LIST OF TABLES

Table	Page
1.1	Effects of inductor non-ideality on each S-Parameter 9
1.2	Inductance and Q Factor of SCAI over Process 16
2.1	Process Voltage Temperature Bounding Corners used in Simulation 32
2.2	Temperature Coefficients for C5 Polysilcon Resistor 43
2.3	Predicted vs Simulated Resistance for BobcatV0 50 Ω Resistor Experiment.....43
3.1	Gain Term Conversion Chart 112
3.2	DC Power For the WPLL Simple Cascoded Active Inductor Compensation Scheme 133
3.3	WPLL Area Breakdown.....134
4.1	Summary and Comparison of Uncontrolled and Controlled SCAI and Lumped Wilkinson 138

LIST OF FIGURES

Figure		Page
1.1	Distributed Wilkinson power divider/combiner topology	3
1.2	Lumped Wilkinson power divider/combiner topology	4
1.3	Wilkinson Reflection coefficient (S_{11}) for various values of Q_L	6
1.4	Wilkinson Transmission coefficient (S_{21}) for various values of Q_L	6
1.5	Wilkinson Isolation (S_{32}) for various values of Q_L	7
1.6	Wilkinson Reflection Coefficient (S_{11}) for various inductance values assuming a $Q_L = 50$	7
1.7	Wilkinson Isolation Coefficient (S_{21}) for various inductance values assuming $Q_L=50$	8
1.8	Wilkinson Reflection Coefficient (S_{32}) for various inductance values assuming $Q_L=50$	8
1.9	Active Magnetic Energy Recovery	10
1.10	Boot Strapped Inductor	11
1.11	Current Mirror Compensated Spiral Inductor	12
1.12	Simple Cascoded Inductor (SCAI) Schematic	14
1.13	Lu's Lumped SCAI Model.....	17
1.14	Small Signal Model Used to Derive SCAI Transfer Function.....	18
1.15	Comparison of SCAI Models for Predicting Series Resistance	19
1.16	Comparison of SCAI Models for Predicting Inductance	20
1.17	SCAI Inductance (L) & Resistance (R) Vs I_1 Bias Current at 250MHz.....	21
1.18	Lyson's CPPL based AI Compensation Scheme.....	22
1.19	Colpitt's VCO w/AI.....	23
1.20	Regulated Active Inductor.....	25
1.21	Enhanced Regulated AI.....	26
2.1	Bobcat_V0 Test-Chip.....	29
2.2	Basic VLSI Design Flow.....	31
2.3	MSU IC Testing Facility	33
2.4	Bobcat_V0 Floating Short Experiment.....	35
2.5	Bobcat_V0 Short Experiment Results	36
2.6	Bobcat_V0 Open Experiment.....	37
2.7	Bobcat_V0 Open Experiment Results	38
2.8	Bobcat_V0 Thru Experiment.....	39
2.9	Bobcat_V0 Thru Experiment Results	40
2.10	Bobcat_V0 50 Ω Polysilicon Resistor Experiment	41
2.11	Bobcat_V0 50 Ω Experiment Results	42
2.12	Bobcat_V0 Open, Short, Thru Experiment Results.....	44

LIST OF FIGURES – CONTINUED

Figure		Page
2.13	Bobcat_V0 9pF Distributed Capacitor.....	45
2.14	Bobcat_V0 9pF Distributed Capacitor Experiment Results	46
2.15	Bobcat_V0 9pF Lumped Capacitor Experiment	47
2.16	Bobcat_V0 9pF Lumped Capacitor Experiment Results	48
2.17	Bobcat_V0 Lumped Vs Distributed Capacitor Results	49
2.18	Bobcat_V0 SCAI Experiment One.....	50
2.19	Bobcat_V0 SCAI Experiment One Inductance Vs Frequency	51
2.20	Bobcat_V0 SCAI Experiment One Resistance Vs Frequency	52
2.21	Bobcat_V0 SCAI Experiment Two Inductance (L) and Resistance (R) Vs Frequency	53
2.22	Bobcat_V0 SCAI Experiment 2 Inductance and Resistance Vs Frequency.....	54
2.23	Bobcat_V0 250MHz Lumped Wilkinson Experiment.....	55
2.24	Bobcat_V0 Wilkinson Experiment 1 S_{11} Vs Frequency	56
2.25	Bobcat_V0 Wilkinson Experiment 1 S_{32} Vs Frequency	57
2.26	Bobcat_V0 Wilkinson Experiment 1 S_{21} Vs Frequency	58
2.27	Bobcat_V0 Lumped Wilkinson Experiment S_{21} Vs Input signal strength @ 250MHz.....	59
2.28	Bobcat_V0 Lumped Wilkinson Experiment S_{32} Vs Input signal strength @ 250MHz.....	59
2.29	Test Setup Used To Characterize 2-Tone Intermodulation Induced Distortion	60
2.30	Wilkinson Primary and 3 rd Harmonic Vs Input Power	61
2.31	Bobcat_V0 Wilkinson Experiment S_{21} Transmission Coefficient Vs Supply Voltage @ 250MHz.....	63
2.32	Bobcat_V0 Wilkinson Experiment S_{32} Isolation Coefficient Vs Supply Voltage @ 250MHz.....	63
3.1	Ideal, Lumped 250MHz Wilkinson in a 50 Ω System.....	65
3.2	SCAI Control System Diagram	67
3.3	Ideal Lumped Wilkinson Signal Phase and Magnitude Vs Inductance at 250MHz	69
3.4	Ideal Lumped Wilkinson Signal Phase and Magnitude Vs Inductor Resistance at 250MHz.....	70
3.5	WPLL Schematic Flow Chart.....	71
3.6	Delay Lock Loop Control System Diagram.....	74
3.7	High Level Delay Lock Loop Schematic.....	75
3.8	DLL Delay Buffer Schematic.....	76

LIST OF FIGURES – CONTINUED

Figure	Page
3.9	1 st Order CSI Model.....78
3.10	Delay of Two Series CSI Vs Control Voltage.....80
3.11	Digital Phase Detector Logic Block 82
3.12	Phase Detector Input and Output Signals.....84
3.13	Phase Detector Error Signal and Offset 85
3.14	Charge Pump Schematic 86
3.15	Charge Pump Transfer Function.....88
3.16	Charge Pump Range.....89
3.17	DLL Transfer Function at 100MHz for various changes in DLL_PBIAS 91
3.18	Unity Gain Buffer 92
3.19	DLL Phase Error and Steady State Control Voltage 93
3.20	Total DLL Phase Error.....95
3.21	DLL Step Response 97
3.22	Original and Modified DLL response for WCP, 15°C, V _{DD} = 5.05V 98
3.23	WPLL Driving Network.....99
3.24	Master ½ Wilkinson Schematic.....100
3.25	Master ½ Wilkinson & 3dB Schematic.....101
3.26	Master Wilkinson Phase Vs Control Voltage.....102
3.27	Master ½ Wilkinson & 3dB Schematic.....103
3.28	Total 3ns DL Phase Error.....106
3.29	Frequency Divide by Four w/Reset Digital Logic Block.....107
3.30	H _{WPLL} (250MHz) Vs ΔWPLL_CNTL 109
3.31	WPLL & DLL Control System Diagram 111
3.32	½ Wilkinson Phase Variation 114
3.33	WPLL Step Response 115
3.34	Original and Modified WPLL response for WCP, 15°C, V _{DD} = 5.05V 116
3.35	Inductance at 250MHz for a Compensated SCAI in the Time Domain 118
3.36	Inductance for Compensated & Uncompensated SCAI in the Frequency Domain 119
3.37	Resistance for the Compensated SCAI in the Frequency Domain 120
3.38	S ₂₁ at 250MHz for a Compensated Wilkinson in the Time Domain 121
3.39	S ₂₁ for a Compensated & Uncompensated Wilkinson in the Frequency Domain 122
3.40	∠ S ₂₁ at 250MHz for a Compensated Wilkinson in the Time Domain 123

LIST OF FIGURES – CONTINUED

Figure	Page
3.41 $\angle S_{21}$ for Compensated & Uncompensated Wilkinson in the Frequency Domain	124
3.42 $ S_{32} $ at 250MHz for a Compensated Wilkinson in the Time Domain	125
3.43 S_{32} for Compensated & Uncompensated Wilkinson in the Frequency Domain.....	126
3.44 S_{11} for Compensated & Uncompensated Wilkinson in the Frequency Domain.....	127
3.45 Load Stability Circles for a Compensated Lumped Wilkinson at 250MHz	129
3.46 Source Stability Circles for a Compensated Lumped Wilkinson at 250MHz	130
3.47 $ S_{21} $ Transmission Coefficient Vs Input Signal Magnitude for a Slave Wilkinson at 250MHz	131
3.48 $ S_{32} $ Isolation Coefficient Vs Input Signal Magnitude for a Slave Wilkinson at 250MHz.....	132
4.1 Temperature & Voltage Conditions Where Existing SCAI Design Can Be Tuned For 45nH & $Q < 15$	141

ABSTRACT

Few academic or industry feasibility studies have been published on the implementation of Active Inductors in a standard CMOS IC process as an alternative to the physically large and typically quite lossy spiral inductors. Development efforts at the simulation level have achieved only limited success in creating an Active Inductor topology that exhibits the quality and inductive tolerance necessary for the large-scale, high-volume production common to most IC components. This thesis focuses on manufacturing and characterizing the basic component circuitry necessary for the implementation of a lumped-element Wilkinson power divider using active inductors and develops a compensation scheme to control the parameters of merit in the active inductor across a useful process, voltage and temperature operating window. Hardware results presented reinforce the need to actively compensate the Active Inductor structure implemented in a 0.6 μ m (AMIS C5) CMOS process. Simulation results presented show the benefits of a compensated Active Inductor incorporated into a typical RF network.

CHAPTER 1

INTRODUCTION TO THE USE OF CMOS ACTIVE
INDUCTORS IN AN RFIC APPLICATIONIntroduction

A significant amount of research both in industry and academia has been focused on developing a cost- and space-efficient device in a CMOS IC technology that exhibits the inductive properties necessary for many RF and analog applications. Passive spiral inductors are readily available in many CMOS IC technologies but this device suffers from a number of inadequacies including but not limited to a very large physical size and unattractive, lossy characteristics or low quality factor (Q). With each succeeding technology, CMOS devices shrink, but the physical size of spiral inductors remain essentially unchanged due to the relationship between inductance and the physical dimensions of the spiral. This implies the spiral inductor consumes a larger percentage of chip area with each succeeding technology, providing great incentive to develop an alternative. The spiral inductors available in most low cost CMOS processes lack a sufficient Q to be useful in many RF applications. Despite their inadequacies, spiral inductors are frequently used in LC tank oscillators and PLL's where the benefits of a low noise circuit far outweigh the design challenges presented by the physical size and lossy characteristics.

Non-Idealities in Lumped Components

Inherent non-idealities and variation plague every manufacturing process. In the case of IC technology, this is exacerbated by ever-decreasing device dimensions. For a given device, key process parameters such as resistance (ΔR), inductance (ΔL) and capacitance (ΔC) typically follow a Gaussian distribution for chip-to-chip as well as random variation. Variation of key environmental variables such as power supply (ΔV_{DD}) and temperature (ΔT) may not necessarily follow a Gaussian distribution but nonetheless significantly contribute to the effective tolerance range of a device or circuit. For the purpose of analog IC circuit design, the physical mechanics behind the variation of key parameters is not under the direct control of the designer. Rather the designer must compensate for these non-idealities by understanding how they affect each circuit and how to compensate and add sufficient margin during the design process.

One of the most commonly referenced figures of merit for a passive energy storage device is the quality factor (Q) which can be defined as follows.

$$Q \equiv \omega * \frac{\text{energy stored}}{\text{average power dissipated}} \quad [1.1]$$

Equation [1.1] defines the general frequency dependent equation that applies to both resonant and non-resonant circuits. The quality factor (Q) referenced at a particular target design frequency can be used to quantify the ideality of an electrical component as suggested in [1.2].

$$Q \equiv \frac{|\text{Im}[Z]|}{|\text{Re}[Z]|} \quad [1.2]$$

Distributed Versus Lumped Wilkinson Power Divider/Combiner

The never-ending demand to reduce the overall size of RF circuitry fuels the desire to combine distributed RF networks and filters with on-chip logic, but the inability to reliably manufacture quality on-chip lumped inductors has limited the achievement of this goal. The Wilkinson Power Combiner/Divider depicted in Figure 1.1 is a popular RF circuit used in a variety of signal distribution functions and historically implemented as a distributed network using $\lambda/4$ transmission lines [1]. The goal of the research presented here is to develop a robust, well-functioning Wilkinson power divider/combiner within a standard digital CMOS process.

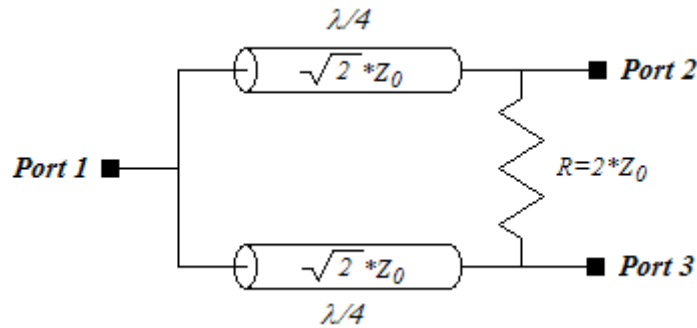


Figure 1.1: Distributed Wilkinson power divider/combiner topology

Some attractive characteristics of this 3-Port network include matching at all ports and high levels of isolation between the output ports (Ports 2 and 3 of Figure 1.1). A Wilkinson power divider/combiner can operate in two modes. An applied signal at Port1 is transmitted to Port2 and Port3 at half the power level and phase shifted 90° assuming Port2 and Port3 are terminated with the correct system impedance. Likewise, in-phase signals applied at Port 2 and Port3 are transmitted to Port1 where the power level is the sum of the two input signals and is phase shifted 90° assuming Port1 is terminated with

the correct system impedance. These characteristics are quantified by the key S-parameters, S_{11} , S_{22} , S_{33} , S_{21} , S_{31} and S_{32} .

The Wilkinson can also be realized with lumped elements as described by Lu [2] and depicted in Figure 1.2 which brings to light the possibility of implementing this network in a low-cost CMOS process. It is important to note that the lumped Wilkinson with shunt inductors and series capacitors is theoretically electrically equivalent to the $\frac{3}{4}\lambda$ rather than the standard $\frac{\lambda}{4}$ transmission line implementation, which corresponds to a 270° rather than 90° phase difference between Port1 and Port2/3.

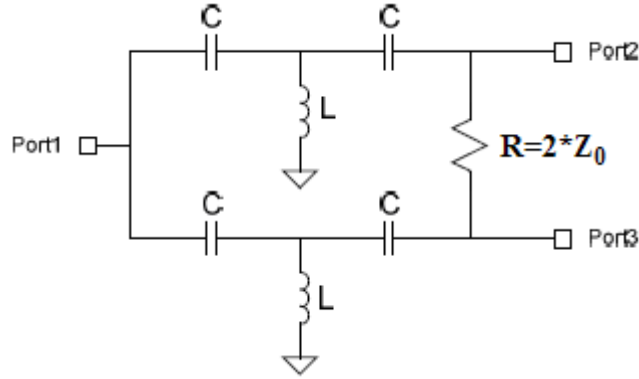


Figure 1.2: Lumped Wilkinson power divider/combiner topology

Given a system impedance Z_0 and a target frequency ω , the values of R , L and C can be calculated using the equations [1.3], [1.4] and [1.5] [2].

$$L = \frac{\sqrt{2}Z_0}{\omega} \quad [1.3]$$

$$C = \frac{1}{\sqrt{2}\omega Z_0} \quad [1.4]$$

$$R = 2 * Z_0 \quad [1.5]$$

The Effect of Non-Idealities in the Lumped Wilkinson

The implementation of an on-chip Lumped Wilkinson in a low-cost IC technology requires the availability of high quality, low tolerance capacitive and inductive components. Capacitors possessing high Q characteristics desirable for RF circuits are very common in most low-cost IC technologies however this is not true for inductors. The single greatest hurdle preventing on-chip design of the lumped Wilkinson Power Combiner/Divider and many other RF circuits is the lack of a high quality, low tolerance inductive component. To help quantify this point, Lyson [3] defined a minimum set of pass/fail criteria that can be used to determine the quality of a Wilkinson at the design frequency. Equation [1.9] below was conceived based on the research described in this thesis.

$$|S_{11}| \leq -15dB \quad [1.6]$$

$$|S_{32}| \leq -15dB \quad [1.7]$$

$$|S_{21}| \geq -3.5dB \quad [1.8]$$

$$\angle S_{21} = 270^\circ \pm 5\% \quad [1.9]$$

For the purpose of this discussion, a Lumped Wilkinson was designed with a target frequency of 250MHz using equation [1.3], [1.4] and [1.5] and assuming ideal capacitive and resistive components. The ideal values of L, C and R calculated in this manner are 45nH, 9pF and 100Ω respectively. The quality (Q) and shunt inductance (L) was varied in a number of simulations to determine the maximum allowable tolerance of L (ΔL_{MAX}) and the minimum allowable Q (Q_{LMIN}) such that the Wilkinson pass/fail criteria are satisfied.

Figure 1.3 - Figure 1.8 shows the adverse effects of L and Q variation on the performance of a lumped, 250MHz Wilkinson.

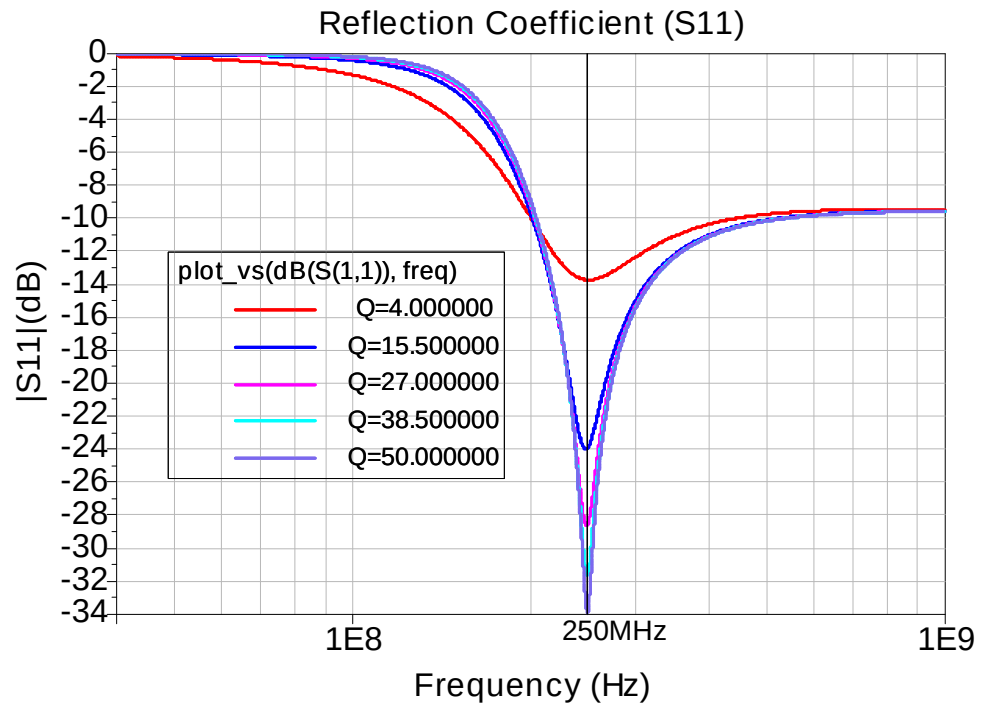


Figure 1.3: Wilkinson Reflection coefficient (S_{11}) for various values of Q_L .

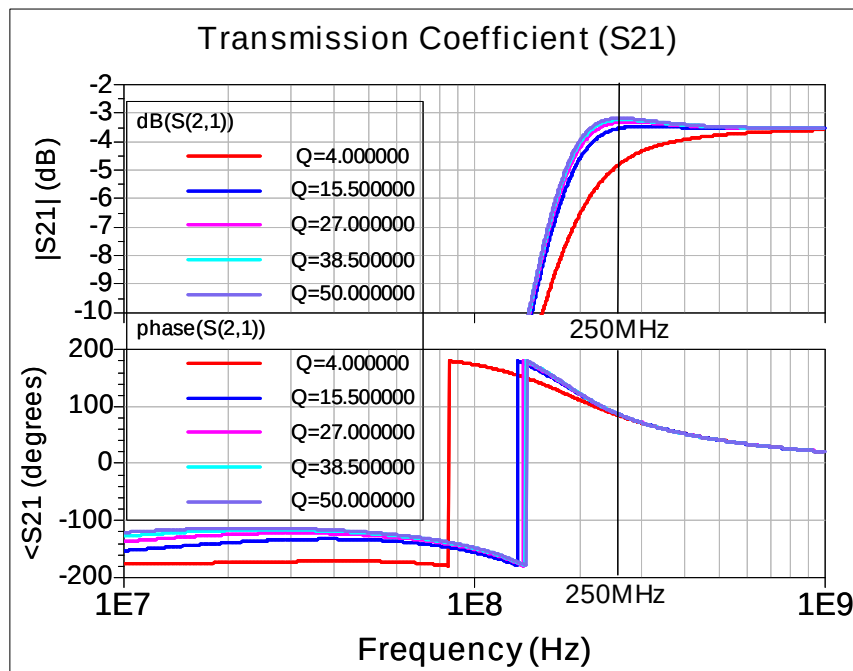


Figure 1.4: Wilkinson Transmission coefficient (S_{21}) for various values of Q_L .

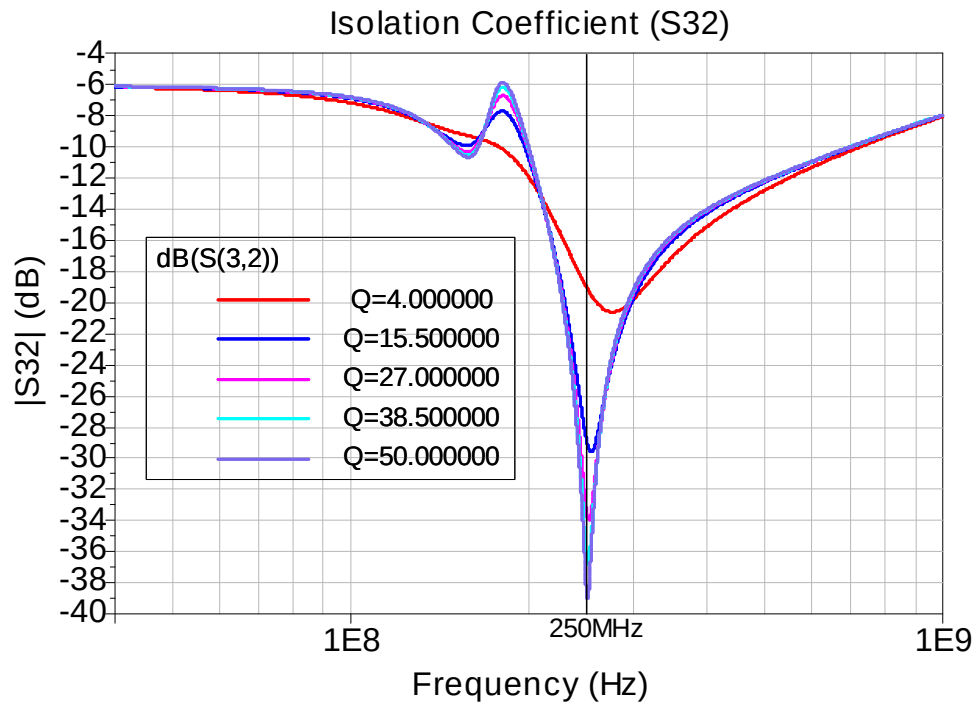


Figure 1.5: Wilkinson Isolation (S_{32}) for various values of Q_L .

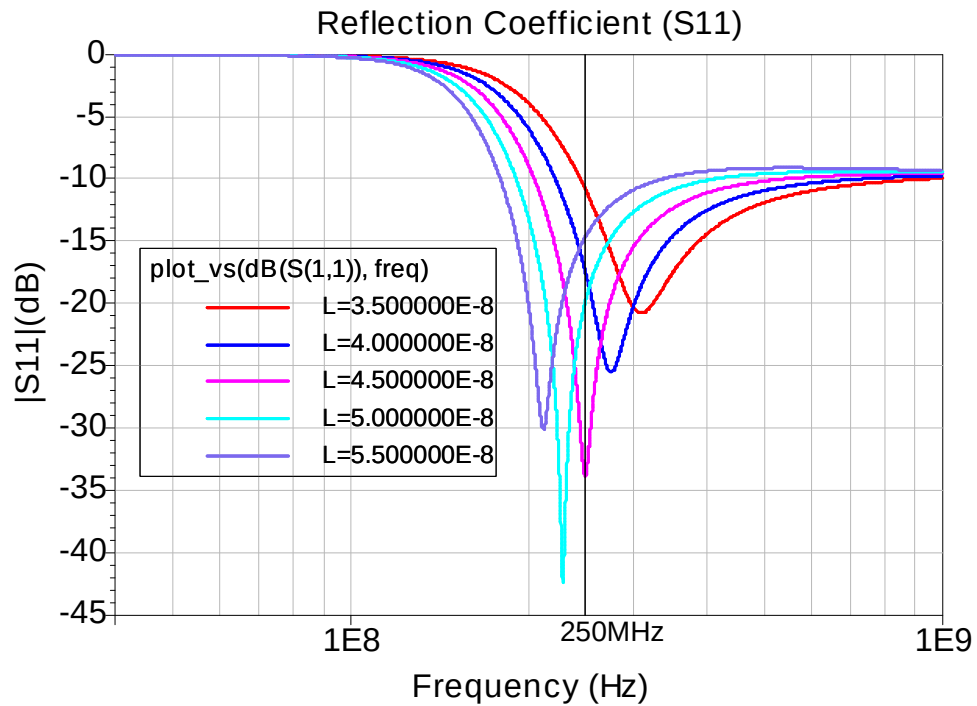


Figure 1.6 Wilkinson Reflection Coefficient (S_{11}) for various inductance values assuming a $Q_L = 50$.

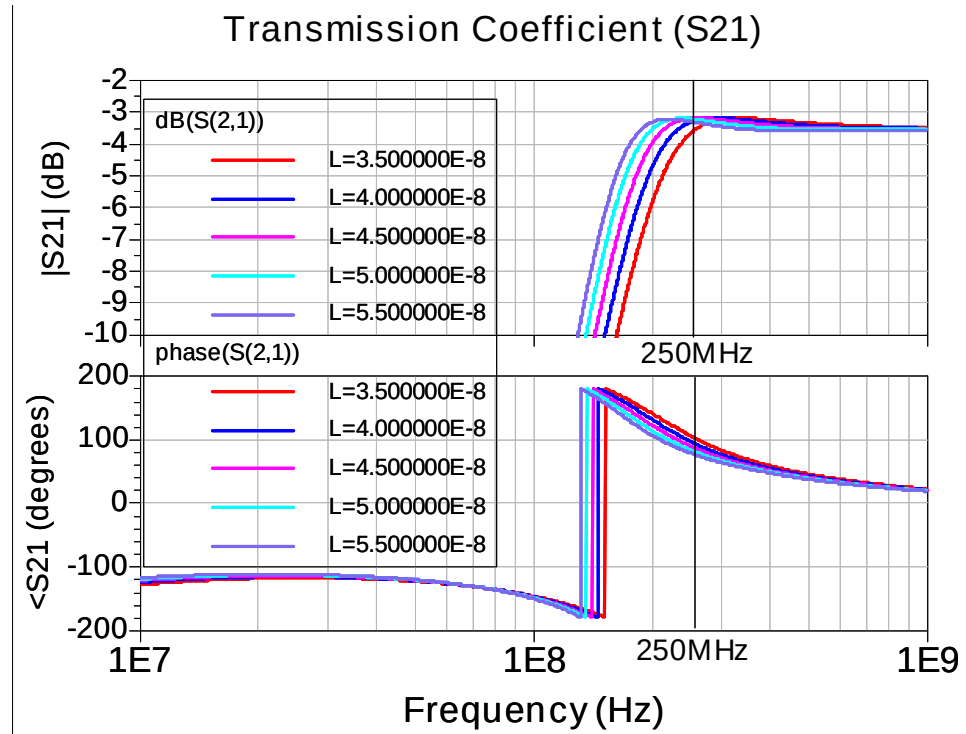


Figure 1.7: Wilkinson Isolation Coefficient (S_{21}) for various inductance values assuming $Q_L=50$.

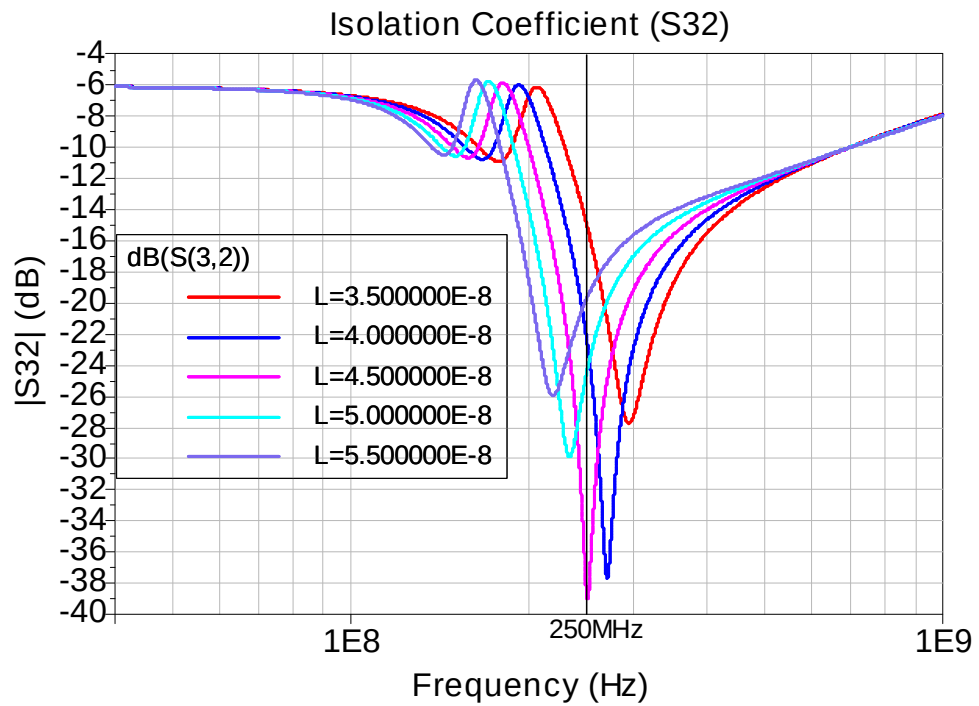


Figure 1.8: Wilkinson Reflection Coefficient (S_{32}) for various inductance values assuming $Q_L=50$.

S-Parameter	$Q_{L\text{MIN}}$	ΔL_{MAX} (nH)
$ S_{11} $ (dB)	5	39 - 54
$ S_{21} $ (dB)	15	36 - 61
$\angle S_{21}$ (°)	2	38 - 67
$ S_{32} $ (dB)	2	34 - 67

Table 1.1: Effects of inductor non-ideality on each S-Parameter

Table 1.1 summarizes these effects and identifies a $Q_{L\text{MIN}}$ and ΔL_{MAX} .

$$Q_{L\text{MIN}} = 15 \quad [1.10]$$

$$\Delta L_{\text{MAX}} = 54nH - 39nH = 46.5nH \pm 16\% \quad [1.11]$$

The technique used to determine overall $Q_{L\text{MIN}}$ and ΔL_{MAX} ignores second order effects or interaction between $Q_{L\text{MIN}}$ and ΔL_{MAX} but provides a good starting point and basic understanding of the tolerances necessary for the implementation of a lumped Wilkinson in an IC technology.

Background

Actively Compensated Spiral Inductors

One method for overcoming the inadequacies of on-chip spiral inductors is to compensate for the large effective series resistance using amplification. This technique combines the use of passive and active devices to provide an inductor suitable for RF design. A number of topologies have been developed that all work on the same principal of Active Magnetic Energy Recovery [5]. This type of compensation utilizes a

transformer constructed of on-chip spirals where the secondary coil is biased to compensate for losses in the primary coil.

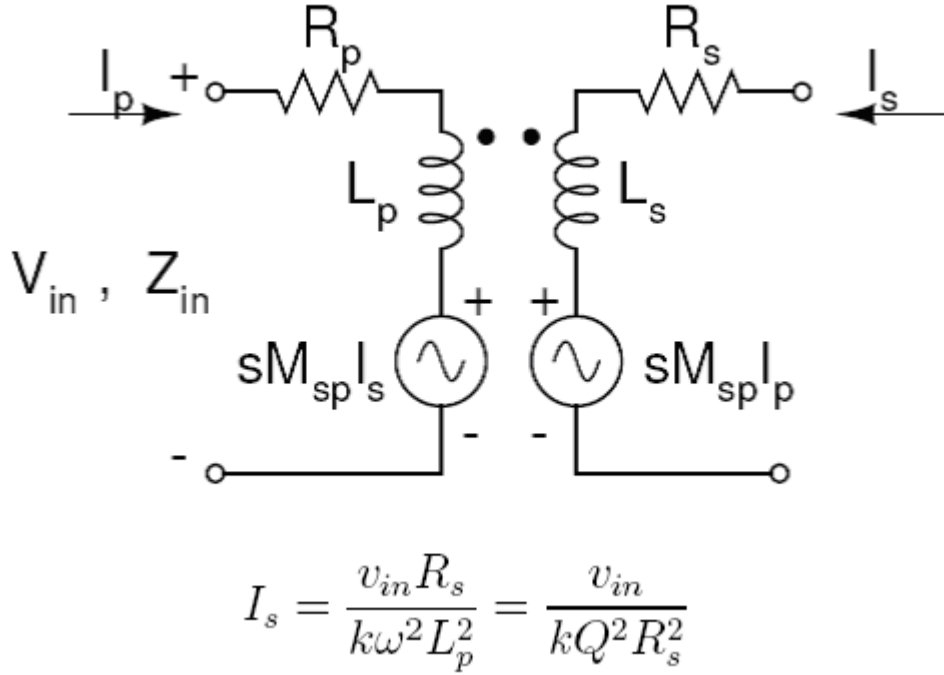
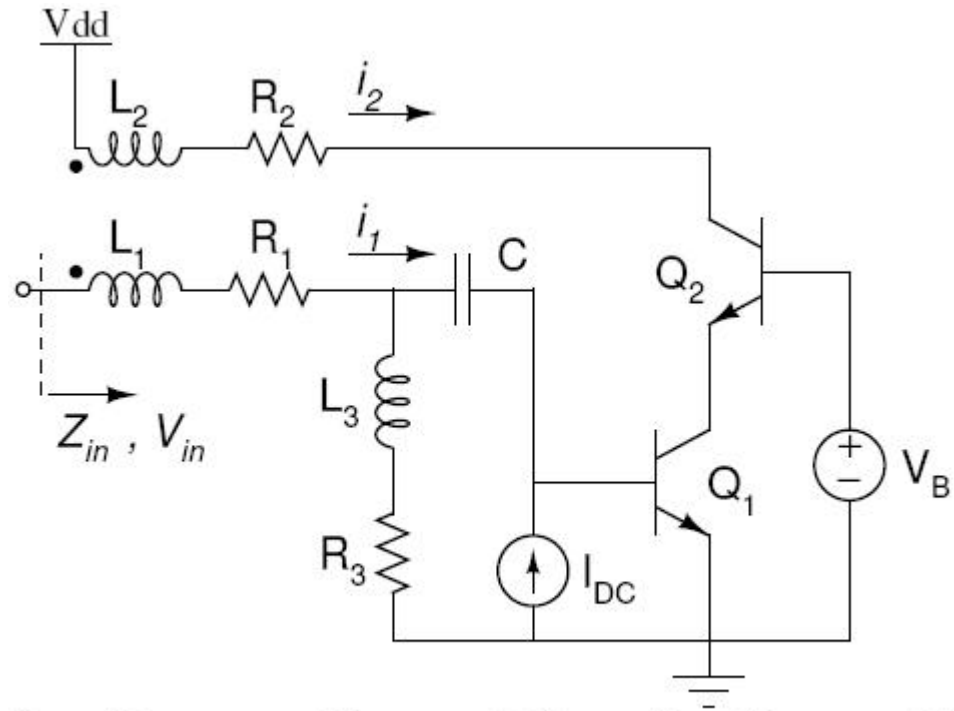


Figure 1.9: Active Magnetic Energy Recovery

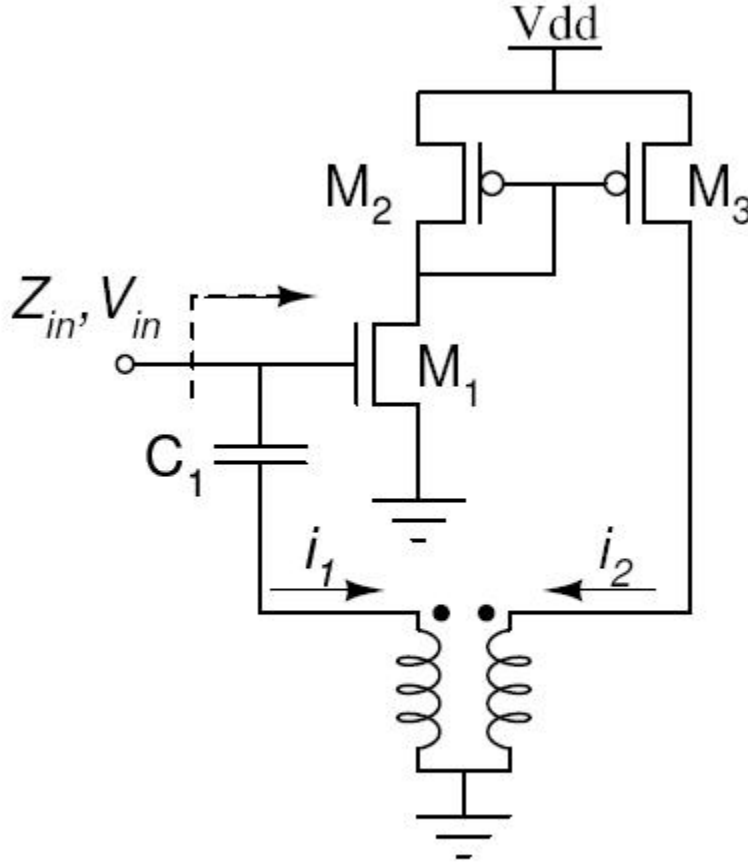
Figure 1.9 shows the circuit model and equation necessary to compensate a spiral inductor L_p with series loss R_p and quality factor Q , assuming $R_p = R_s$, $L_p = L_s$, where k is the coupling factor between the primary and secondary windings. There are a number of different methods for providing this bias current but all seek to minimize the distortion and noise contribution from active devices. This is done by minimizing the number of active devices and selectively connecting them to the spiral. Two of these topologies are reviewed here.



$$Z_{in} = [R_1 + r_{\pi} - \omega M g_m r_{\pi} \sin(\phi)] + j\omega [L_1 + M g_m r_{\pi} \cos(\phi)]$$

Figure 1.10: Boot Strapped Inductor

Figure 1.10 shows a boot strapped inductor scheme to enhance the effective Q of an on-chip spiral inductor. The equation describes the relationship between spiral and transistor device design parameters and the effective input impedance, where ϕ is the phase between i_1 and i_2 . The bias point of Q_1 and Q_2 can be used to control the inductance and effective series resistance. This topology was used to achieve a quality factor of 30 in a SiGe bipolar process [6].



$$Z_{in} = [R_1 + r_{\pi} - \omega M m_0 \sin(\phi)] + j\omega[L_1 + M m_0 \cos(\phi)]$$

Figure 1.11: Current Mirror Compensated Spiral Inductor

Figure 1.11 shows a current mirror compensation scheme to boost the effective quality of an on-chip spiral inductor. The equation describes the relationship between spiral and transistor device design parameters and the effective input impedance, where $i_2 = i_1 m_0 e^{j\phi}$ and M is the mutual coupling between the primary and secondary windings [7].

Active Inductor Circuits in RFIC Applications

A number of research papers have been published on transistor based structures that mimic the behavior of discrete inductors but strive for a larger Q than traditional

spiral inductors while using a fraction of the physical space. These circuits, called Active Inductors or AI's range in complexity, size and required power but all employ negative feedback to produce the desired inductive qualities. Simulations suggest and hardware confirms that the AI can easily be tuned to provide the desired L and Q at any particular process, voltage, and temperature (PVT) corner but L and Q vary wildly across a realistic PVT window.

The goals of this research were threefold. The first goal was to design and incorporate an AI into an on-chip, lumped element Wilkinson divider/combiner and to demonstrate a strong correspondence between simulation and hardware. Having established confidence in the model-to-hardware correlation, the second goal was to demonstrate, through transistor level simulation, an on-chip compensation scheme capable of controlling the inductance of the AI within the inductive limits defined by equation [1.11] while maintaining the minimum Q defined in equation [1.10], for application within a lumped element Wilkinson. The final goal was to summarize the limitations and design considerations that should be followed when implementing an AI based control scheme. That summary would then guide any future development of CMOS Active Inductors.

Simple Cascoded Active Inductor

Lyson [3] achieved a significant amount of progress towards identifying, understanding and implementing an AI and a compensation scheme that fulfils the requirements of many RFIC applications.

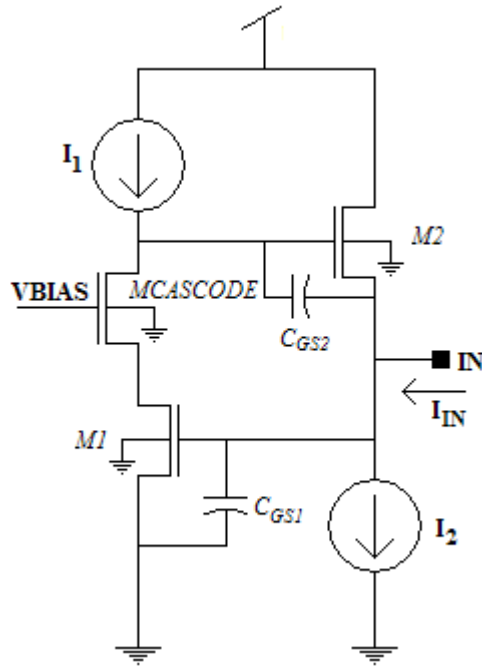


Figure 1.12: Simple Cascoded Inductor (SCAI) Schematic

He identified the Simple Cascoded Active Inductor (SCAI) in Figure 1.12 as a potential candidate for use as an inductive component in an RFIC application and proposed a compelling compensation scheme. While Lyson failed to produce a reliable compensation scheme across the entire PVT map of the AMIS C5 process, his work is the basis for further development of the AI and a potential compensation scheme.

The SCAI topology is composed of two cross coupled NMOS FETs (M1, M2) connected in a Gyrator configuration, where the DC bias point of each FET is controlled by a current source. A cascoding NMOS device (MCASCODE) is placed between the drain of M1 and the I_1 current source to increase the impedance seen by M2 and decouple the gate of M2 from the drain of M1 [2]. This has the effect of improving the Q, or reducing the effective series resistance looking into node IN. For the work presented herein, the I_1 and I_2 current sources are designed with long channel devices connected in

the typical current mirror configuration with on-chip reference poly-silicon resistors. The current sources are sized to provide a current ratio $I_2/I_1 \approx 8.46$ at typical process, 27°C , $V_{DD}=5.0\text{V}$. Later in this research it will be shown that this current ratio can be used to control the effective inductance of the SCAI.

Basic SCAI Operation: First, let's assume the initial current load (I_{IN_INIT}) is equal to zero. The circuit will arrive at a steady state operating condition where $I_{DM1} = I_1$, and $I_{DM2} = I_2$. The feedback associated with the gyrator topology will work to meet these criteria by adjusting V_{GM1} and V_{GM2} . The sizing of M1 is critical and has a large influence on the effective series resistance and the operating point of current source I_2 . To minimize the effective series resistance of the SCAI, M1 must be sized large enough such that V_{GM1} is only a few hundred millivolts greater than V_{THM1} but small enough such that the resulting V_{GM1} does not push current source I_2 into the linear region of operation.

If a load is connected and a current I_{IN} is forced into node IN, charge will accumulate raising V_{IN} and V_{GSM1} because under the initial conditions, $I_{DM2} = I_2$. The increase of V_{GSM1} will cause a subsequent increase in I_{D1} such that $I_{D1} > I_1$. This increase in I_{D1} discharges the gate of M2 faster than current source I_1 can charge it such that V_{GM2} decreases. As V_{GM2} decreases charge is pulled through C_{GS2} (the main integrating capacitor). This reduction in V_{GSM2} causes a subsequent reduction in I_{DM2} and so the iterative process continues until the circuit has successfully reduced I_{D2} enough to accommodate the input load current I_{IN} . It is this characteristic delay in accommodation of ΔI_{IN} which can be equated to an inductor or the resistance to a change in current.

MOS Corner	Bias Resistor Corner	L(nH)	Q _L
TYP	TYP	44.6	53.9
WC0	MIN	36.3	30.3
WC0	MAX	57.4	83.2
WCP	MIN	24.9	26.1
WCP	MAX	38.8	76.7
WCS	MIN	50.3	34.0
WCS	MAX	80.8	63.2
WC1	MIN	34.8	34.3
WC1	MAX	54.9	107.1

Table 1.2: Inductance and Q Factor of SCAI over Process

A 45nH SCAI was implemented in the AMIS C5 (0.6μm) process to determine the performance of the circuit across the process window of a low cost CMOS technology. The 45nH design point was chosen in accordance with equation 1.3 to be incorporated into a 250MHz lumped element Wilkinson. A summary of the simulated L and Q values is depicted in Table 1.2 shows that despite a sufficient Q_{LMIN}, the ΔL variation is much too large for most RF applications and certainly for the Wilkinson as determined in equations [1.10] and [1.11]. Active compensation is necessary to reduce the ΔL variation within acceptable limits. It should be noted that care was taken in the tuning of the 45nH SCAI to minimize the effective series resistance and maximize Q. This approach results in a small negative series resistance under some corners but when incorporated into a Wilkinson the load on the SCAI is such that stability is unconditional.

The SCAI Transfer Function: A simplified version of the SCAI transfer function was presented by Lu [4] and is shown in equation [1.12]

$$Y_{IN} = \frac{1}{Z_{IN}} \approx \frac{g_{M1}g_{M2}g_{MCAS}}{sC_{GSM2}(g_{MCAS} + sC_{GSMCAS})} + \frac{g_{M1}g_{MCAS}}{g_{MCAS} + sC_{GSCAS}} + sC_{GS1} \quad [1.12]$$

This transfer function assumes ideal current sources I_1 and I_2 , infinite transistor output impedance ($\frac{1}{g_{DS}} \approx \infty$), and neglects the effects of all parasitic capacitance with the exception of C_{GS} .

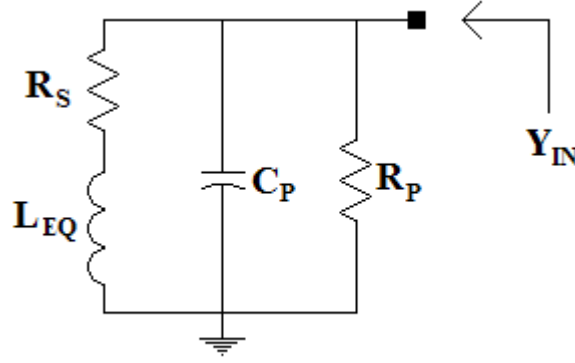


Figure 1.13: Lu's Lumped SCAI Model

$$\begin{aligned}
 L_{EQ} &\approx \frac{C_{GS2}}{g_{M1}g_{M2}} & R_S &\approx \frac{-\omega^2 C_{GS2}C_{GSCAS}}{g_{M1}g_{M2}g_{MCAS}} \\
 R_P &\approx \frac{1}{g_{M1}} & C_P &\approx C_{GS1}
 \end{aligned} \quad [1.13]$$

Figure 1.13 shows a lumped equivalent model for the SCAI. Values for the components shown in equation [1.13] were derived from the transfer function. Using this simple model, it is easy to understand the first order relationships between the SCAI input impedance and transistor design parameters. While equations [1.12] and [1.13] work well for predicting trends, the absolute accuracy is poor.

A simulation based sensitivity analysis was conducted to determine if a more accurate small signal model could be derived. The analysis began with a more complete model of the SCAI, assuming ideal current sources (I_1 , I_2) and including gate to source and drain parasitic capacitors. Each component was systematically removed to determine its contribution to the predicted impedance until only critical components remained.

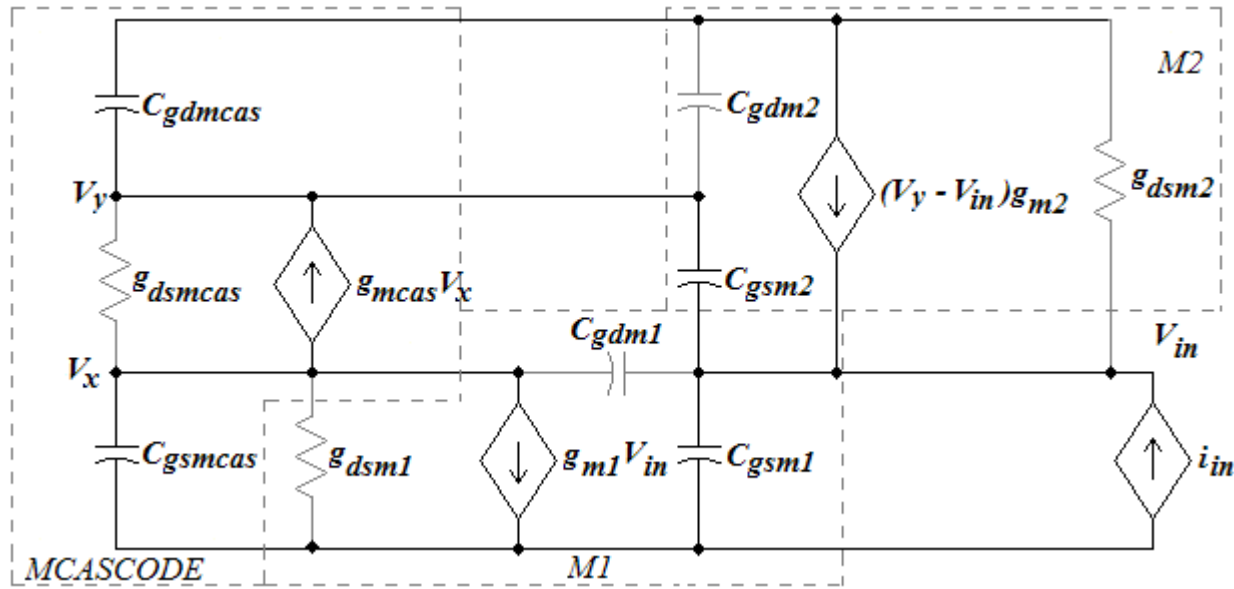


Figure 1.14: Small Signal Model Used to Derive SCAI Transfer Function

$$Z_{IN}(s) = \frac{s^2 C_{GSMCAS} [C_{GS2} + C_{GDMCAS}] + g_{MCAS} [C_{GS2} + C_{GDMCAS}] s}{C_{GSMCAS} [C_{GS1} (C_{GS2} + C_{GS4}) + C_{GS2} C_{GDMCAS}] s^3 + [C_{GS1} g_{MCAS} (C_{GS2} + C_{GDMCAS}) + C_{GDMCAS} C_{GSMCAS} g_{m2}] s + g_{MCAS} [C_{GDMCAS} g_{m2} + C_{GS2} g_{M1}] s + g_{M1} g_{M2} g_{MCAS}}$$

[1.14]

Figure 1.14 shows the small signal model used to derive an improved SCAI transfer function. The devices grayed out were determined to have a minimal effect at frequencies below 500MHz. This analysis shows the finite output impedance of each transistor ($\frac{1}{g_{DS}}$) can be ignored as well as C_{GDM1} and C_{GD2} . The remaining parasitic capacitors play an important role in the transfer function. Another sensitivity analysis was conducted with the derived transfer function to further minimize the equation by removing terms with little effect on the predicted input impedance. The final minimized transfer function for the SCAI is shown in equation [1.14].

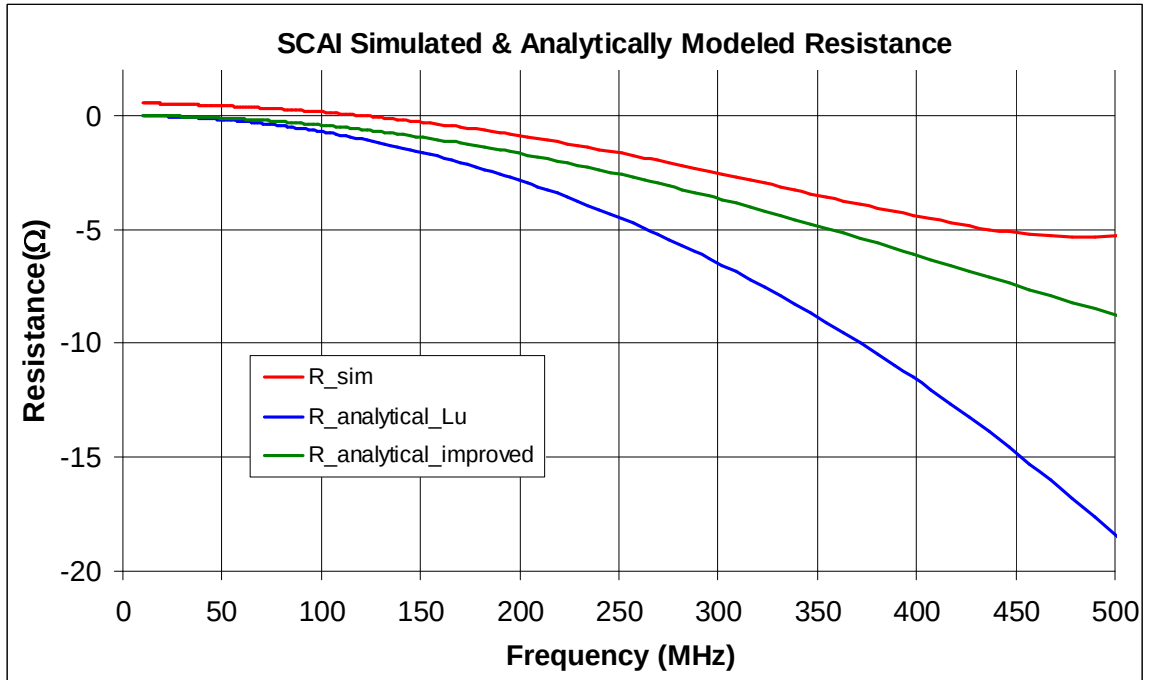


Figure 1.15: Comparison of SCAI Models for Predicting Series Resistance

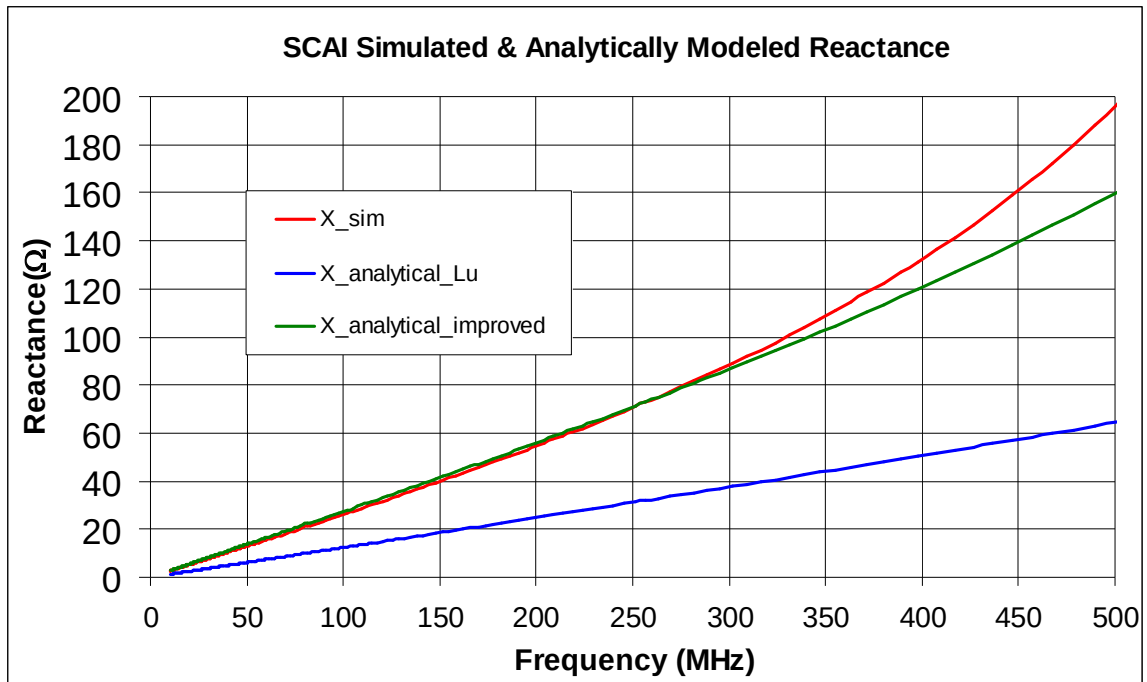


Figure 1.16: Comparison of SCAI Models for Predicting Inductance

Figure 1.15 and Figure 1.16 show a comparison of the models used to predict the behavior of the SCAI. The curves labeled R_{sim} and X_{sim} were generated using full small signal transistor models including all parasitics. The curves labeled $R_{analytical_improved}$ and $X_{analytical_improved}$ were generated with equation [1.14]. The curves labeled R_{Lu} and X_{Lu} were generated using Lu's simplified transfer function shown in [1.12]. From these curves it is easy to conclude that a vast improvement in accuracy can be obtained by including critical parasitic capacitance. However, the addition of these parameters complicates the equation to a point where the SCAI design parameters (R_S , L_{EQ}) are no longer easily discernable. Lu's equations should be used as a starting point for design but a circuit simulator is necessary to fine tune the circuit.

CPLL SCAI Compensation Scheme:

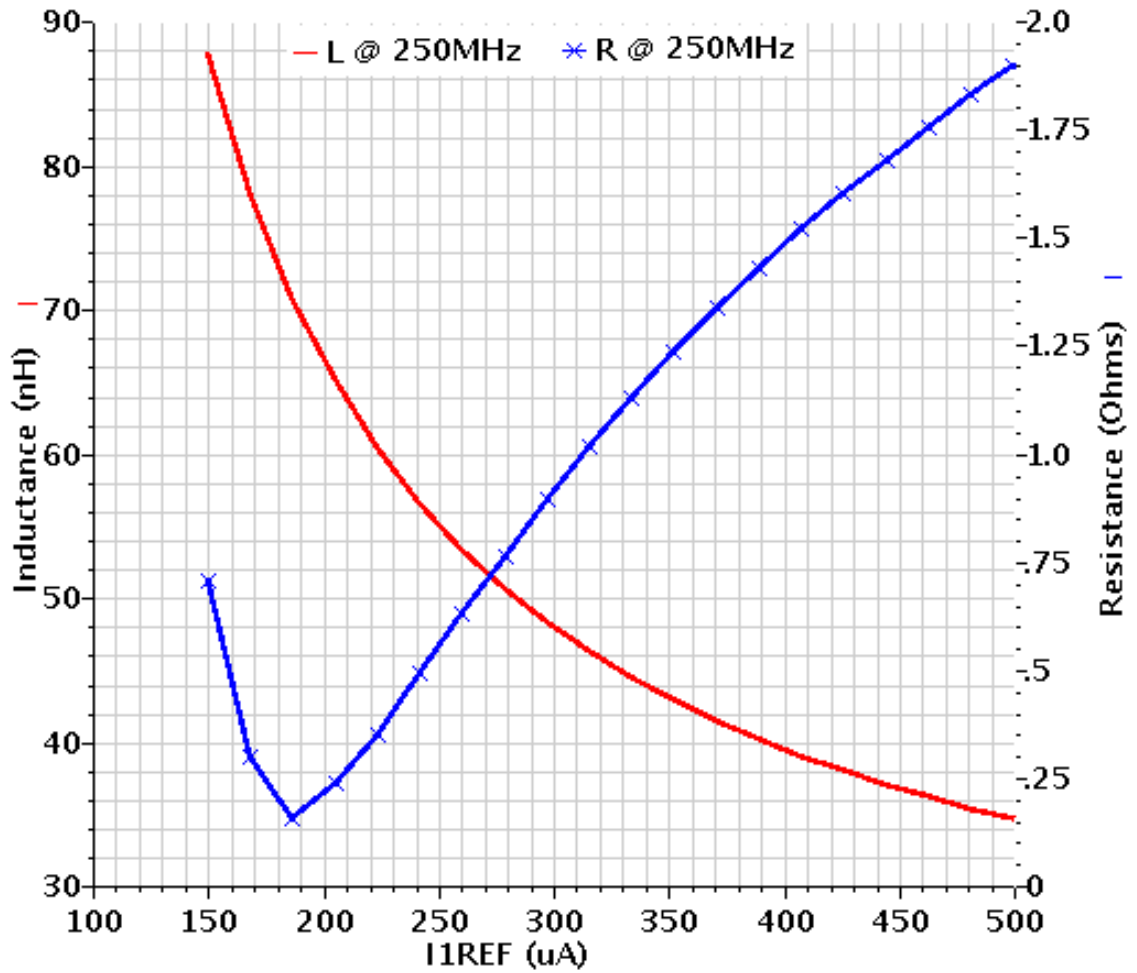


Figure 1.17: SCAI Inductance (L) & Resistance (R)
Vs I_1 Bias Current at 250MHz

The simulation results depicted in Figure 1.17 suggest a strong relationship between the Inductance (L) looking into node IN of Figure 1.12 at particular target frequency (250MHz) and the current I_1 .

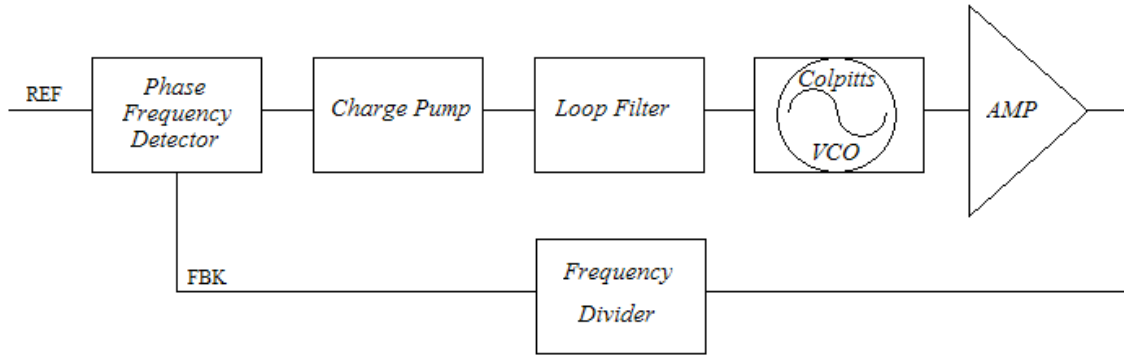


Figure 1.18: Lyson's CPPLL based AI Compensation Scheme

Lyson [3] proposed the control scheme depicted in Figure 1.18 to compensate the SCAI and maintain a constant L across PVT. This scheme involves embedding the SCAI in the feedback network of a Colpitts VCO (Figure 1.19) where the frequency of oscillation is controlled using a Charge Pump Phase Lock Loop (CPPLL) configuration. Assuming the operating frequency of the VCO is strictly a function of the inductive and capacitive values of the components in the feedback network and the variation of the feedback capacitors is negligible across PVT, the CPPLL will adjust the current through I_1 in the SCAI until the target inductance is reached.

Lyson [3] showed partial success with this scheme but was unable to achieve the desired inductive tolerance across the entire process window. Specifically, at the fast transistor process corner, the CPPLL adjusts the SCAI to have an inductive value much below the target of 45nH. Simulations confirm that at the fast transistor process corner the amplitude of the signal swing at node IN of the SCAI is large enough to push the NMOS transistor used to implement current source I_2 in and out of the saturated region. This makes the inductance looking into the SCAI vary as a function of the input voltage which is not an electrical characteristic indicative of an ideal inductor. The feedback

associated with the gyrator topology is such that the DC operating point of the circuit sets V_{GSM1} at a voltage only slightly higher than the device threshold V_{THM1} . As a result, the NMOS transistor used to implement current source I_2 is on the edge of the saturated and linear region of operation which limits the signal range over which the SCAI behaves like an ideal inductor to around 75mVpp. It is also important to note that accurate transistor modeling in and around the sub-threshold or depletion region of operation is imperative for this circuit to behave as designed.

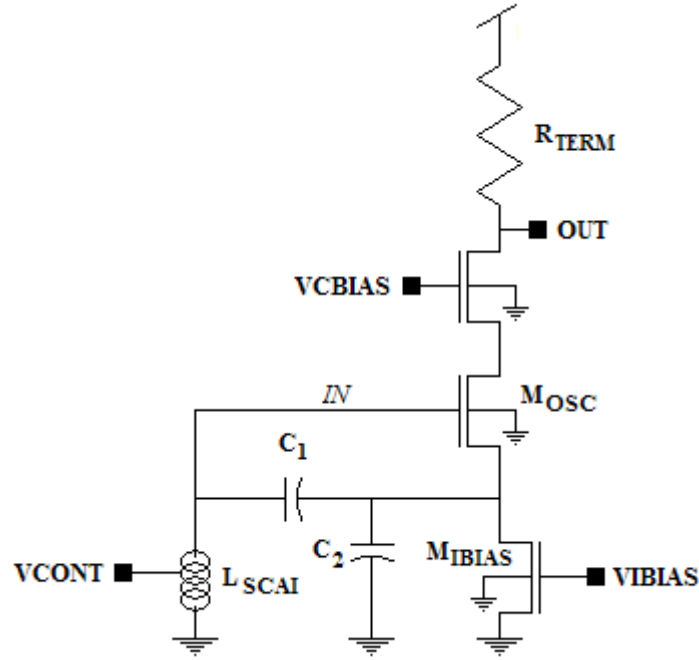


Figure 1.19: Colpitt's VCO w/AI

The amplitude of signal swing at node IN is primarily controlled by the small signal gain (g_m) of transistor M_{OSC} in Figure 1.19, which at the fast transistor corner is minimal. A large signal swing on node IN pushes the NMOS transistor used to implement I_2 in Figure 1.12 out of the saturated region for a portion of the period. As a result, the inductance looking into the SCAI also varies across the period and the SCAI

effectively distorts the signal at node IN. This is not an electrical characteristic indicative of an ideal inductor and thus the CPPLL adjusts the SCAI to an incorrect value.

More importantly, Lyson's research was conducted assuming an ideal current source for the VCO instead of the transistor implementation (M_{IBIAS}) as depicted in Figure 1.19. This assumption does not account for the effective reduction in V_{GSMOSC} caused by the voltage drop across M_{IBIAS} . While the gate voltage V_{GMOSC} is set by the DC operating point of the SCAI (which is slightly higher than the threshold voltage of M1 in the SCAI), the source voltage V_{SMOSC} is pushed up by the current source M_{IBIAS} . The reduction in effective V_{GSMOSC} is enough to significantly affect the frequency of oscillation and in some cases prevent oscillation. To maintain a high output impedance and minimize $V_{DSMIBIAS}$, M_{IBIAS} must be very large, adding a significant amount of parasitic capacitance in parallel with C2. Suggestions on how to improve the SCAI and alleviate this problem will be made later.

The Regulated Active Inductor

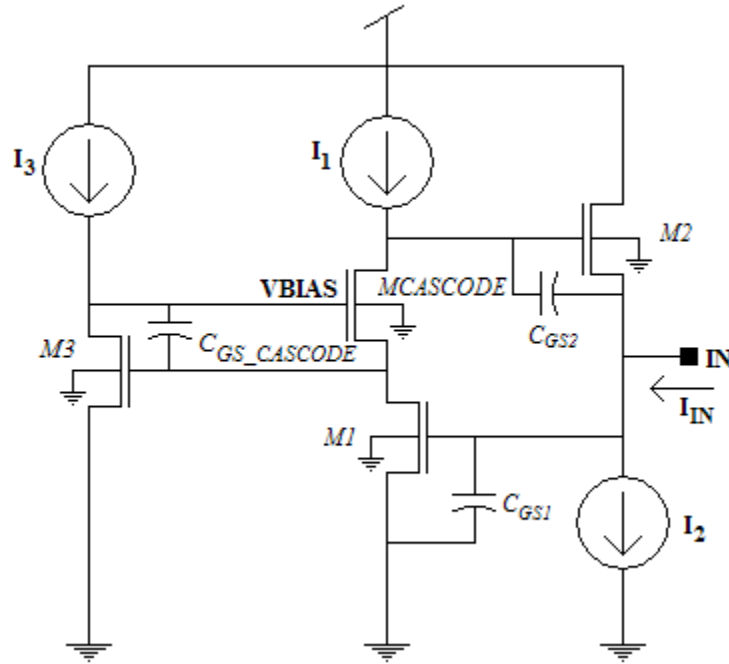


Figure 1.20: Regulated Active Inductor

The Regulated Active Inductor (RAI) depicted in Figure 1.20 functions similar to the SCAI but M3 acts to improve the effectiveness of the cascoding device MCASCODE [8]. An ideal inductor ($Q = \infty$) is achieved when the zero introduced by $C_{GS_CASCODE}$ perfectly cancels out the dominant pole associated with C_{GS2} . If the AI is tuned such that the zero occurs at a frequency lower than the pole, the effective series resistance of the AI will be negative at some frequencies which can lead to instability depending on the loading condition. The Q of the inductor at a target frequency is determined by the small signal gain $g_{m_CASCODE}$ which cannot be changed without affecting the location of the zero relative to the dominant pole. In other words, the Q at the target frequency cannot be optimized without risking a negative series resistance at other frequencies. The addition of M3 allows the effective small signal gain to be increased without affecting

$C_{GS_CASCODE}$ and its corresponding zero. In essence, the addition of regulating device M3 provides a method to control Q independent of L by tuning I_3 thereby giving the designer another degree of freedom [8].

$$L \propto 1/I_1 \quad [1.15]$$

$$R \propto I_3 \quad [1.16]$$

Unfortunately, like its counterpart, the RAI topology in Figure 1.20 also suffers from a very low node IN DC voltage in addition to signification variation of effective inductance across a reasonable PVT window.

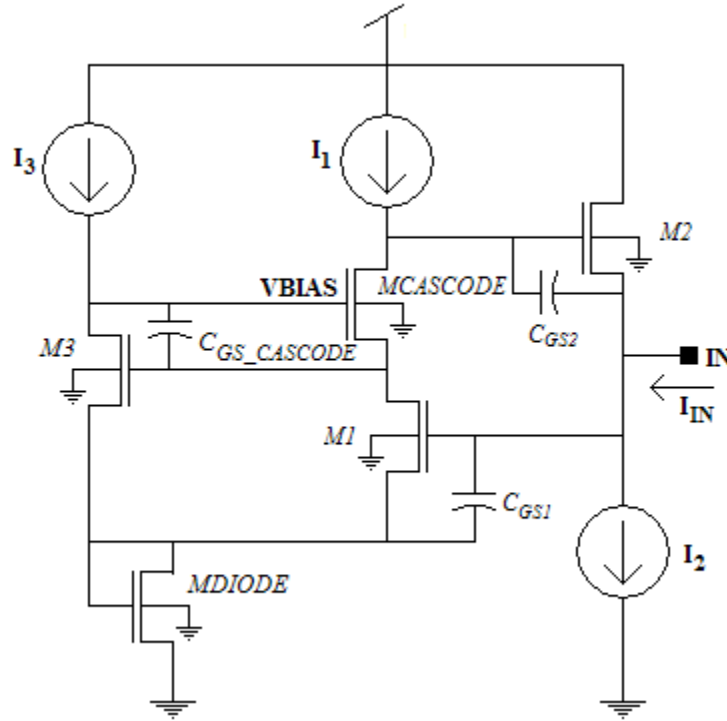


Figure 1.21: Enhanced Regulated AI

Figure 1.21 depicts an Enhanced Regulated Active Inductor (ERAI) that uses a diode connected NMOS device below the source of M1 to boost the DC voltage of node

IN by an amount ΔV_{LIFT} . The current through MDIODE is the sum of I_1 and I_3 . Unless these two currents are extremely small, MDIODE operates in saturated and strong inversion region.

$$\Delta V_{LIFT} = V_{DSMDIODE} = V_{GSMDIODE} = \sqrt{\frac{2I_{DSMDIODE}}{\mu_n C_{OX}}} * \frac{L}{W} + V_{THN} \quad [1.17]$$

Equation [1.17] shows how ΔV_{LIFT} can be manipulated with physical transistor design variables. ΔV_{LIFT} comes at the cost of additional effective series resistance in the AI but that adjusted by further reducing I_3 . The combination of an uplifted DC bias point at node IN and the ability to independently control Q and L suggests the ERAI could be useful in a wider range of RFIC applications. In reality PVT variation has a significant enough effect on the Q and L that both variables must be compensated for this AI to be useful in most RF applications. The availability of two independent controls (I_1 and I_3) makes a compensation scheme with two control loops theoretically possible however the complexity of developing a scheme like this may far outweigh the benefit of an on chip inductive component and thus this research focuses on developing an on chip control scheme for the SCAI configuration.

Thesis Overview

Chapter 2 presents the hardware results and basic model-to-hardware correlation of various experiments on the BOBCAT_V0 test chip. This chip, fabricated in the AMIS C5 process, is intended to verify functionality and manufacturability of key components in the on-chip SCAI compensation scheme proposed in Chapter 3. Basic model-to-hardware correlation is used to highlight potential inaccuracies in device modeling,

simulation technique, measurement technique, design technique and any real world circuit limitations not accounted for during development. In Chapter 3, a novel Master Slave SCAI compensation scheme is presented differing significantly from that developed by Lyson [3] but still designed with the goal of producing an inductive element for use in an on-chip lumped Wilkinson and potentially a broader array of RF applications. The simulated performance of the master compensation scheme as well as the slave Wilkinson is analyzed. Chapter 4 is a brief summary of results, limitations and suggestions for future improvements to the compensation scheme.

BOBCAT_V0 HARDWARE MEASUREMENTS, PERFORMANCE
AND MODEL TO HARDWARE CORRELATION

Introduction

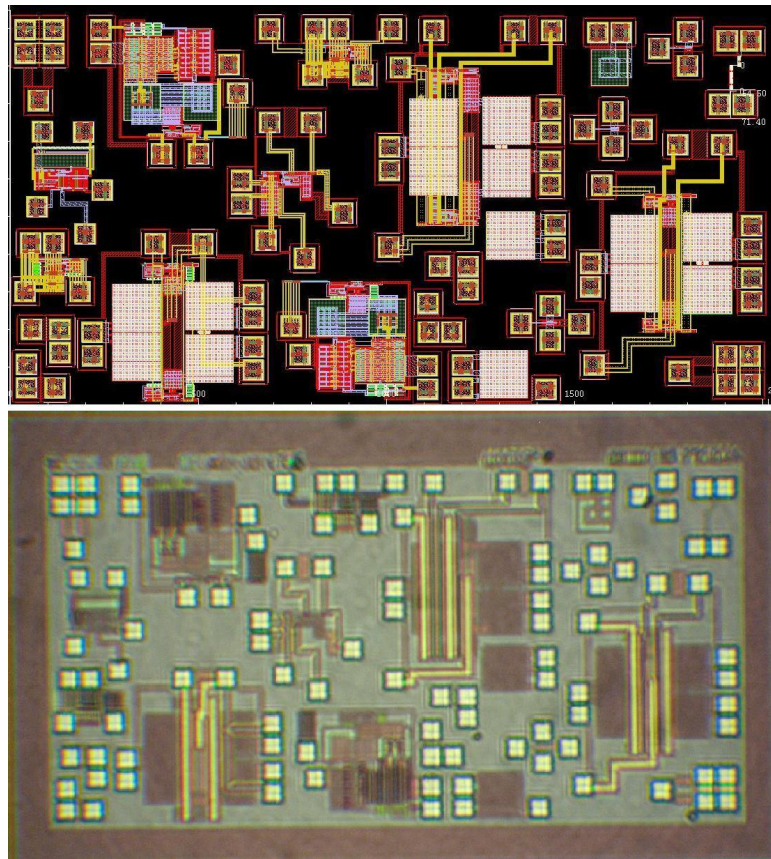


Figure 2.1: Bobcat_V0 Test-Chip

Figure 2.1 shows the Bobcat_V0 Test-Chip, which was designed and manufactured in the AMIS C5 Process (0.6 μ m) through the MOSIS Educational Program for the purpose of verifying the functionality and performance of critical circuits to be used in future implementation of an on-chip, PVT-compensated Wilkinson power divider/combiner.

A series of experiments focused on three key circuits groups.

1. Critical Passive Device Characterization
 - a. Short, Open, Thru calibration comparison
 - b. 250MHz Wilkinson 9pF poly-silicon parallel plate capacitor
 - c. 50 Ω poly-silicon terminating resistors
2. Simple Cascoded Active Inductor (SCAI)
 - a. Fixed on-chip current references tuned for 45nH at 250MHz under typical operating conditions (nominal process, 27°C, $V_{DD} = 5V$).
 - b. Independently programmable, on-chip current references tuned for 45nH at 250MHz under typical operating conditions to enable at test tuning.
3. On-Chip Lumped Wilkinson w/fixed on-chip current references used to bias an SCAI tuned for 45nH at 250MHz under typical operating conditions (nominal process, 27°C, $V_{DD} = 5V$).

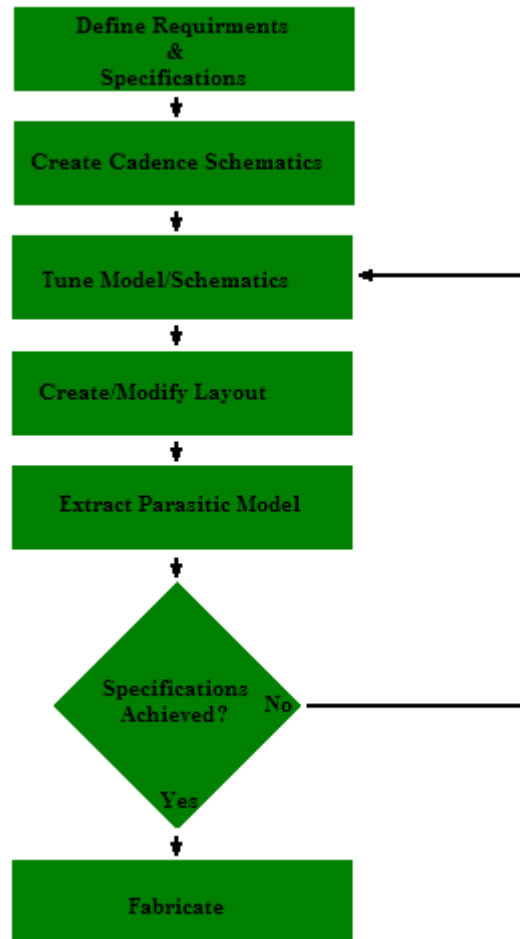
Design Implementation Strategy

Figure 2.2: Basic VLSI Design Flow

An iterative approach, as depicted in Figure 2.2, was employed to design each individual circuit component and eventually each experiment. Circuits were initially designed using schematic-based models, which do not include parasitic resistance or capacitance. A DRC and LVS complete layout is necessary for a parasitic inclusive model.

Parameter	Corner Values
Temperature ($^{\circ}\text{C}$)	15, 30
Voltage (V)	4.95, 5.05
Transistor Process	Fast P/Fast N, Fast P/Slow N, Slow P/Slow N, Slow P/ Fast N
Capacitor Process	High Capacitance, Low Capacitance
Resistor Process	High Resistance, Low Resistance

Table 2.1: Process Voltage Temperature Bounding Corners used in Simulation

An initial design point is reached by simulating each of 64 possible Process, Voltage, and Temperature (PVT) corners defined in Table 2.1 to ensure each design parameter falls within a desired range under any possible operating condition. Industry compliant designs typically support a much wider temperature and voltage range, -55°C to 125°C and $\pm 10\%$ power supply variation respectively, but given the controlled environment of the MSU laboratory, reduced ranges were deemed sufficient.

Once an initial design point is reached the physical implementation or layout is completed using the Assura Design Rule Checking (DRC) and Assura Layout Vs Schematic (LVS) tools available in the AMIS C5 design kit. Once a circuit is LVS and DRC clean, the Assura Extraction tool can be used to develop a circuit model which includes parasitic devices (capacitors, resistors) as well as proximity effects that model device-to-device interaction. The circuit is then retuned to compensate for changes in behavior caused by the parasitics included in the new model. This iterative approach is repeated until the circuit (including parasitics) meets the requirements defined by the application and environment.

Hardware Measurements and Results

Test Setup

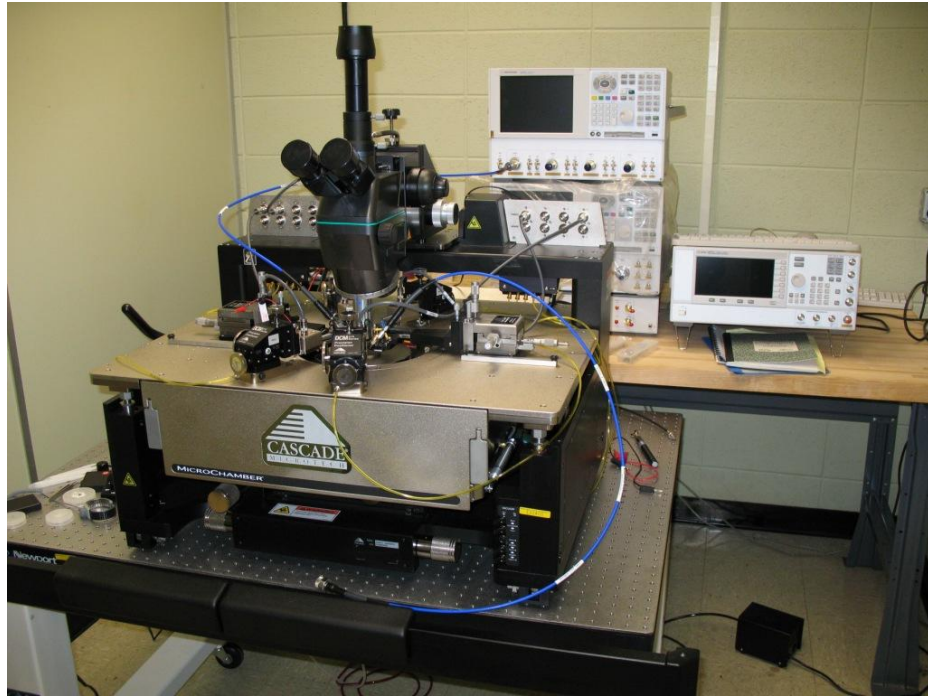


Figure 2.3: MSU IC Testing Facility

Figure 2.3 shows a portion of the MSU IC test facility including the probe station with microscope, various RF and DC probes, power supplies, oscilloscope, and vector network analyzer.

As a general test approach, the Vector Network Analyzer is used to characterize the S-Parameters for each circuit/experiment. Measured S-Parameters can be mathematically manipulated to a more common form such as resistance, capacitance and inductance if desired. The measured and simulated electrical characteristics are then graphically compared to achieve basic model-to-hardware correlation. The following is a list of components used in a typical test setup for the experimental results reported herein.

Vector Network Analyzer: Agilent N5230A

Calibration Standard: CS-8

1 Port RF Probe: GGB 40A-65-50-P-N GGB Picoprobe

2 Port RF Probe: GGB 40A-5G-50-D-50-N GGB Picoprobe

Probe DC Block: BLK-89-S+

Probe Bias T Block: Zx85 Bias-T

Power Supply: Tektronix P5280 DC Power Supply

Multi-meters: Agilent 34411A & U1250A DMM

Potentiometer: 123T-W503

A GGB CS-8 calibration substrate was used prior to every measurement to calibrate the VNA and place the reference plane at the probe tips ensuring the utmost measurement accuracy. The VNA was calibrated using a short open, load technique for one port measurements and a short, open, load, thru technique for multi-port measurements as instructed by the user manual.

Critical Passive/Active Device Characterization

The standalone, passive devices were characterized first for the purpose of verifying the test setup, approach and quantifying the parasitics associated with the probe pads.

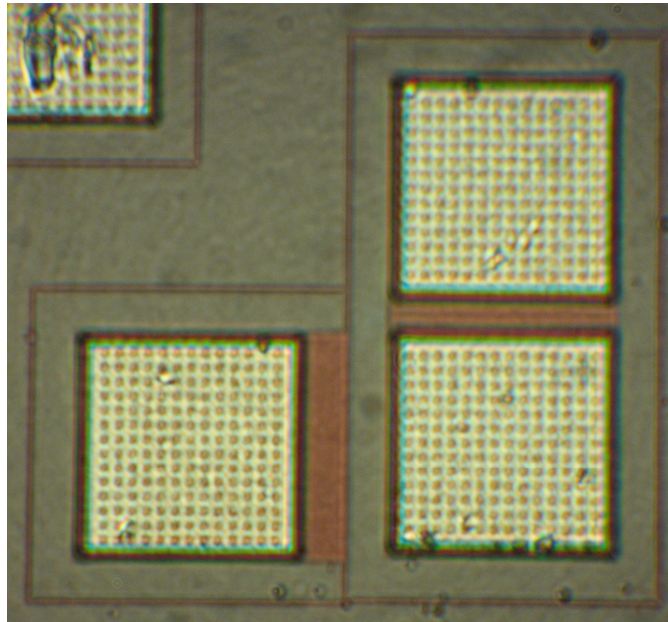


Figure 2.4: Bobcat_V0 Floating Short Experiment

Figure 2.4 shows the Floating Short experiment available on Bobcat_V0. The Grounded Short experiment is identical with the exception that all pads are connected to the substrate which is then grounded. Multiple levels of metal are used to connect the pair of pads, and the relative spacing is small to minimize the resistive contribution from the connecting metal such that any measured resistance can be attributed to the pads themselves. The structure depicted in Figure 2.4 is used to determine the parasitic resistance associated with the measurement network which, is subtracted from subsequent measurements.

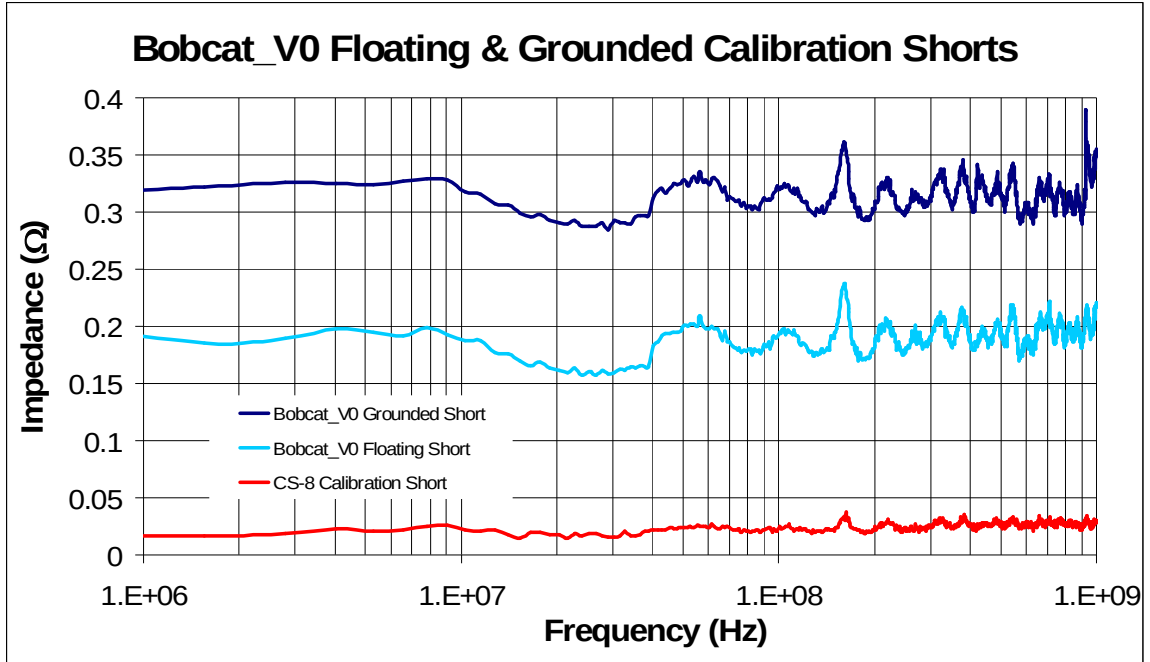


Figure 2.5: Bobcat_V0 Short Experiment Results

The measured S-parameters were manipulated to produce Figure 2.5 , which displays the real component of the impedance across the frequency range of interest. Because the resistance of the metal connecting the pads is very small, the Grounded and Floating Shorts curves can be thought of as the resistive contribution by the measurement network to the measured series resistance (R_{TESTER}). The measurement network for each experiment varies only slightly, allowing R_{TESTER} to be subtracted from each set of measurement results if 0.3Ω - 0.2Ω is a significant part of the total real impedance. It is also important to note the lack of relationship between the real component of impedance and frequency over the desired frequency range. The reactive component of the impedance was omitted from Figure 2.5, but it was very close to zero over the entire frequency range.

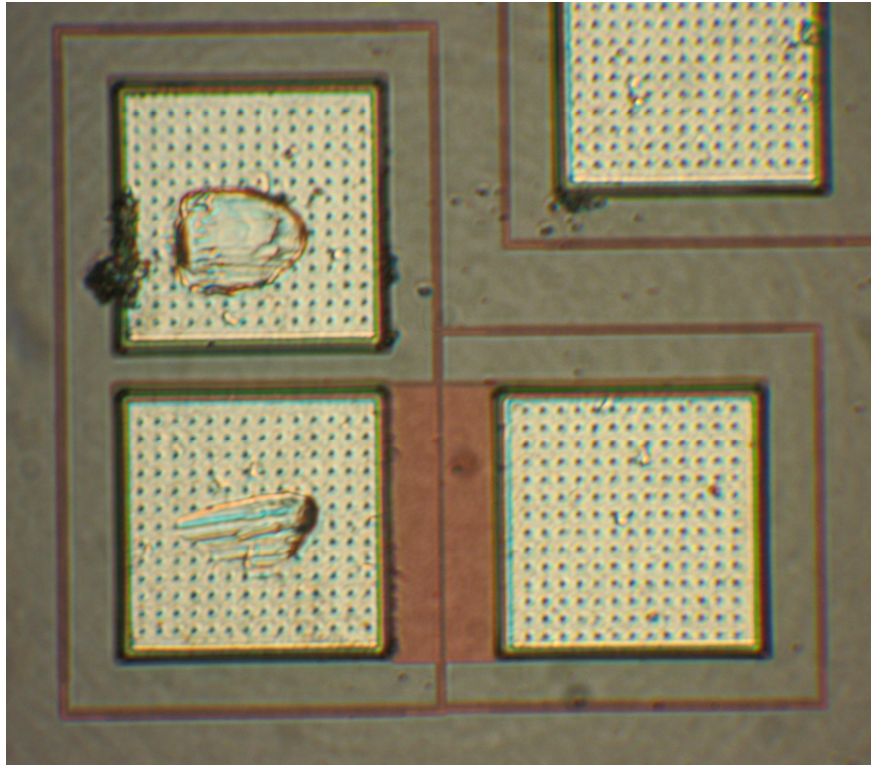


Figure 2.6: Bobcat_V0 Open Experiment

Figure 2.6 shows the Open experiment available on Bobcat_V0. The pads in the upper and lower left coincide with the positive and negative probe terminals while the pad on the lower right can be used to connect the substrate to ground through a DC probe. Multiple levels of metal are used to connect the negative terminal and substrate connection to ground to minimize any series resistance. The structure depicted in Figure 2.6 is used to determine the parasitic capacitance associated with the measurement network. If this parasitic capacitance becomes a large percentage a subsequent measurement it can be subtracted.

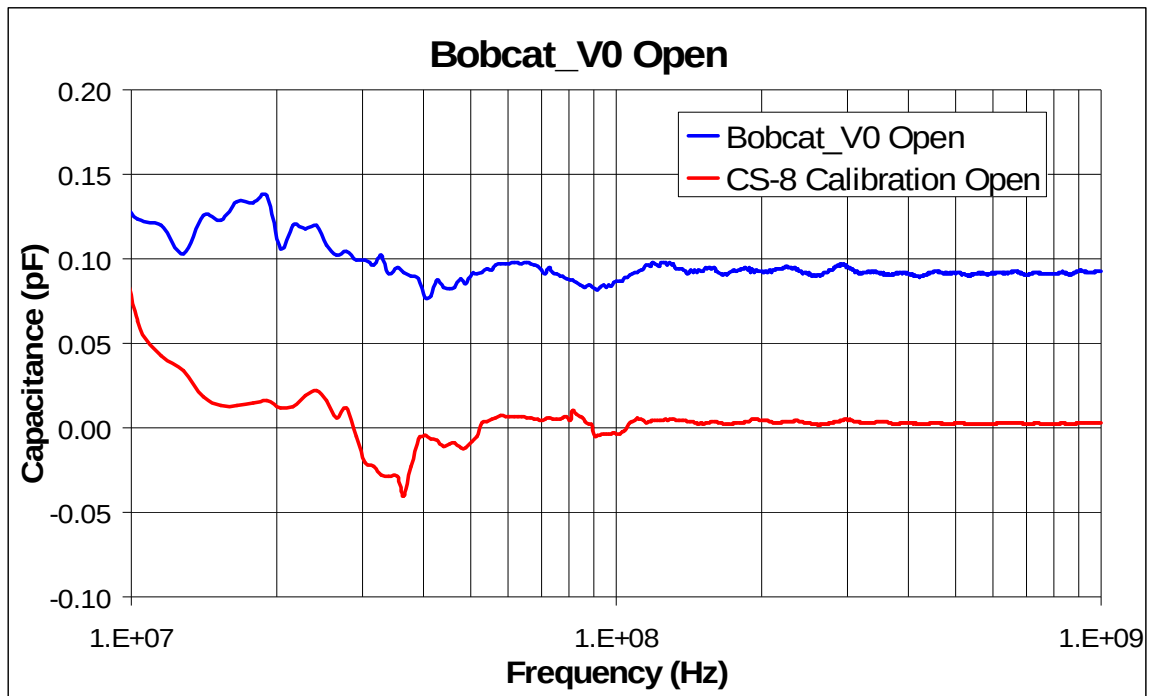


Figure 2.7: Bobcat_V0 Open Experiment Results

Figure 2.7 shows the Bobcat_V0 Open experiment (in blue) yielded S-parameters and an effective capacitance very similar to the Open calibration standard (in red) which implies good isolation between the two probe terminals and associated networks. The Bobcat_V0 Open experiment represents the capacitive contribution by the measurement network and theoretically could be subtracted from each subsequent measurement. At the frequencies of interest, the contribution of 100fF is insignificant.

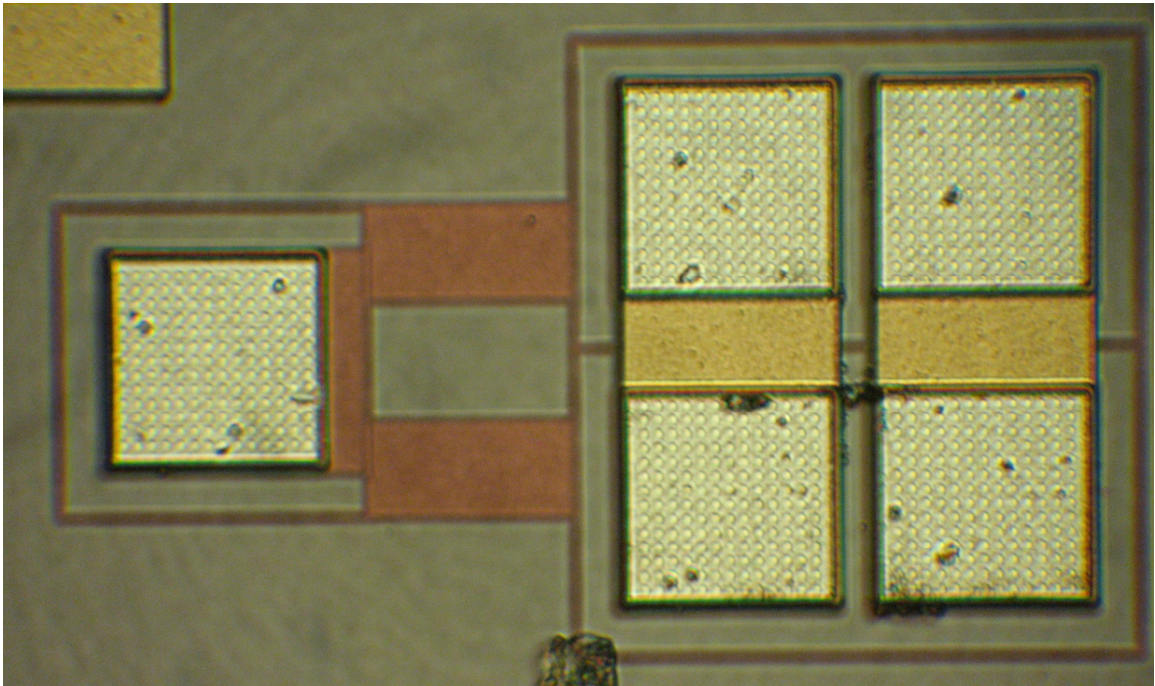


Figure 2.8: Bobcat_V0 Thru Experiment

Figure 2.8 shows the Thru experiment available on Bobcat_V0. The two pairs of pads on the right are probed with the RF probe terminals while the single pad on the left is used to ground the substrate with a DC probe. To minimize resistance and insertion loss, a 24 μ m strip of Metal 3 the width of the pads connects the two pair.

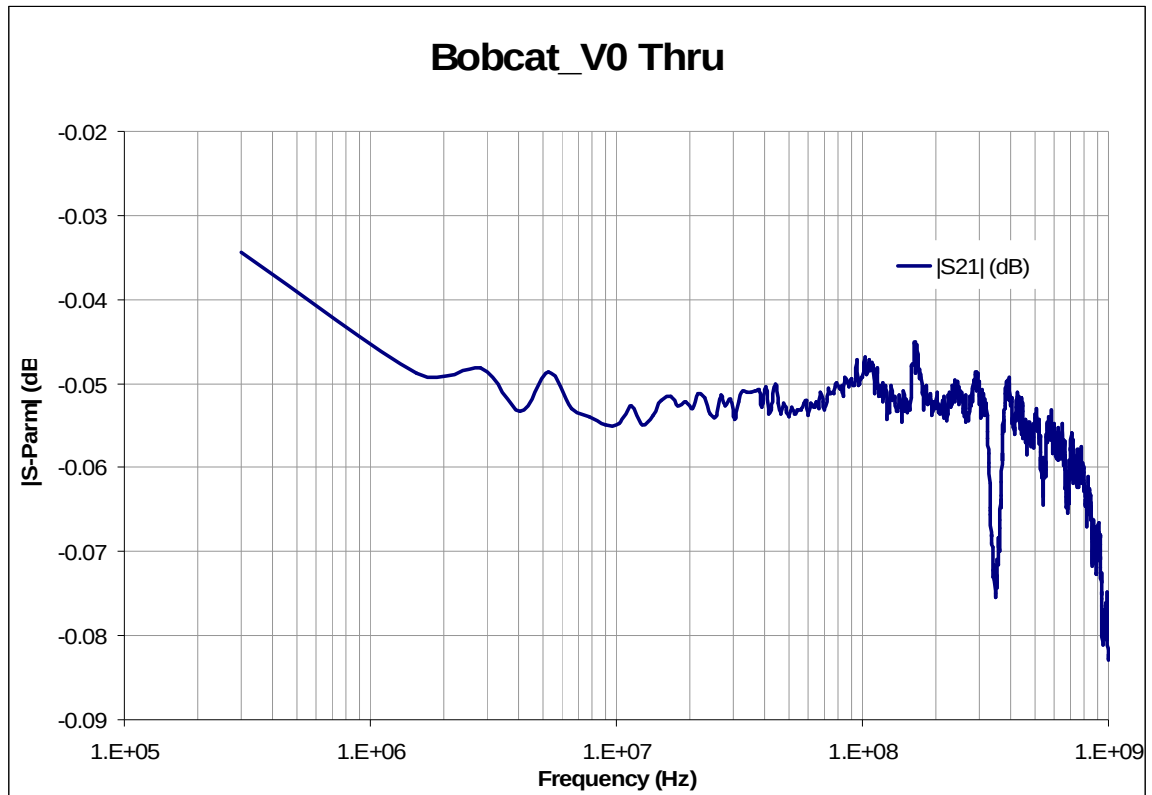


Figure 2.9: Bobcat_V0 Thru Experiment Results

Figure 2.9 shows the measured Transmission Coefficient (S_{21}) for the on-chip thru experiment. A 24 μ m long strip of Metal 3 connects Ports 1 and 2 and causes approximately 0.055dB of attenuation at these low frequencies. This relatively small amount of signal attenuation associated with the measurement network can be ignored when making comparisons between measured and predicted results for a significantly lossy network like the Wilkinson.

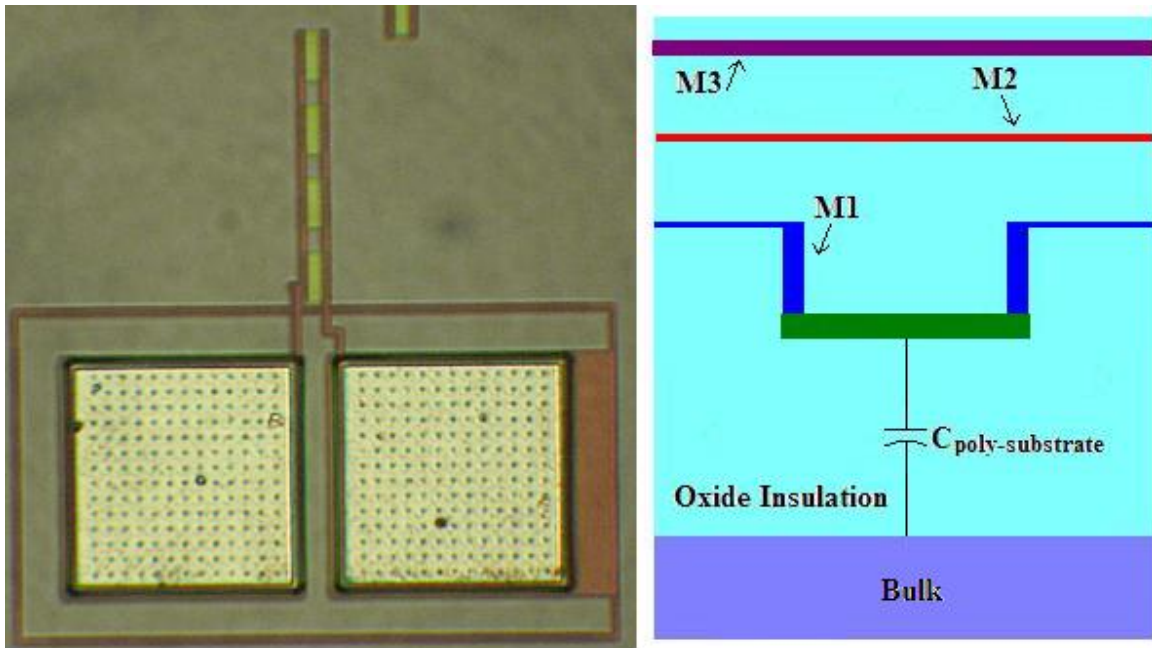


Figure 2.10: Bobcat_V0 50Ω Polysilicon Resistor Experiment

Figure 2.10 shows the 50Ω polysilicon resistor experiment available on Bobcat_V0. The 50Ω resistor is actually composed of 4 200Ω resistors connected in parallel. The C5 technology offers a polysilicon and diffused resistor. I selected the polysilicon option because of the higher sheet resistance which, based on the desired resistance values, resulted in a physically smaller device with less parasitic capacitance. The cross section of the device shows the resistor is built on the second level of poly to minimize parasitic capacitance to substrate and metal 1 is used to wire each terminal

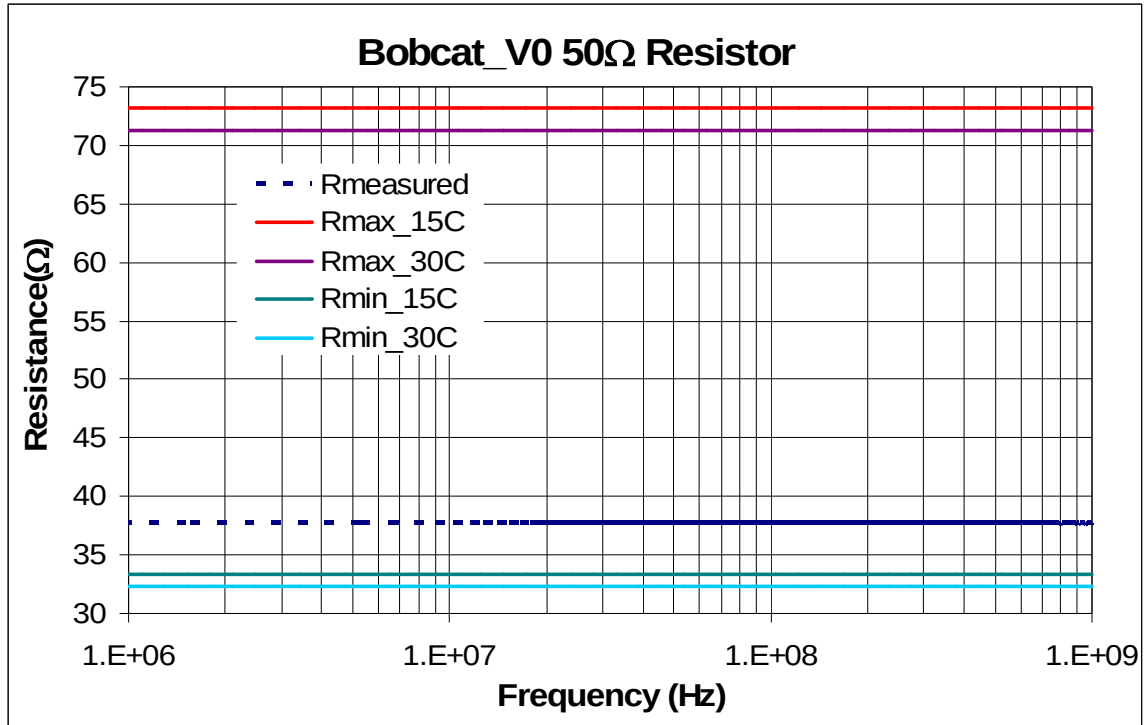


Figure 2.11: Bobcat_V0 50Ω Experiment Results

Figure 2.11 shows the predicted and measured resistance of a polysilicon resistor designed to 50Ω. The resistance measured is well within simulation-based predictions but appears to be lower than the target 50Ω. The four simulated corners show that process (Rmax/Rmin), rather than temperature, has the largest effect on the resistance. It is also interesting to note that simulations indicate this polysilicon resistor has a negative temperature coefficient which is contrary to the diffused resistor also available in the C5 process.

The relationship between temperature and resistance described by equation [2.1] can be used as a sanity check to verify the simulator [18].

$$R = R_0[1 + T_{CO1}(T - T_{NOM}) + T_{CO2}(T - T_{NOM})^2] \quad [2.1]$$

Process Corner	$T_{C01}(^{\circ}\text{C}^{-1})$	$T_{C02}(^{\circ}\text{C}^{-1})$
Minimum Resistance	-2.13×10^{-3}	3.88×10^{-6}
Maximum Resistance	-1.74×10^{-3}	6.04×10^{-6}

Table 2.2: Temperature Coefficients for C5 Polysilcon Resistor

Temperature coefficients shown in Table 2.2 were obtained from the C5 simulation models.

Resistor Process	Temperature ($^{\circ}\text{C}$)	$R_{\text{PREDICTED}} (\Omega)$	$R_{\text{SIMULATED}} (\Omega)$
MIN	15	33.39	33.39
MIN	30	32.34	32.34
MAX	15	73.18	73.18
MAX	30	71.28	71.28

Table 2.3: Predicted Vs Simulated Resistance for Bobcat_V0 50 Ω Resistor Experiment

Table 2.3 shows a comparison between predicted and simulated resistance. The results confirm that equation [2.1] is used by the Spectre simulator to calculate the temperature dependency of polysilicon resistors in the C5 process.

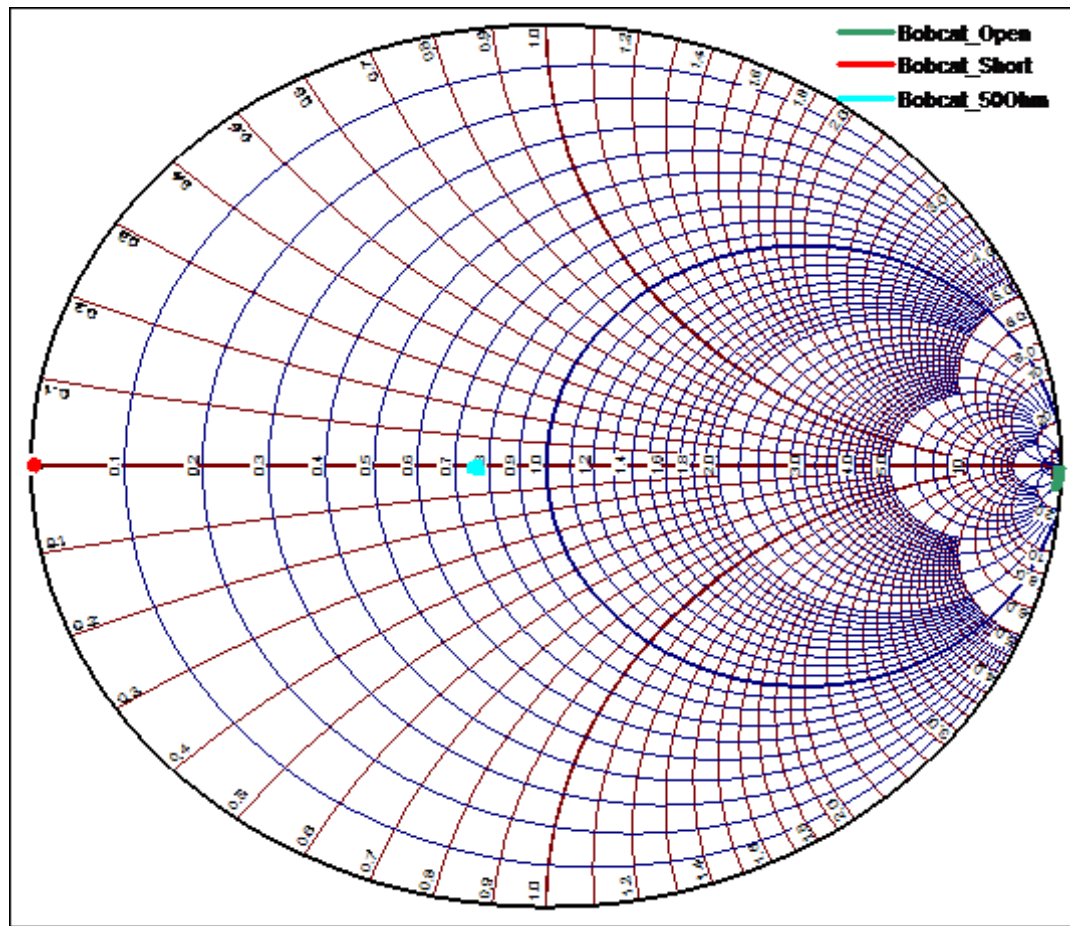


Figure 2.12: Bobcat_V0 Open, Short, Thru Experiment Results

Figure 2.12 shows the measured S_{11} parameters for the Open, Short and 50Ω polysilicon experiments plotted on a Smith Chart. As depicted in Figure 2.5, Figure 2.7 and Figure 2.11 the open and short are near perfect and the polysilicon resistance is slightly below the target of 50Ω.

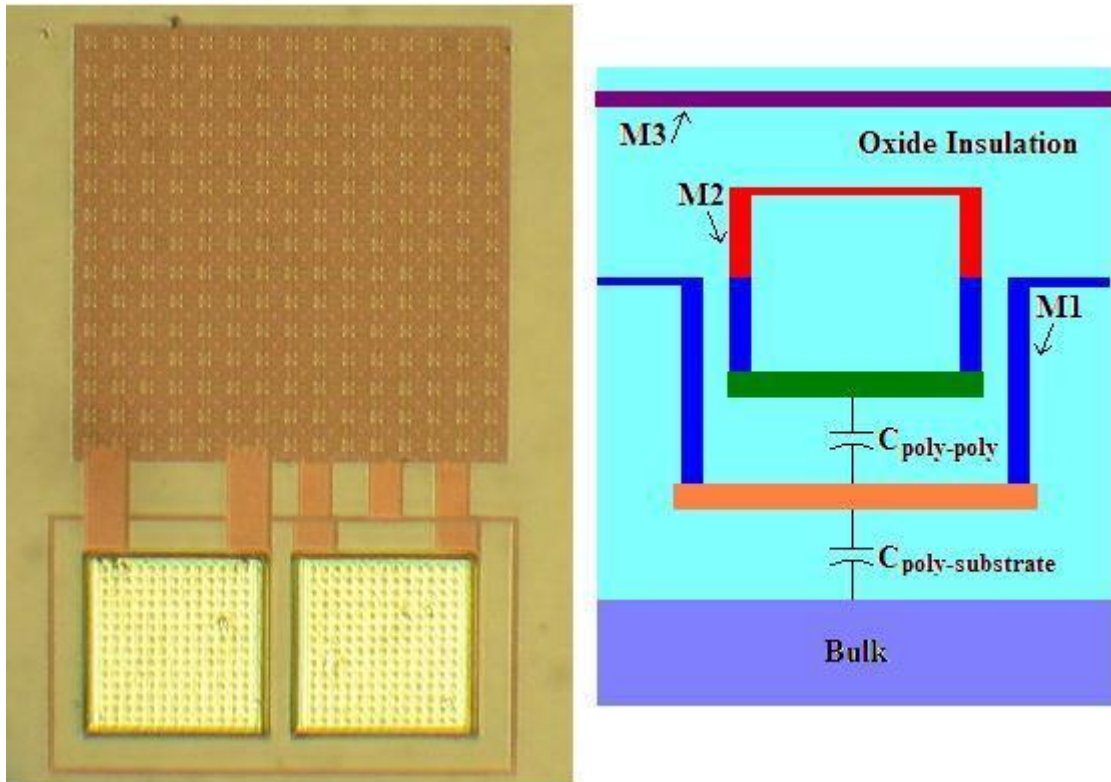


Figure 2.13: Bobcat_V0 9pF Distributed Capacitor

Figure 2.13 shows the 9pF distributed capacitor experiment available on Bobcat_V0. The capacitor is constructed in a distributed fashion with 225, $3\mu\text{m} \times 3\mu\text{m}$ poly-to-poly, parallel plate capacitors wired together in parallel to minimize anode and cathode resistance. The pad located in the lower right of Figure 2.13 is connected to the cathode and substrate. The pad located in the lower left is connected to the anode. The cross section on the right shows how the capacitor is constructed, isolated and wired. The majority of the capacitance is between the two polysilicon parallel plates. A parasitic capacitor between the lowest level of polysilicon and substrate has a capacitance roughly equal to 10% of the poly-to-poly device.

The distributed design approach segments and parallelizes the anode and cathode resistance to reduce the total effective series resistance. For a given unit cell with

capacitance C_i and effective resistance R_i , the total capacitance and resistance of the distributed device is shown in equations [2.2] and [2.3]

$$C_{TOT} = N * C_i \quad [2.2]$$

$$R_{TOT} = \frac{R_i}{N} \quad [2.3]$$

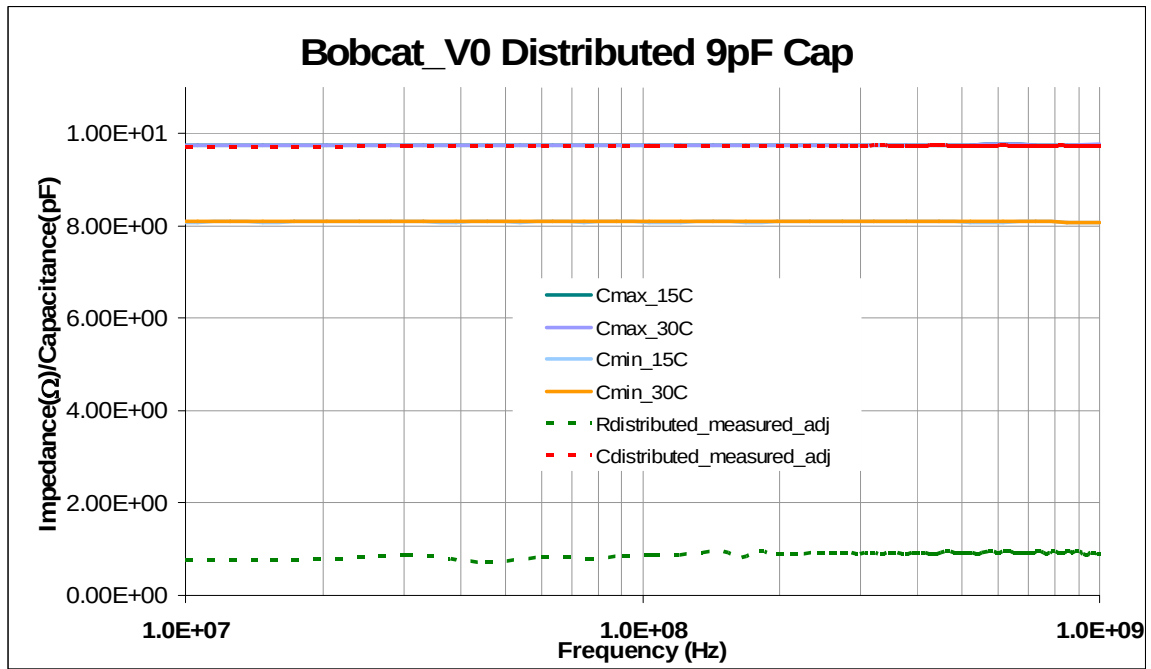


Figure 2.14: Bobcat_V0 9pF Distributed Capacitor Experiment Results

Figure 2.14 shows the predicted and measured capacitance and measured series resistance of the distributed 9pF capacitor experiment. The measured results have been manipulated to account for the resistive and capacitive contribution of the measurement network shown in Figure 2.5 and Figure 2.7. This manipulation slightly shifted the capacitance curve ($C_{distributed_measured_adj}$) to fall within the bounds predicted by simulation and had a significant effect on the measured resistance and Q of the capacitor. At 250MHz, a measured reactance of -65Ω and resistance of 0.904Ω corresponds to a Q

= 71.9. The parasitic capacitance associated with the metal required to wire all the parallel devices together was not included in the simulation model. This modeling inaccuracy could explain the near deviation from simulation based predictions. It also appears that temperature has very little if any effect on the capacitor models as the simulated curves at different temperatures are identical. equations [2.2] and [2.3] imply that the smallest allowable unit cell would result in the highest quality distributed capacitor but there are other design tradeoffs to consider. As the unit cell dimensions approach technology minimum, ΔW and ΔL variation will have a more pronounced effect on the capacitors tolerance. In addition, fringe capacitance becomes a much larger percentage of the total capacitance and may not be modeled well in a small device.

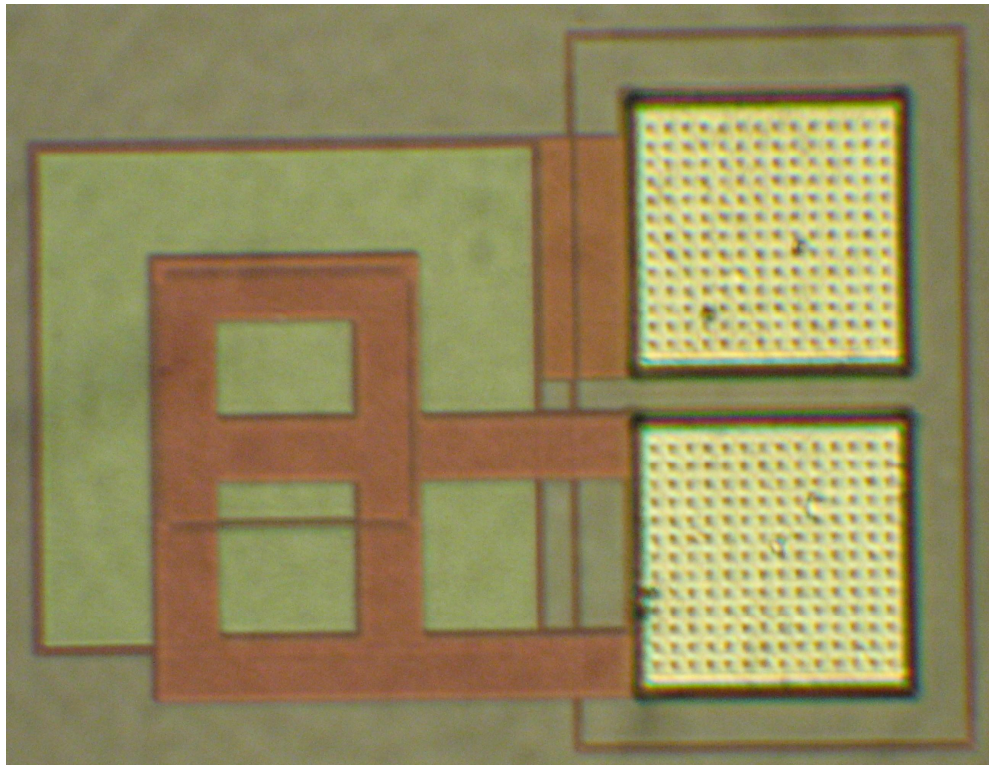


Figure 2.15: Bobcat_V0 9pF Lumped Capacitor Experiment

Figure 2.15 shows the 9pF Lumped capacitor experiment available on Bobcat_V0. This capacitor design is composed of one single 1000um x 1000um capacitor, so the physical nature of this design technique does not allow for minimizing series resistance. The pad located in the upper right is connected to the cathode and substrate. The pad located in the lower right is connected to the anode.

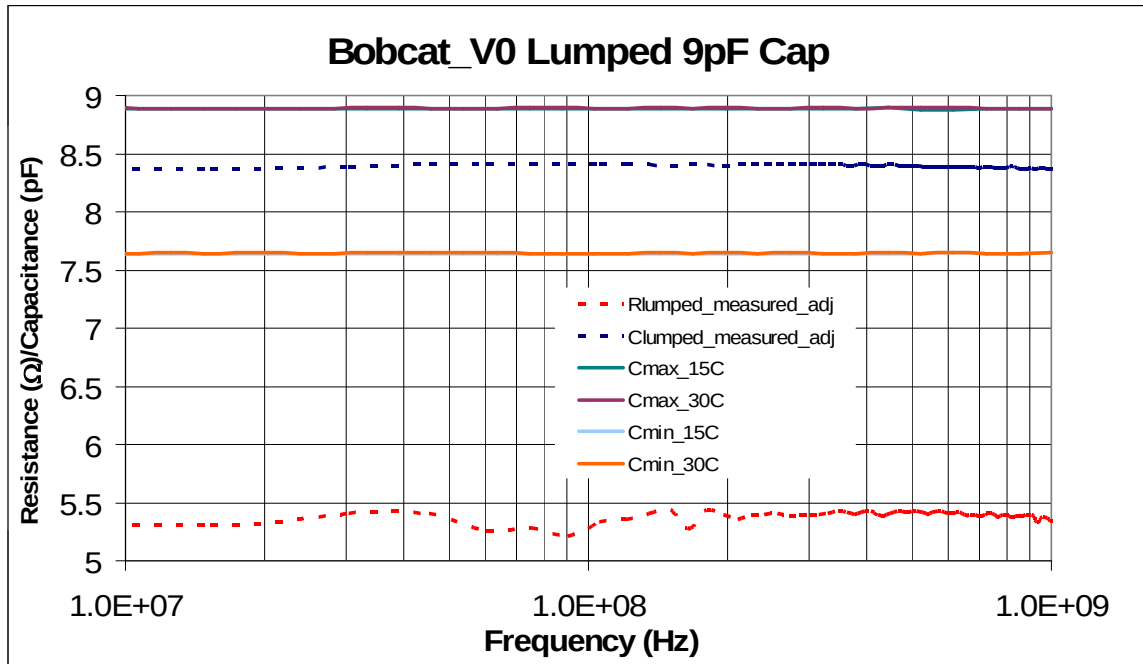


Figure 2.16: Bobcat_V0 9pF Lumped Capacitor Experiment Results

Figure 2.16 shows the predicted and measured capacitance and measured series resistance of the lumped 9pF capacitor experiment. The measured results have been manipulated to account for the resistive and capacitive contribution of the measurement network shown in Figure 2.5 and Figure 2.7. This manipulation slightly shifted the capacitance and resistance curves. At 250MHz, a measured reactance of 71.9Ω and resistance of 5.4Ω corresponds to a $Q = 14.1$. Measured results fall well within the bounds of simulation in contrast to the distributed capacitor experiment, implying a more

accurate model. This is consistent with the theory that parasitic wiring capacitance is not adequately modeled in the distributed capacitor experiment.

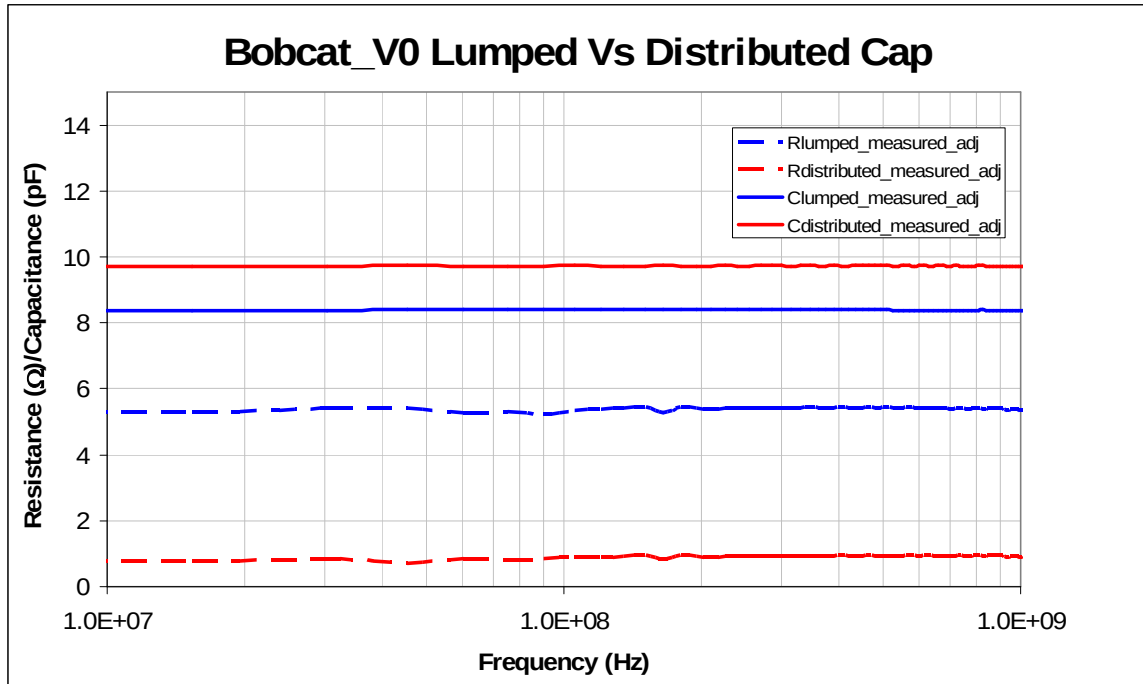


Figure 2.17: Bobcat_V0 Lumped Vs Distributed Capacitor Results

Figure 2.17 shows a graphical comparison of the measured results for both capacitor design techniques. The measured series resistance of approximately 5.5Ω is significantly larger than observed in the distributed capacitor results of Figure 2.14. To determine which technique is truly superior, the capacitance per unit area and the series resistance must also be taken into account.

$$D_{CAP_DENSITY} = \frac{Capacitance}{Area} \quad [2.4]$$

$$D_{DISTRIBUTED_CAP_DENSITY} = \frac{9.81pF}{16486um^2} = 0.60 \text{ fF}/um^2 \quad [2.5]$$

$$D_{LUMPED_CAP_DENSITY} = \frac{8.49 pF}{9801 \mu m^2} = 0.87 \frac{fF}{\mu m^2} \quad [2.6]$$

Despite the slightly larger capacitance per unit area calculated for the Lumped Capacitor, the Distributed Capacitor has significantly less series resistance, making it the better choice for any application requiring high Q capacitors such as a Wilkinson Power Divider/Combiner.

SCAI Characterization

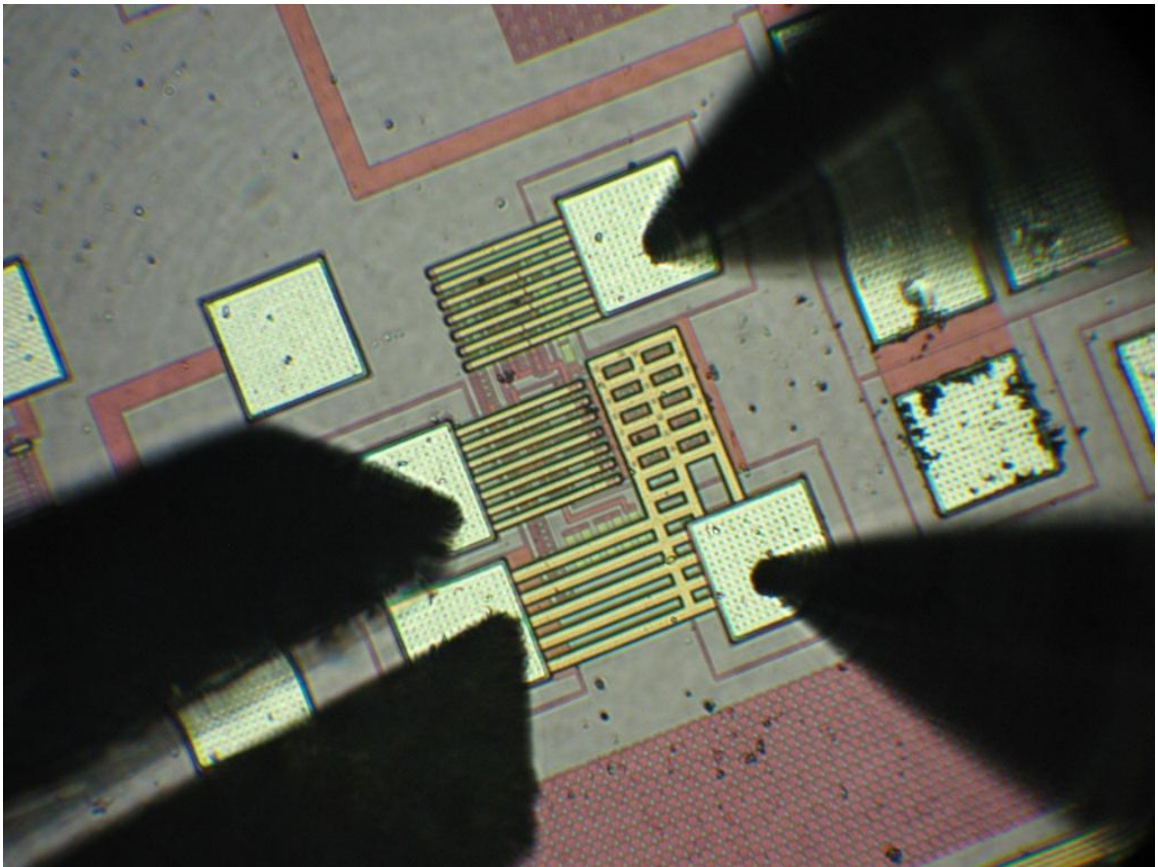


Figure 2.18: Bobcat_V0 SCAI Experiment One

Figure 2.18 shows SCAI experiment one available on Bobcat_V0. This experiment requires only a power and ground connection, while the second (not shown)

requires off chip resistors that provide reference currents used to properly bias the SCAI.

In the second experiment the reference currents can be changed to characterize the relationship between bias current and effective impedance.

Ideal power supplies were assumed during the design process and subsequently the negative effects of a poor RF ground were not observed in simulation. This false assumption and inadequate power supply modeling became very apparent when initial measurements showed a large deviation from simulation based predictions. To mitigate the lack of a decent RF ground, a bias-T network was connected between the two supply probes approximately 1.5” from the SCAI supply pads effectively providing a near ideal RF short. At frequencies greater than 500MHz, the electrical distance from the SCAI to RF short becomes significant and transmission line effects begin to impact the quality of the RF ground. Subsequent designs should include on-chip decoupling capacitors to provide an adequate RF ground as close to the SCAI as possible.

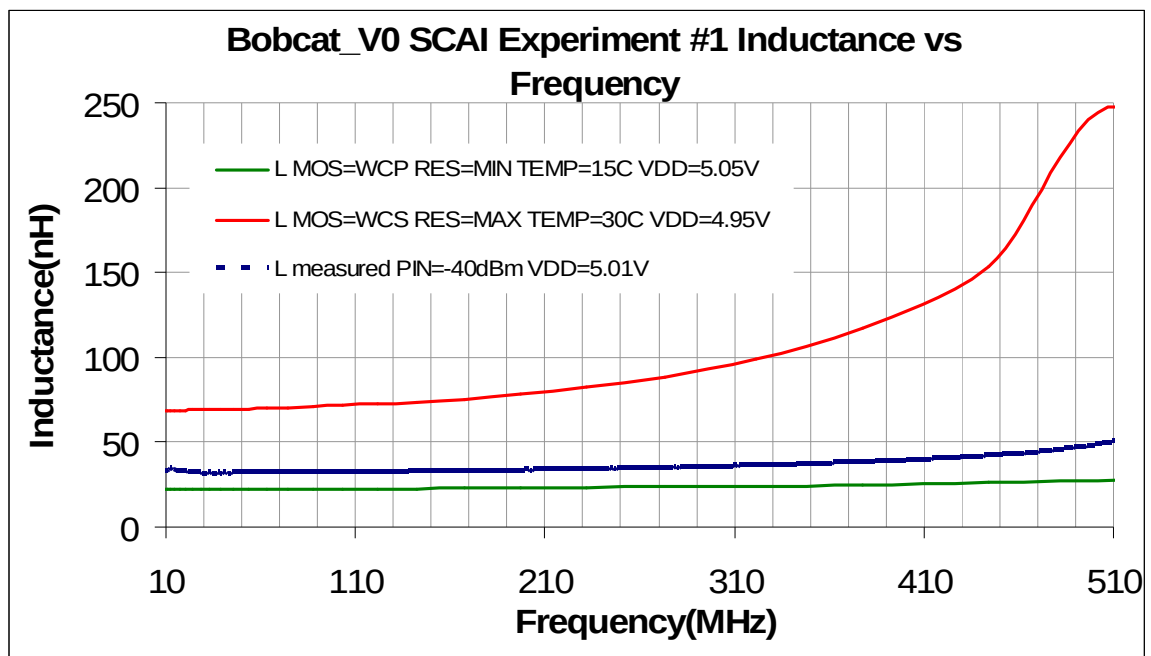


Figure 2.19: Bobcat_V0 SCAI Experiment One Inductance Vs Frequency

Figure 2.19 shows the inductance for the two bounding simulated corners in addition to the measured results. After the addition of the bias-T network between supply probes, the measured inductance falls well within the range predicted by simulations at frequencies below 500MHz, but transmission line effects associated with an inadequate RF ground adversely affect results at higher frequencies. At 250MHz an inductance of 34.3nH is measured which, corresponds to 53.93 Ω of reactance.

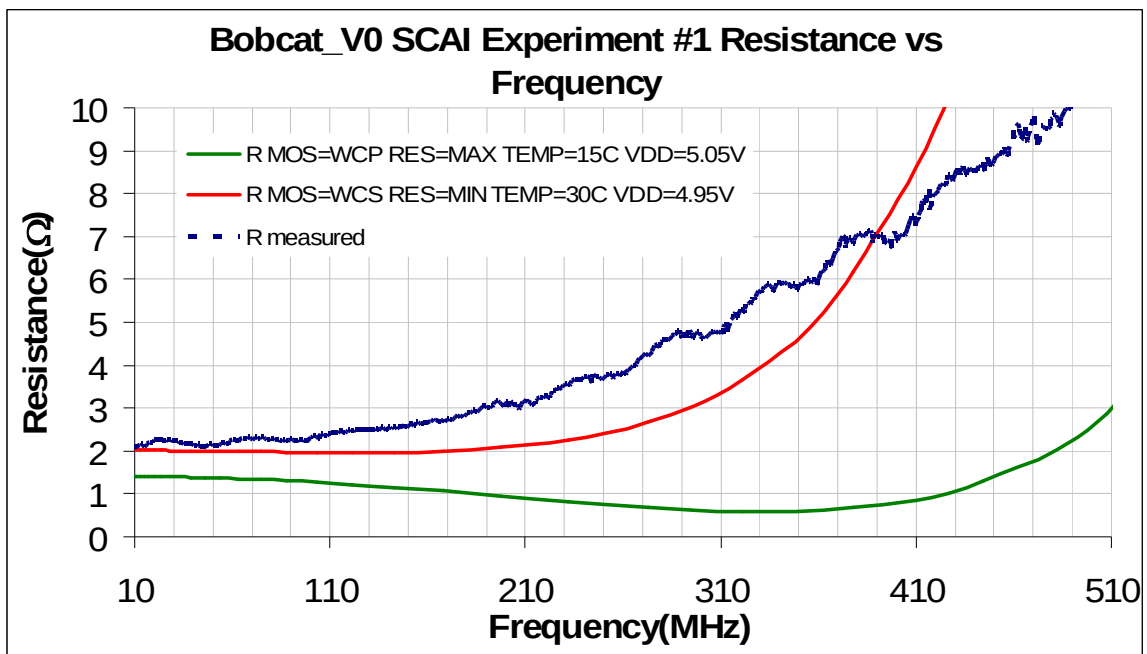


Figure 2.20: Bobcat_V0 SCAI Experiment One Resistance Vs Frequency

Figure 2.20 shows the resistance for the two bounding simulated corners in addition to the measured results. The measured results, which fall slightly outside the predicted range, have been manipulated to account for the resistive contribution of the measurement network shown in Figure 2.5 and Figure 2.7. At 250MHz, a series resistance of 3.7 Ω is measured which can be used in combination with the measured reactance of 53.93 Ω to calculate a $Q = 14.6$. A portion of the unpredicted series

resistance may be attributed to an insufficient RF ground connection in the measurement setup and/or inaccuracies in the linearized small signal model used during Spectre AC analysis to generate the simulated corner curves.

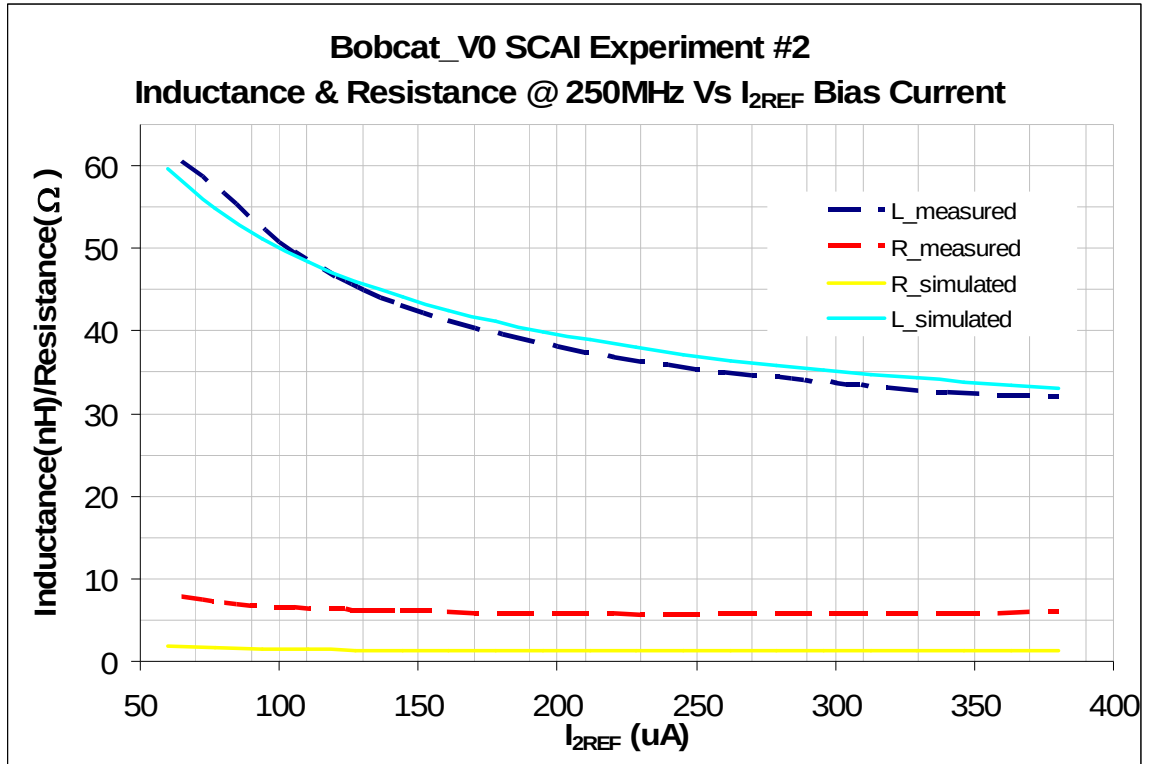


Figure 2.21: Bobcat_V0 SCAI Experiment Two
Inductance (L) and Resistance (R) Vs Frequency

Figure 2.21 shows the measured and simulated relationship between L and the I_{2REF} bias current. Simulations were run at the nominal process corner, 27°C, $V_{DD} = 5.0V$. Both measurements and simulations show a weak relationship between Resistance and I_2 bias current however these measurements show significantly more resistance than observed in SCAI_EXP1 Figure 2.21 and in simulations. Capacitive coupling between the DC probe used to provide the off-chip bias connection and the RF probe and an inadequate RF ground connection on the test setup may be the cause of this additional measured resistance. The important thing to note is the strong relationship between

inductance and the I_2 bias current as well as the weak relationship between resistance and I_2 bias current. These relationships imply the inductance of the SCAI can be controlled somewhat independent from the resistance.

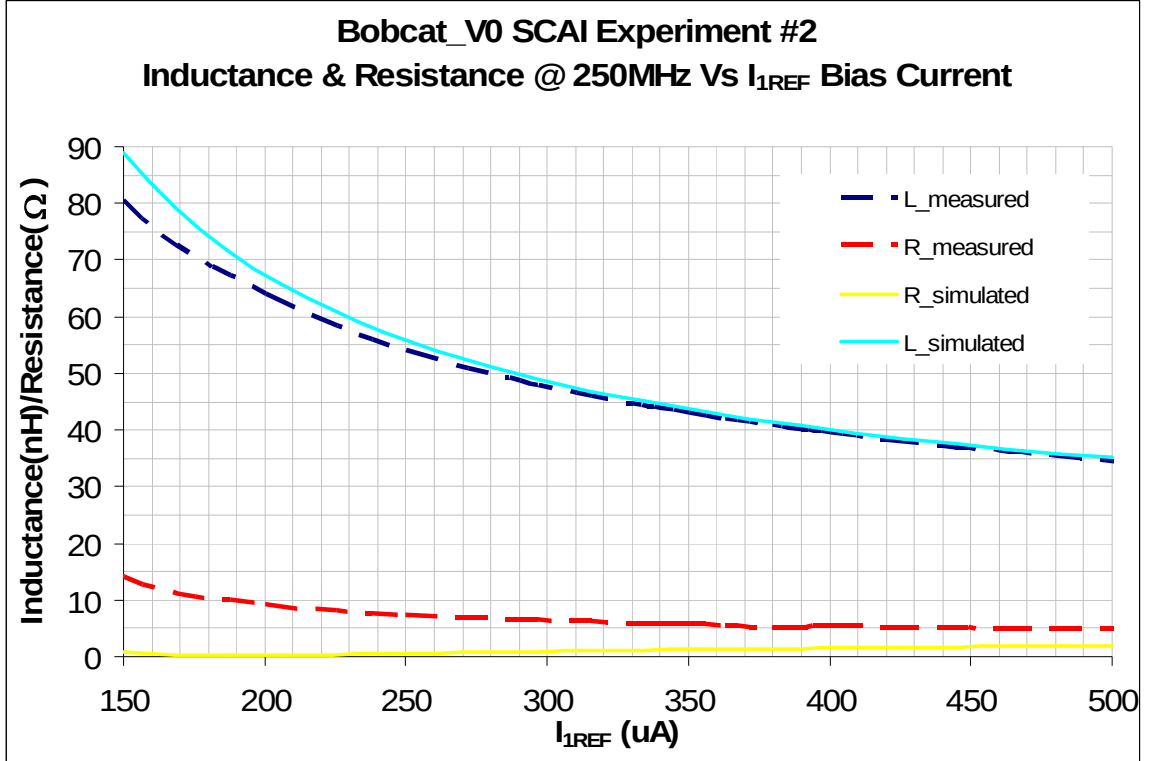


Figure 2.22: Bobcat_V0 SCAI Experiment 2 Inductance and Resistance Vs Frequency

Figure 2.22 shows the measured and simulated relationship between L and the I_{1REF} bias current. Simulations were run at the nominal process corner, 27°C , $V_{DD} = 5.0\text{V}$. Both measurements and simulations show a weak relationship between resistance and I_{1REF} bias current. However, like the I_{2REF} characterization in Figure 2.21, the measurements show much more resistance than observed in AI_EXP1 Figure 2.20 and predicted by simulations. Again, this can be attributed to capacitive coupling between the bias connections and off-chip resistors and inadequate RF ground connections on the

test setup. The important thing to note is the strong relationship between inductance and the I_1 bias current and weak relationship between resistance and I_1 bias current. These relationships confirm the inductance of the SCAI can be controlled independent from the resistance.

Wilkinson Characterization

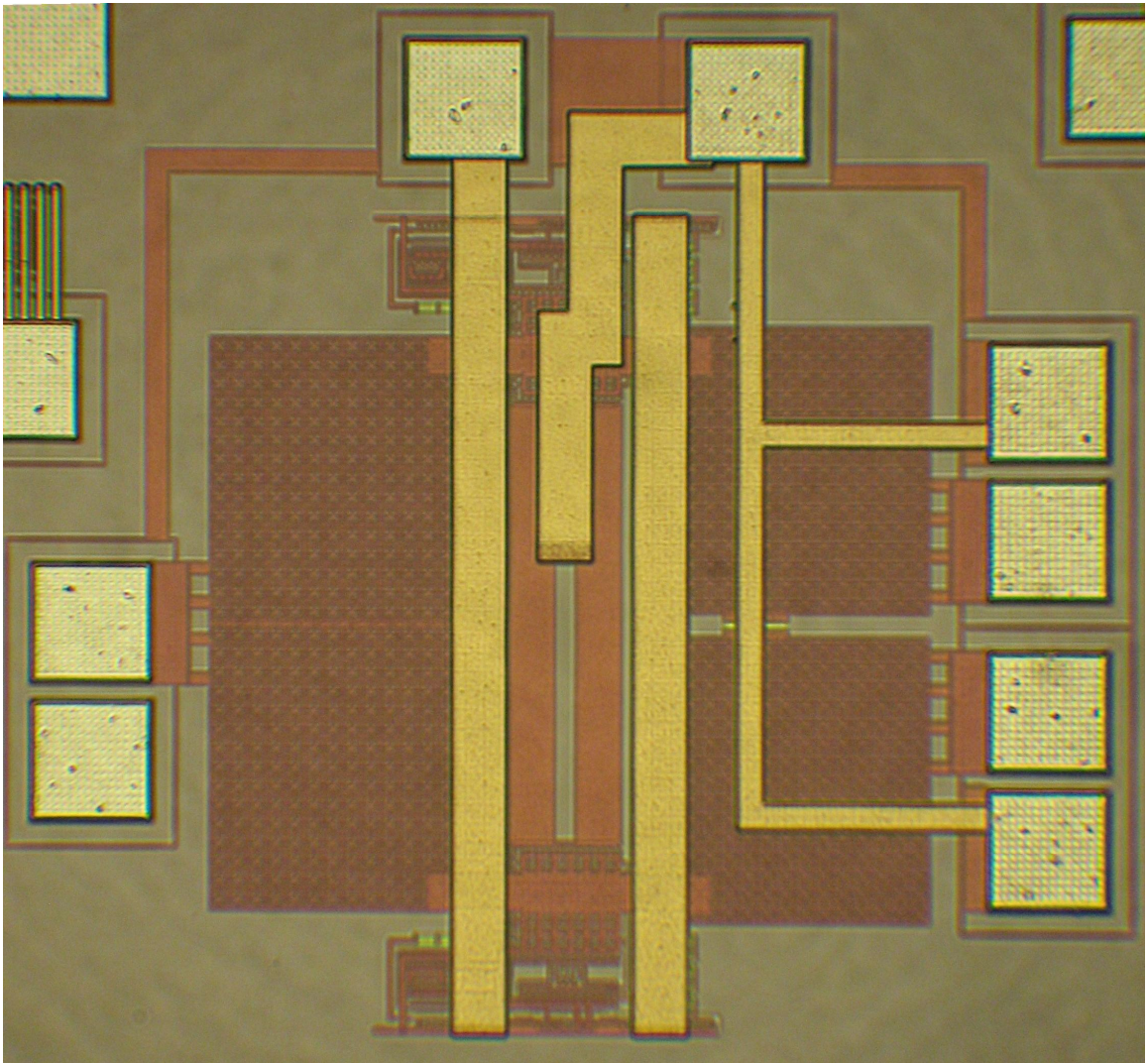


Figure 2.23: Bobcat_V0 250MHz Lumped Wilkinson Experiment

Figure 2.23 shows the 250MHz Lumped Wilkinson experiment available on Bobcat_V0. The upper left pad provides power (V_{DD}) while the upper right pad provides ground (V_{SS}). The pair of pads on the lower left provide an RF connection to Port 1 while the upper right and lower right pairs of pads provide RF connections to Port 2 and Port 3 respectively. Bias currents for the embedded SCAI are developed on chip with diffusion resistors similar to SCAI experiment one. Three RF probes are used in unison to measure the S-parameters associated with this three port network.

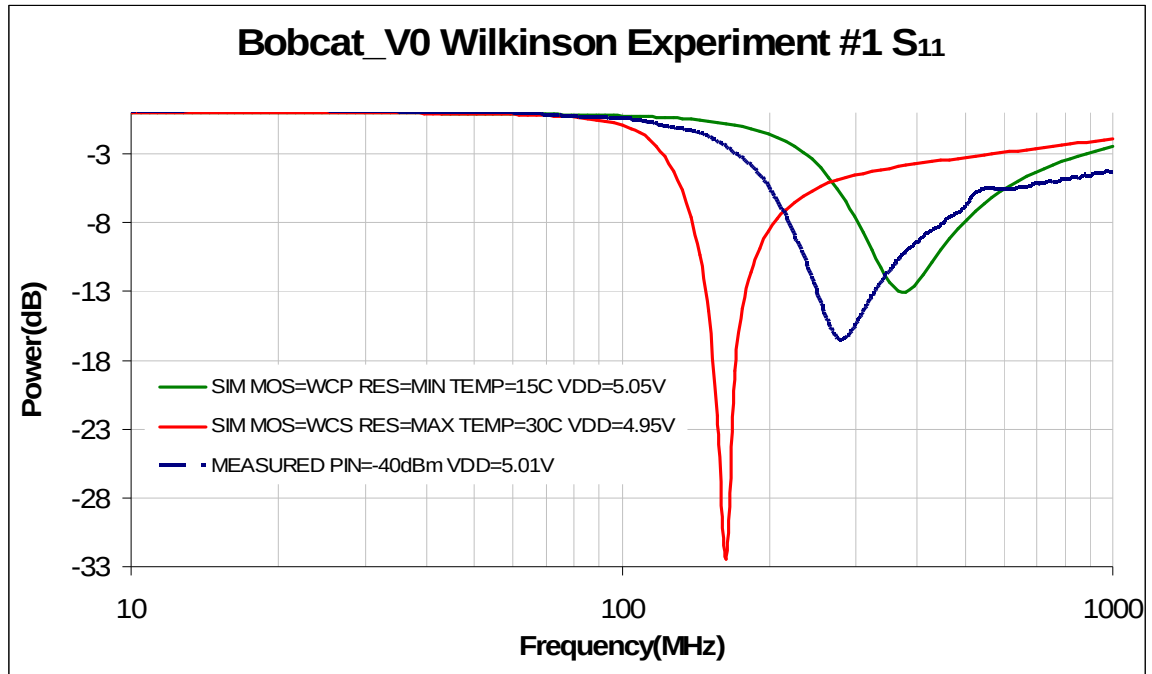


Figure 2.24: Bobcat_V0 Wilkinson Experiment 1 S₁₁ Vs Frequency

Figure 2.24 shows the reflection coefficient (S_{11}) for the two bounding simulated corners in addition to the measured results for the first Wilkinson experiment. In this experiment, the current references are implemented on-chip, and only a power and ground connection is required. The measured results fall within the range defined by the

simulated corners. Again it is important to note the variability in the S_{11} parameter predicted by simulations, which shows the need for active control of the SCAI.

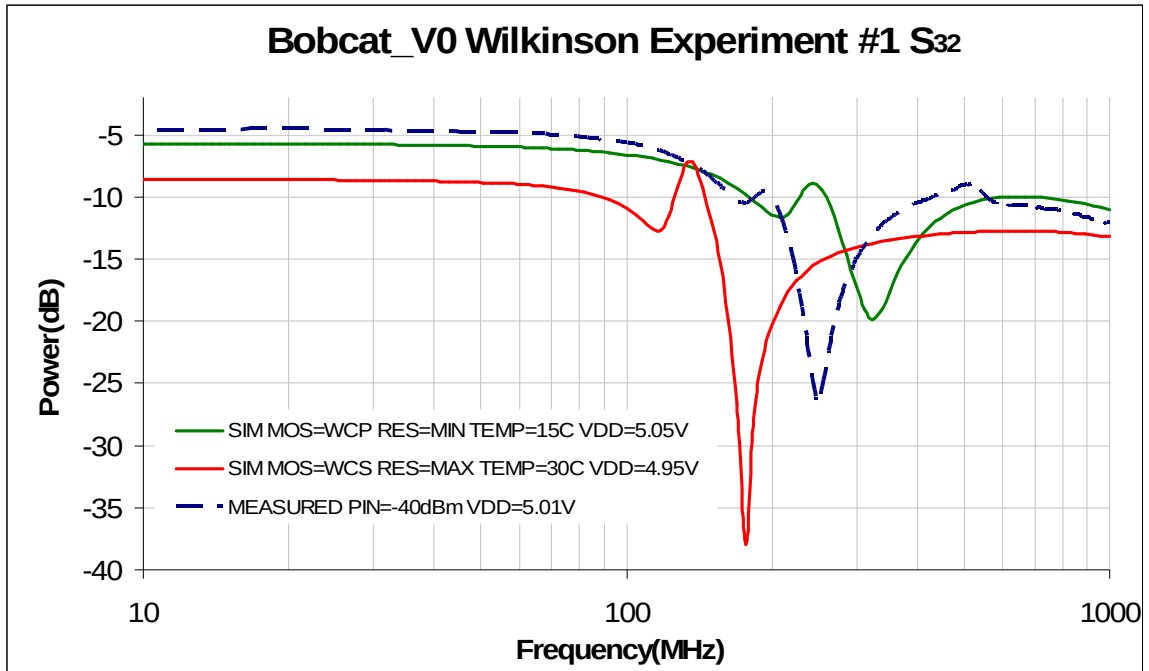


Figure 2.25: Bobcat_V0 Wilkinson Experiment 1 S_{32} Vs Frequency

Figure 2.25 shows the isolation coefficient (S_{32}) for the two bounding simulated corners in addition to the measured results for the first Wilkinson experiment. The frequency of maximum isolation as well as magnitude is well bounded by simulation. It is important to note that variability in the S_{32} parameter predicted by simulations indicates a need for active control of the SCAI.

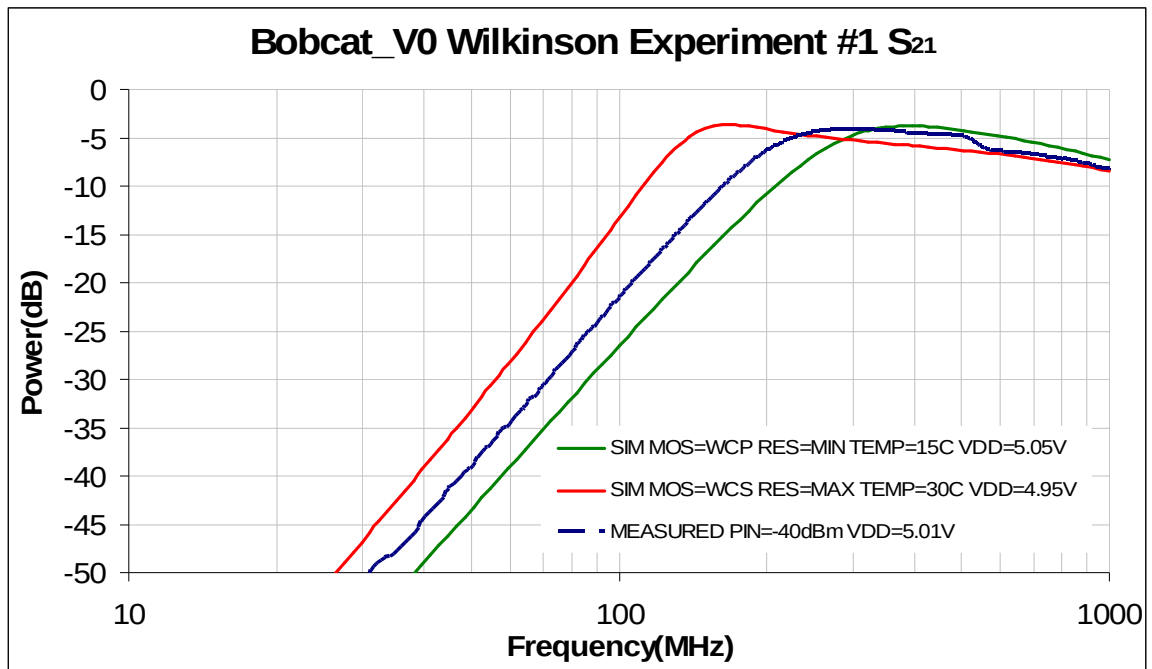


Figure 2.26: Bobcat_V0 Wilkinson Experiment 1 S_{21} Vs Frequency

Figure 2.26 shows the transmission coefficient (S_{21}) for the two bounding simulated corners in addition to the measured results for the first Wilkinson experiment. The magnitude of S_{21} and the frequency at which the peak value of S_{21} occurs is bounded by simulations. It's important to note that variability in the S_{21} parameter predicted by simulations implies the need for active control of the SCAI.

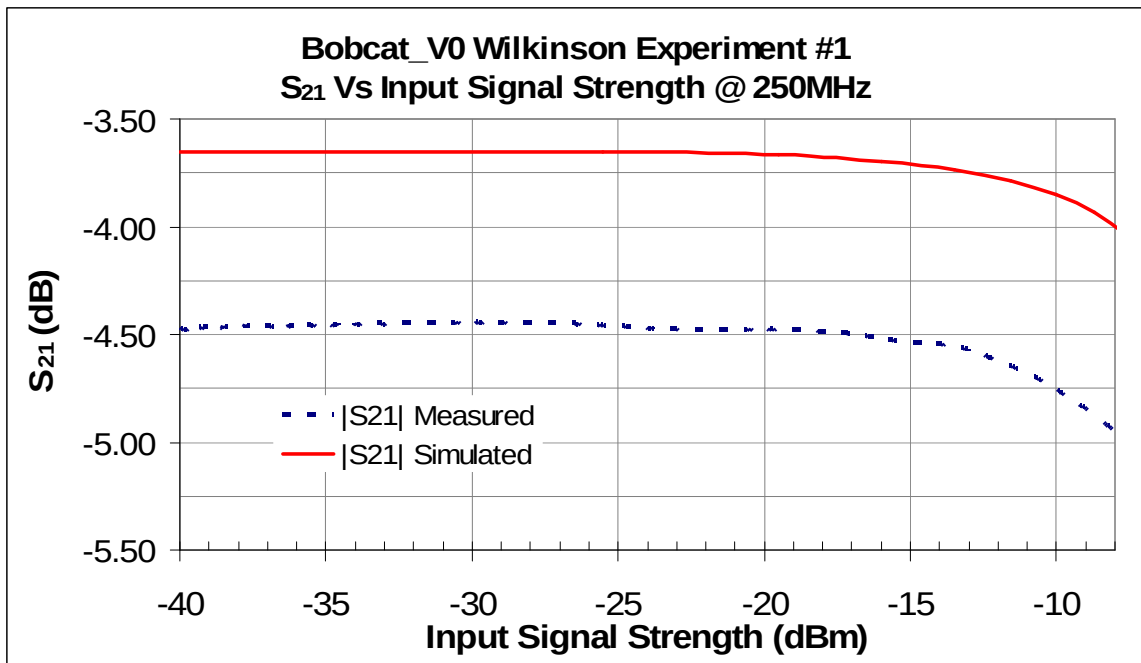


Figure 2.27: Bobcat_V0 Lumped Wilkinson Experiment
 S_{21} Vs Input signal strength @ 250MHz

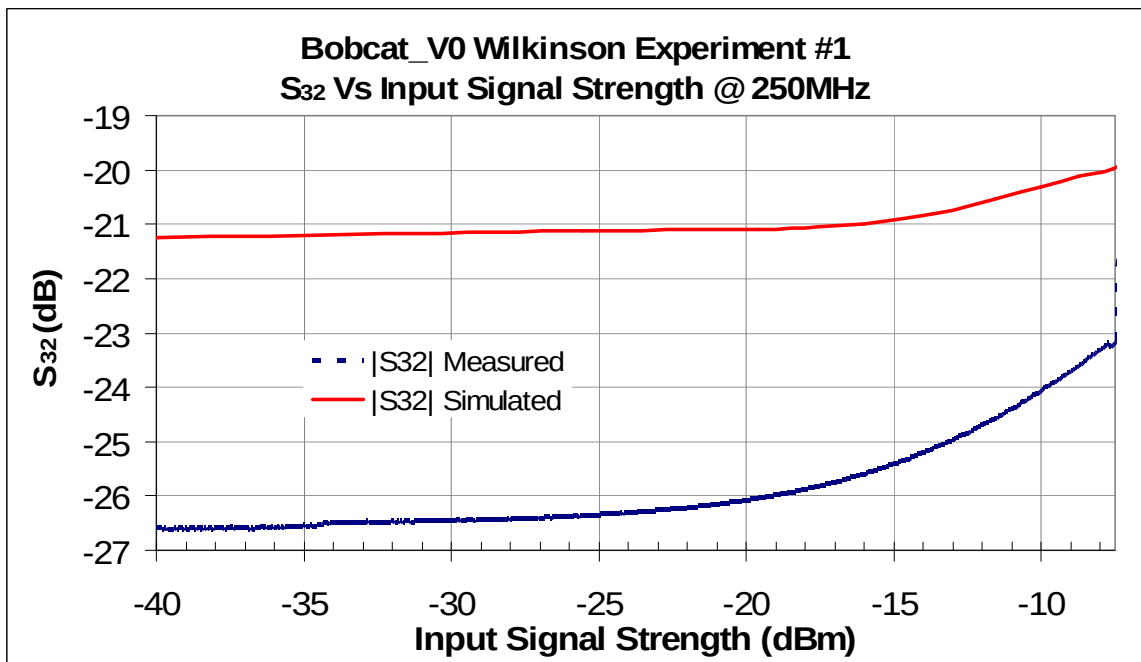


Figure 2.28: Bobcat_V0 Lumped Wilkinson Experiment
 S_{32} Vs Input signal strength @ 250MHz

The simulations and measurements of the Lumped Wilkinson Experiment depicted in Figure 2.27 and Figure 2.28 show the S_{21} transmission coefficient and S_{32} isolation coefficient both have considerable dependence on input signal strength. The dependency on input signal strength and cause of distortion will be further analyzed in the Chapter 3 section on Wilkinson Power Limitations. Simulations indicated and measurements confirmed that SCAI behavior massively deviates from ideality at signal swings greater than 75mVpp, which corresponds to an input power of -9.5dBm, but non-ideal behavior begins at power levels as low as -16dBm or 35mVpp. The input signal power/swing limitations of the SCAI shown here call to question the practicality of the SCAI in a common RFIC application.

Two-Tone Intermodulation based Harmonic Distortion is another method used to analyze signal limitations of the Wilkinson Power Divider/Combiner and SCAI. Characterization of the harmonic distortion is used to define the upper limit of the input signal strength where the active circuitry distorts the signal to a point where the quality of the fundamental tone is compromised by the 3rd harmonic.

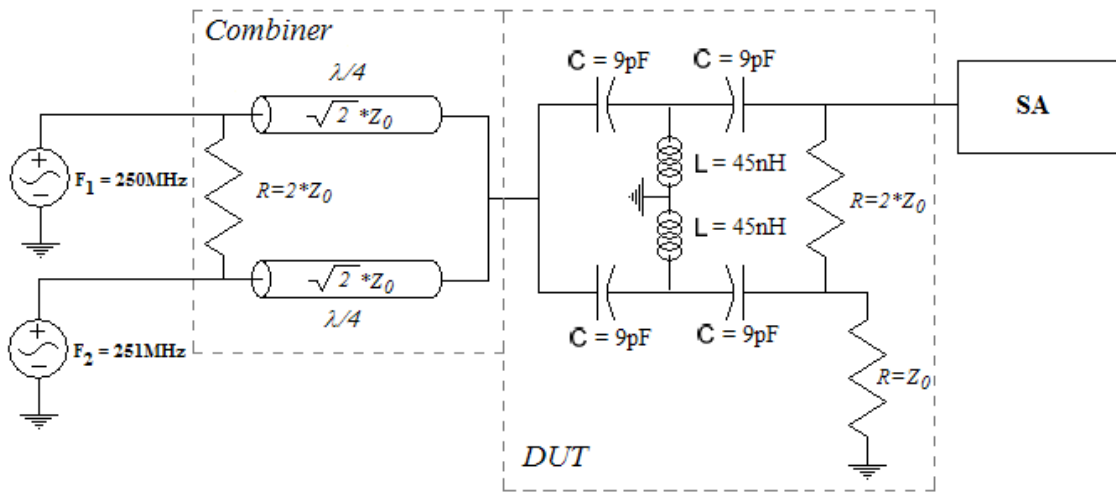


Figure 2.29: Test Setup Used To Characterize 2-Tone Intermodulation Induced Distortion

Figure 2.29 shows the test setup used to characterize the 2-Tone intermodulation-induced distortion limits of the Wilkinson with embedded SCAI. A stimulus is required, such that the input signal contains two signals of equal amplitude but slightly different frequencies. A precision power combiner can be used to combine input signals from two separate function generators while minimizing reflections and interaction between the sources. The frequencies of the two tones were set at $\pm 1\text{MHz}$ from the Wilkinson target frequency of 250MHz . Port 1 of the Wilkinson was stimulated with the output of the power combiner, and a spectrum analyzer with 50Ω load impedance was connected to Port 2 while Port 3 was terminated with 50Ω . Measurements were taken at two different power levels, -20.2dBm and -31.2dBm to ensure power levels were well below the 1dB compression point.

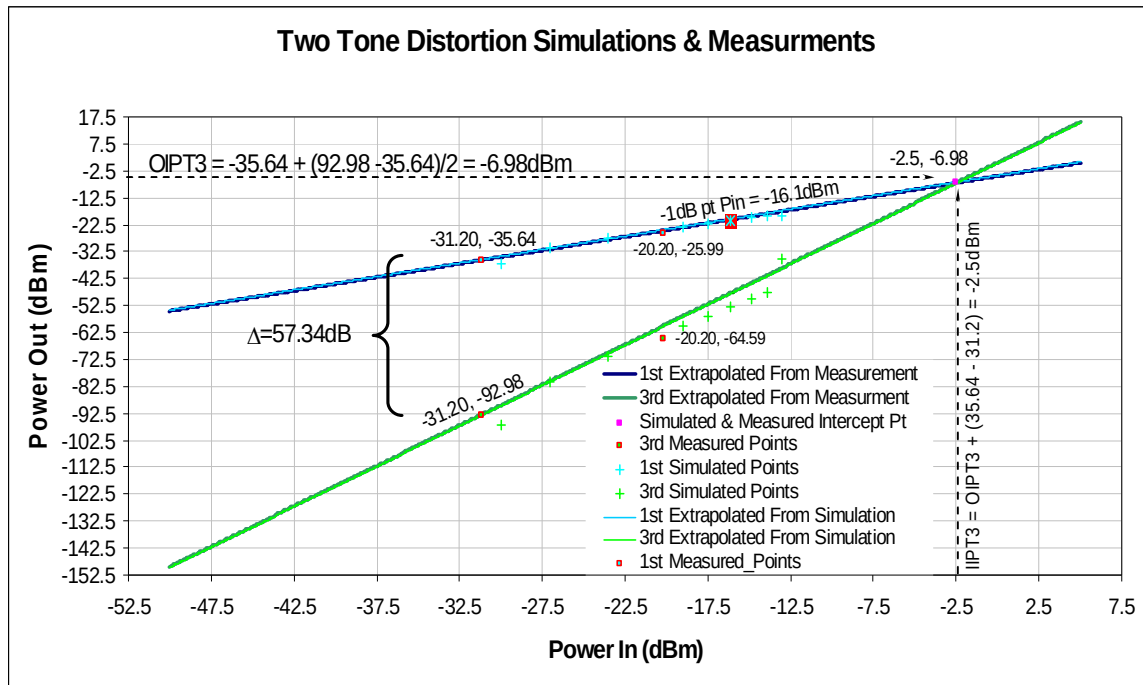


Figure 2.30: Wilkinson Primary and 3rd Harmonic Vs Input Power

Figure 2.30 shows the magnitude of the primary and 3rd harmonic as a function of input signal power. The measured data point corresponding to an input signal strength of -31.2dBm and the simulated data point corresponding to an input signal strength of -27dBm were each used to extrapolate the theoretical intercept point, assuming the primary and 3rd harmonic curves have a slope of 1dBm/dBm and 3dBm/dBm respectively. Both measured and simulated data yielded identical extrapolated theoretical intercept occurring at an input power level of -2.5dBm (167mVpp) and output power level of -6.98dBm (100mVpp).

The 1dB compression point, which is commonly used to define the upper limit of the input signal power range, is defined as the input power level at which the output power deviates from the theoretical primary power curve by -1dB. The lower limit of the input signal power range is defined by the minimum SNR of the preceding stage or circuit. Simulations indicate the -1dB compression point for this Wilkinson occurs at an input power level of -16.1dBm, which corresponds to 35mVpp.

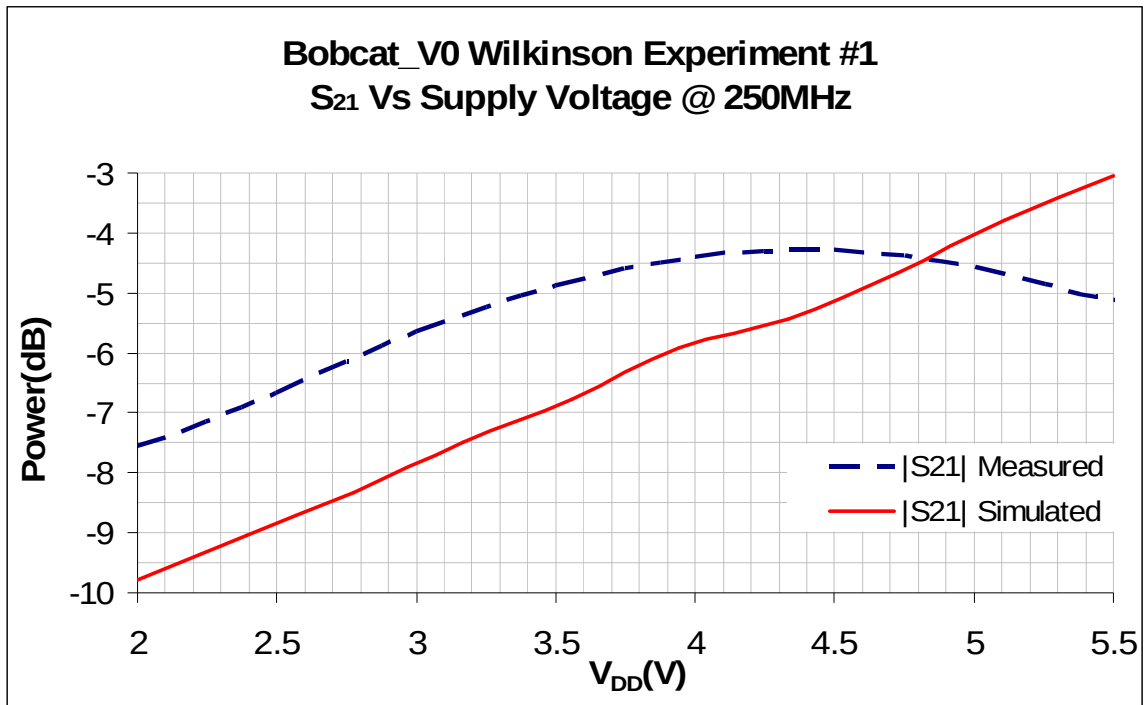


Figure 2.31: Bobcat_V0 Wilkinson Experiment
 S_{21} Transmission Coefficient Vs Supply Voltage @ 250MHz

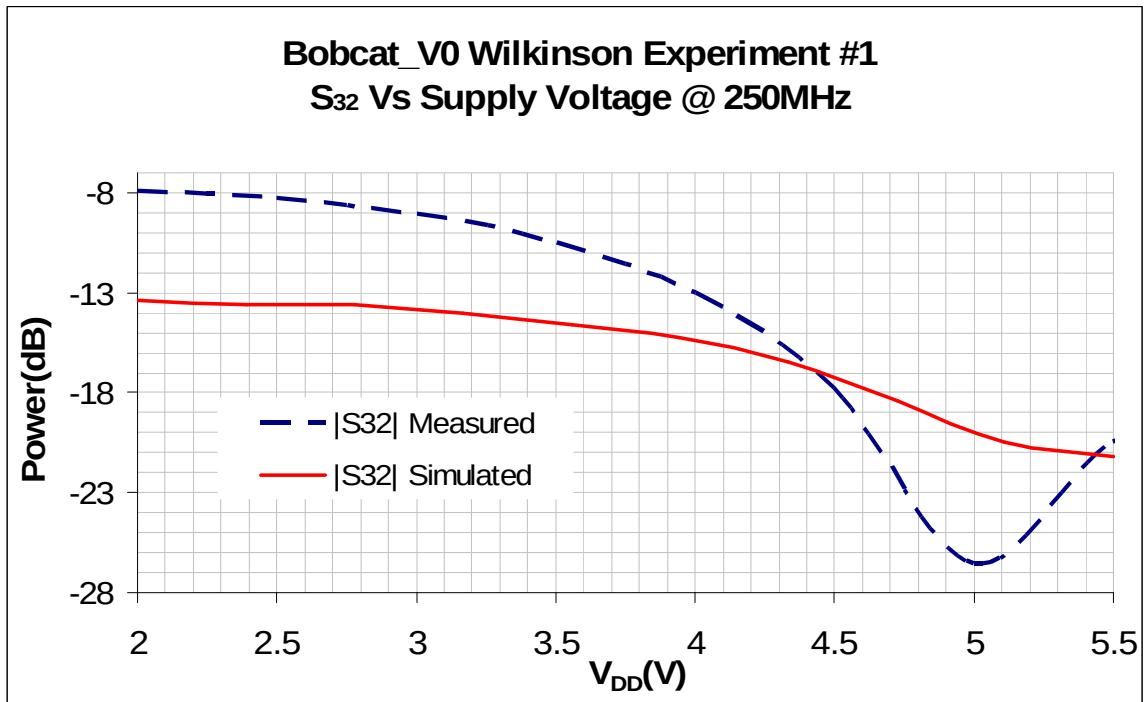


Figure 2.32: Bobcat_V0 Wilkinson Experiment
 S_{32} Isolation Coefficient Vs Supply Voltage @ 250MHz

Figure 2.31 and Figure 2.32 shows the relationship between Supply Voltage and important S-parameters like S_{21} and S_{32} . The reference current used to internally bias the SCAI is a strong function of the supply voltage. The apparent relationship between supply voltage and S-parameters is really showing the effect of a varying reference current. However, this relationship still confirms the need for active compensation of the SCAI when supply voltage variation is not well controlled.

Hardware Based Conclusions

The measurements of passive and active devices correlate well with simulations. The only discrepancies between simulations and measurements were likely caused by insufficient modeling of the power supply and power distribution network between the supply and chip or inaccuracies in the small signal linear models used during AC Spectre analysis. In general, on-chip power supply stabilization was under designed which required modification of the test setup for good model-to-hardware correlation. For future designs, the pervasive use of on-chip decoupling capacitors should provide an even better RF ground than that which resulted from the addition of the bias-T network to the test-setup. In addition, on-chip decoupling capacitors will filter power supply noise.

Bobcat_V0 was designed as a test vehicle to prove the functionality of basic components that will ultimately be used in a compensation scheme aimed at controlling the inductance of the SCAI. Bobcat_V0 successfully proved the accuracy of C5 device models, the viability of the SCAI topology for use in a common RF application, and a method for controlling the SCAI inductance via the I_1 bias current.

CHAPTER 3

ACTIVE INDUCTOR/WILKINSON COMPENSATION SCHEME

IntroductionThe Wilkinson Design Point

As discussed in Chapter 1, equations [1.3], [1.4] and [1.5] were used to determine the inductive, capacitive and resistive values for the 250MHz Wilkinson depicted in Figure 3.1.

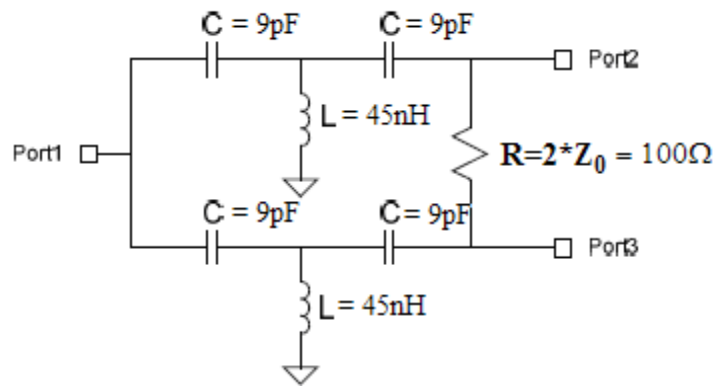


Figure 3.1: Ideal, Lumped 250MHz Wilkinson in a 50Ω System

Optimizing the Control Loop ArchitectureAvoiding Prior Issues with Control Systems

As discussed in Chapter 1, Lyson failed to achieve full success with the CPPLL compensation scheme for two main reasons:

- 1.) At signal levels greater than 75mVpp, a significant level of distortion causes the SCAI to lose its ideal inductive behavior. This implies that if a master-slave compensation scheme is used to control the SCAI, the signal swing across both master and slave must be less than 75mVpp.

- 2.) The nature of the SCAI topology sets the DC bias or V_{GS} for the amplifying transistor (M_{OSC} of Figure 1.19) in the Colpitts VCO very close to the threshold voltage of M1 in Figure 1.12. As a result M_{OSC} must be sized very large to reduce its threshold and maintain sufficient gain and signal swing at the VCO output. To further complicate matters, the current source (M_{BIAS} of Figure 1.19) must be sized large to minimize the V_{DS} required to maintain operation in the saturated region. The combination of the large size of M_{OSC} and M_{BIAS} adds a significant amount of parasitic capacitance which can dominate the resonant frequency of the VCO.

Minimizing Systematic Offsets Between Master & Slave Elements

Assuming all environmental conditions (process, local supply voltage and local temperature) are equal, it makes sense that systematic offset in a master slave control system can be minimized if the master and slave elements experience the same electrical environment in terms of input signal amplitude/frequency and output load. Since the ultimate goal of this research is to design an on-chip Lumped Wilkinson that is tuned to 250MHz and uses a controlled SCAI as the inductive component, the master control loop should somehow incorporate a Wilkinson or Wilkinson-like structure to minimize systematic offset. This implies monitoring one of the many transmission or reflection characteristics of the Wilkinson and compensating the SCAI appropriately. Monitoring a reflected waveform from a multi-port network without corrupting the waveform during measurement requires a directional coupler, but monitoring a transmitted signal is much a

much simpler task. From a high level, a control loop used to monitor and compensate a specific Wilkinson transmission characteristic might function as depicted in Figure 3.2.

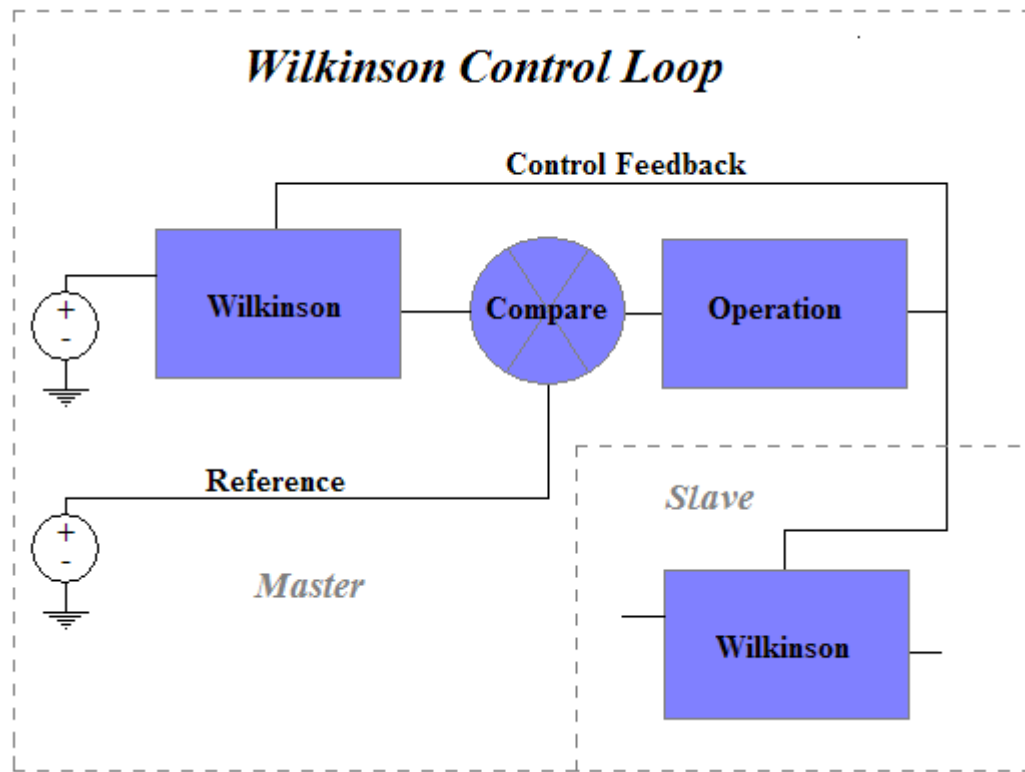


Figure 3.2: SCAI Control System Diagram

- 1.) A stimulus is applied at one port and the resulting waveform is observed at another port.
- 2.) Some characteristic of this waveform is compared to a reference and an error signal is issued based on the comparison.
- 3.) A control voltage or current is changed appropriately, based on the error signal.

Selecting the Measured Variable

Three sets of criteria should be evaluated when selecting the optimal measurement variable in a control loop.

- 1.) The variable should be selected such that the measurement process does not corrupt the result.
- 2.) The controlled and measured variables should have a linear, first-order relationship.
- 3.) Second-order relationships between the controlled and measured variables should be minimal.

The first step is to determine which of the Wilkinson transmission coefficients (S_{12} , S_{13} , S_{21} , S_{23} , S_{31} , or S_{32}) can be accurately monitored such that the measurement does not adversely influence the results. Based on the characteristics of the lumped Wilkinson with shunt inductor (namely that it is a matched three port network), we know that ideally $S_{12}=S_{21}=S_{13}=S_{31}=-3\text{dB} \angle -270^\circ$ and $S_{32}=0$. It would be challenging to design a control loop that monitored S_{32} and controlled the Wilkinson such that the signal at the output was undetectable or below some minimum level. Even if this approach was taken, controlling the SCAI such that $S_{32} = 0$ would not necessarily yield a properly tuned Wilkinson since S_{32} can be 0 for multiple values of inductance. Clearly, monitoring one of the other transmission coefficients is the best approach.

In polar form, a transmission coefficient can be broken down into two different components, the phase and magnitude which correspond to the signal delay and gain from one port to another.

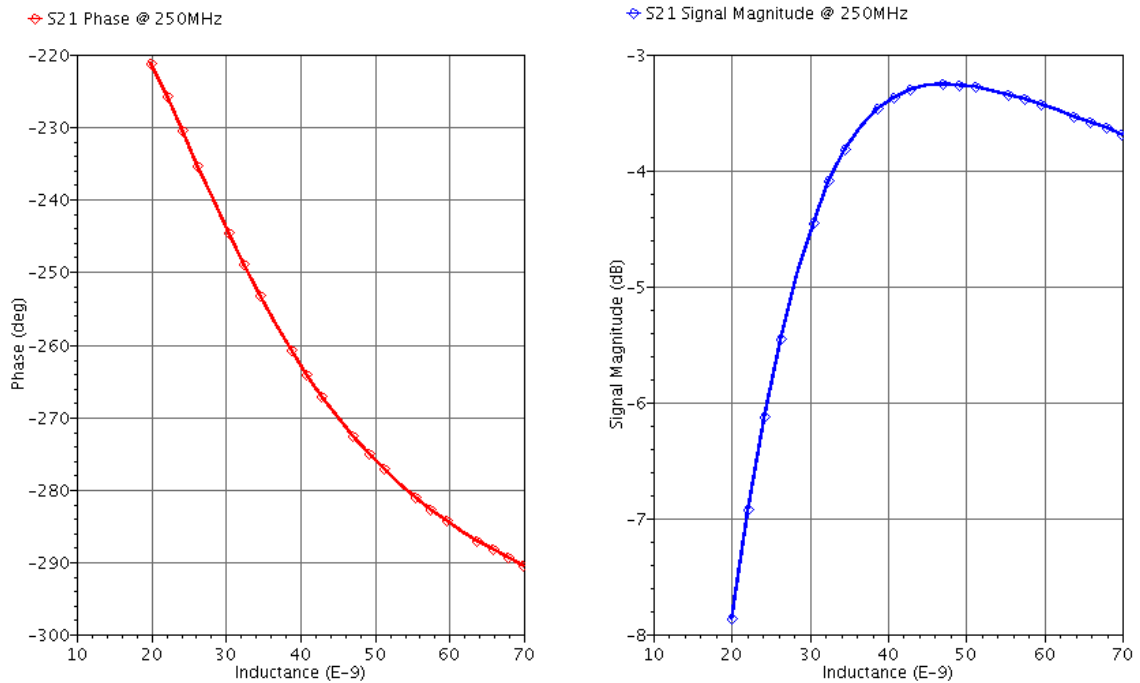


Figure 3.3: Ideal Lumped Wilkinson Signal Phase and Magnitude Vs Inductance at 250MHz

A control loop with S_{21} magnitude as the measured variable would compare the peak amplitude between two cycles and adjust the inductance until the maximum peak amplitude was ascertained. Figure 3.3 shows the relationship between inductance and signal magnitude is non-monotonic which implies a control loop monitoring signal strength would need a well define starting point to ensure compensation in the proper direction. Figure 3.3 also shows that the phase to inductance relationship is much more linear than that of the magnitude making the phase a better candidate for the measured variable in the control loop.

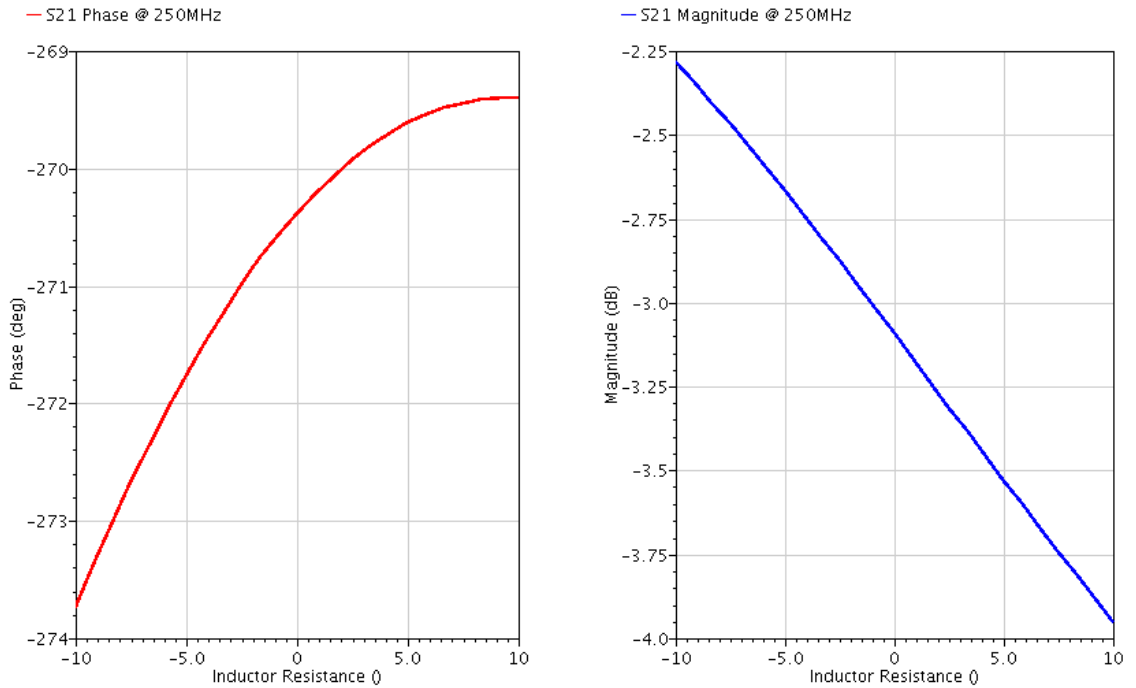


Figure 3.4: Ideal Lumped Wilkinson Signal Phase and Magnitude Vs Inductor Resistance at 250MHz

Every lumped inductor has a finite amount of series resistance which results in deviation from ideal behavior. This non-ideality is quantified by Quality Factor (Q) as discussed in Chapter 1. When designing the SCAI, a design approach is taken such that the absolute value of the series resistance is minimized across the defined PVT, space thereby maximizing the Quality of the inductor. Despite attempts to minimize the resistance, there will be inherent positive and negative variation. While resistance is not the controlled variable, its effect on the measured variable needs to be understood and minimized. Figure 3.4 shows a strong and linear relationship between signal magnitude and resistance but a very weak relationship between the phase and resistance. Monitoring and controlling the phase shift between Port 1 and Ports 2 or 3 is clearly the most intuitive approach due to the strong linear relationship between inductance and phase as

well as the weak relationship between resistance and phase shown in Figure 3.3 and Figure 3.4.

The Wilkinson Phase Lock Loop

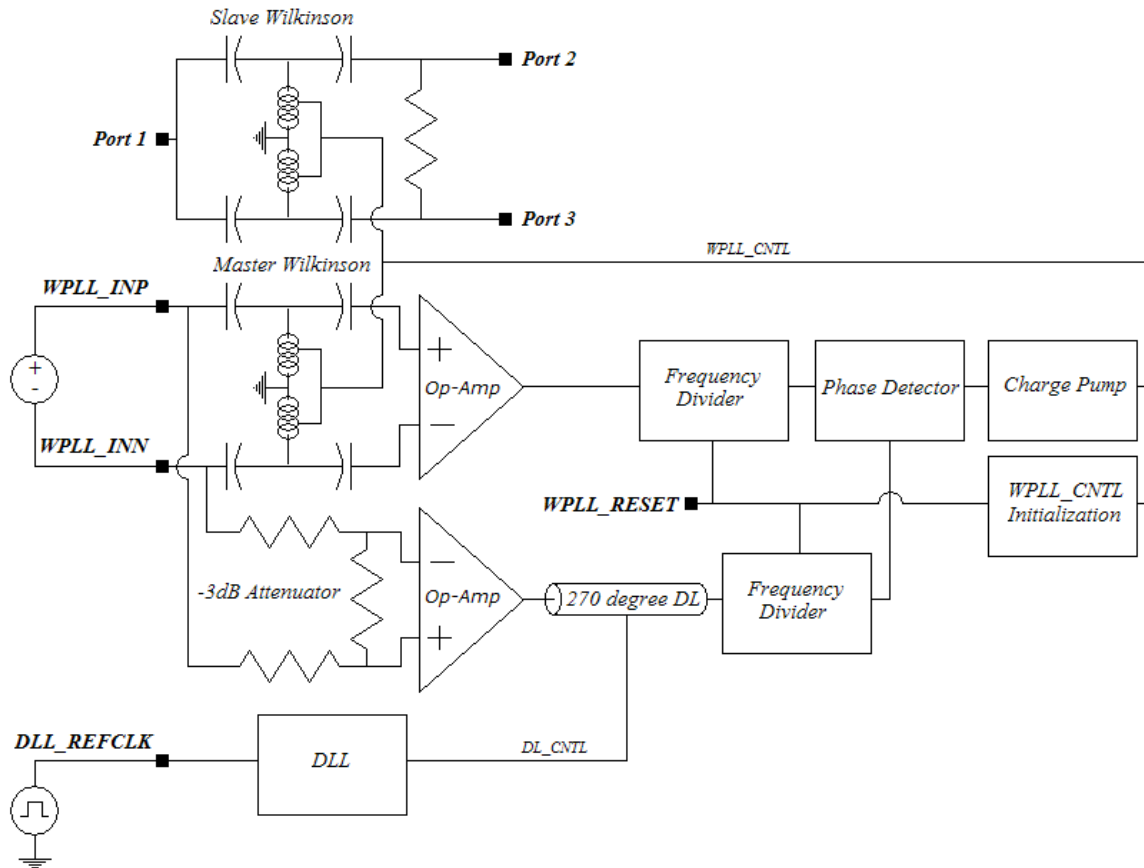


Figure 3.5: WPLL Schematic Flow Chart

Figure 3.5 shows a high level schematic for a proposed control loop to monitor and control the phase of a Wilkinson-like structure by adjusting the bias current and thereby, inductance of embedded SCAI. This control loop will be referred to as a Wilkinson Phase Lock Loop (WPLL). This control approach requires manipulation or amplification of the relatively small signal propagating through the Wilkinson to a rail to rail signal that can be used as an input to a digital phase detector. Unfortunately, as soon

as signal amplification is introduced, distortion becomes a major concern. Two methods for canceling the effect of distortion are employed to ensure that both the signal at the master Wilkinson output and the Phase Detector (PD) reference signal are distorted by the same amount. As discussed in Chapter 1 and Chapter 2, the non-ideal SCAI behavior or distortion at larger signal levels implies the smallest possible signal level should be used as a reference for the master Wilkinson. While the AMIS C5 technology is inexpensive, the device performance is also relatively poor. These technology constraints make it challenging to design an amplifier with enough bandwidth and a sufficient edge rate to amplify a very small, single-ended signal to a rail- to-rail signal across the entire PVT space. Amplifier distortion caused by this small input signal amplitude can be minimized by modifying the master Wilkinson to present a differential signal, effectively doubling the signal strength at the inputs of the amplifiers. To achieve this, the master Wilkinson must be modified by removing the $2 \cdot Z_0 = 100\Omega$ termination between Ports 2 and 3 and breaking the connection at Port 1. This effectively creates two 2 Port networks each consisting of an LC filter with a differential stimulus applied between the two input ports. As depicted in Figure 3.5, I'll define this differential network to be called a $\frac{1}{2}$ Wilkinson. It's important to note that this modification to the master Wilkinson drastically changes the impedance looking into both input and output ports, but the parameter of interest S_{21} remains unchanged. To match and cancel any remaining distortion differences between the two amplified signals, the signal amplitude at the amplifier inputs must be matched so the reference signal must be attenuated by the same amount as the output of the master $\frac{1}{2}$ Wilkinson. A purely resistive, 3dB attenuator is

inserted before the reference amplifier in parallel with the master $\frac{1}{2}$ Wilkinson to serve this purpose.

Once the reference signal has been attenuated such that the signal amplitude at the inputs of both amplifiers match and both signals have been amplified from a small to rail-to-rail signal, the reference signal must be phase shifted by 270° before entering a Frequency Divider (FD). By doing this, the phase error of the master $\frac{1}{2}$ Wilkinson is equal to the phase difference between the two PD input signals. A Delay Line, tuned by a Delay Lock Loop (DLL) provides a PVT invariant 270° phase shift for the digital reference signal. At this time, it's only important to understand the purpose of the DL. The intricacies and design techniques will be discussed during the in-depth description of each control loop component. It is also important to note that because the phase error is captured in the phase difference between the two PD input signals, the actual signal delay and delay variation through the amplifiers is irrelevant. Frequency Dividers are used to divide the switching rate by 4 to 62.5MHz which is well within the frequency limitations of the PD. Finally, a control voltage initialization circuit is used to initialize WPLL_CNTL during startup. To summarize, the topology suggested in Figure 3.5 effectively stimulates a differential Wilkinson-like filter and phase aligns the output signal to a 270° phase shifted version of the input signal. The following sections describe the various functional blocks of the WPLL and develop first-order transfer functions based on the curve fitting of simulated results.

Using a Delay Lock Loop for a Phase/Time Reference

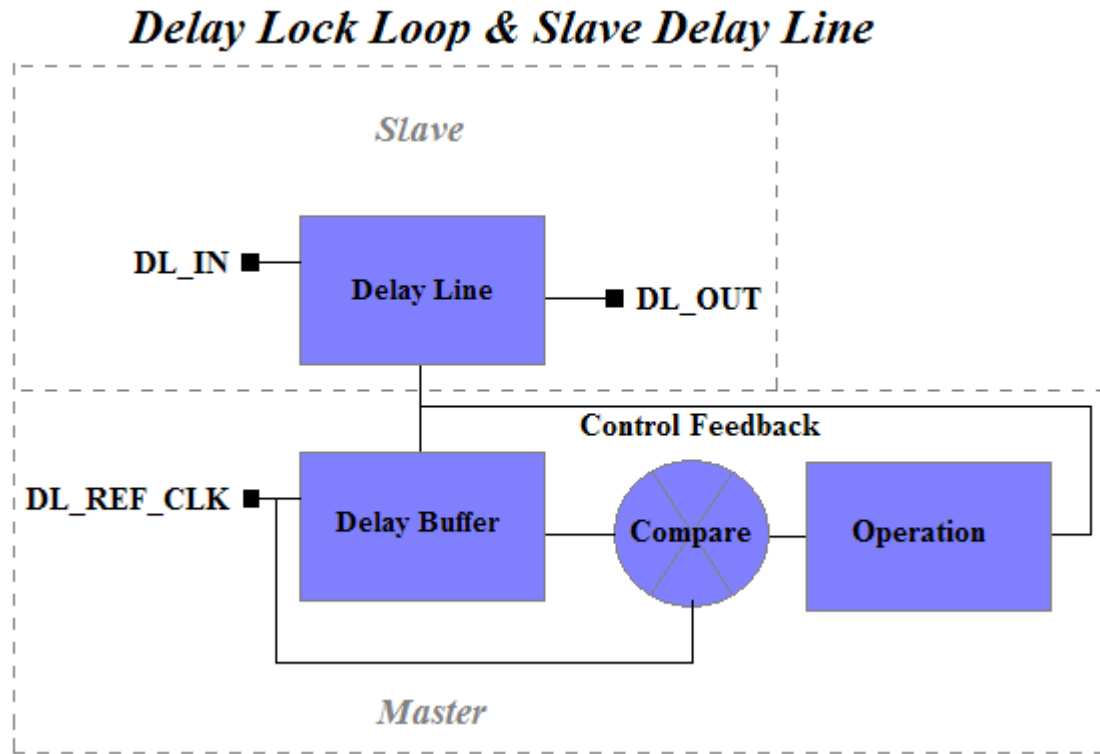


Figure 3.6: Delay Lock Loop Control System Diagram

A Delay Lock Loop (DLL) phase aligns a digital output signal to a digital reference clock by adjusting the propagation delay through the buffer until $T_{\text{BUFFDEL}} = K \cdot T_{\text{REFCLK}} = K / F_{\text{REFCLK}}$. Depending on how the DLL is designed, $K \geq 1$; but to minimize the size of the DLL, I selected $K = 1$. To minimize coupling between the DLL and WPLL control loops, the DLL input reference frequency is set to 100MHz which is within the frequency limitations of the PD and CP. A high-level control diagram of the DLL is depicted in Figure 3.6.

Figure 3.7 shows a high-level schematic of the delay lock loop (DLL). The Delay Line (DL) and Delay Buffer (DB), shown in detail in Figure 3.8, are simply a chain of delay controlled inverters. The compare function is implemented with a Phase Detector (PD), which provides an error signal to a Charge Pump (CP). The CP operates on a control voltage, increasing or decreasing the propagation delay through the DB and DL respectively.

The Delay Buffer:

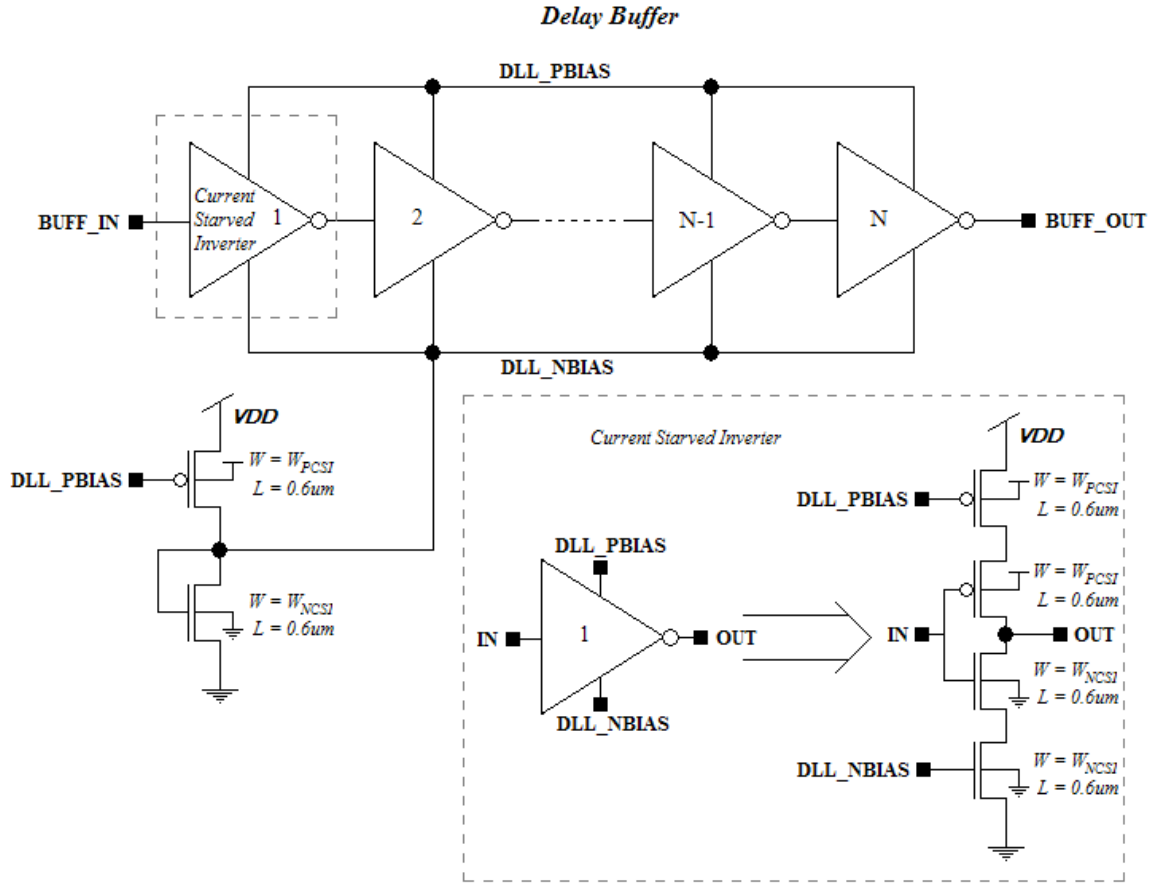
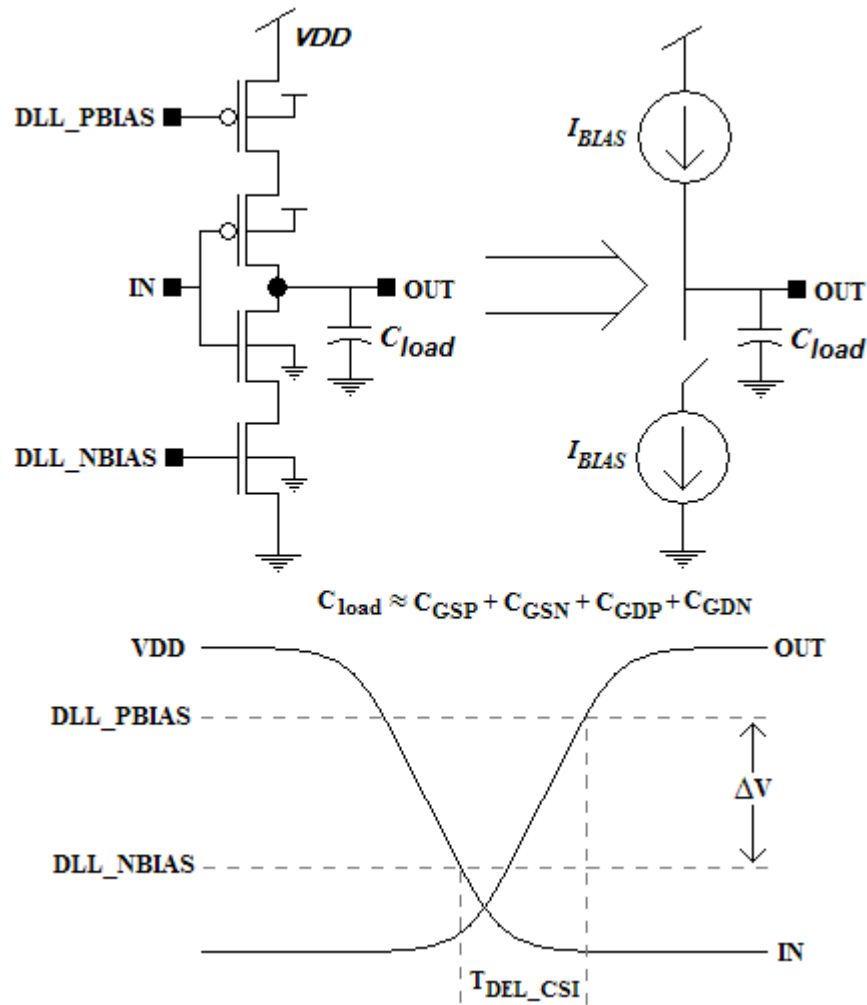


Figure 3.8: DLL Delay Buffer Schematic

A DLL can be implemented using a number of methods, I choose the analog approach to maximize accuracy or minimize tolerance/jitter in the time reference [13]. This approach uses a delay buffer constructed of N Current Starved Inverters (CSI), as depicted in equation [3.1], where $T_{DLL_REF_CLK}$ is the period of the DLL reference signal and T_{DEL_CSI} is the signal propagation delay through one CSI stage.

$$N = \frac{T_{DLL_REF_CLK}}{T_{DEL_CSI}} \quad [3.1]$$

Each CSI consists of an inverting pair of transistors with current controlling PMOS and NMOS devices connected to each source. Control voltages on the gates of the current starving devices are used to adjust the transient current through each inverting pair which in turn controls the transition rate of each stage and the total signal propagation delay through the chain as depicted in Figure 3.8. It is possible to only implement current control on the NMOS device or the pull-down to minimize parasitic capacitance, propagation delay and maximize transition rates. Under some PVT conditions this approach can result in asymmetric delays and transition rates through the CSI and Delay Buffer. When current control is implemented on only one side of the CSI, the effective strength of each side relative to the other (and therefore the transition time) changes as a function of PVT. At the expense of delay and transition rate, I choose to use current control on both sides of the inverter to minimize delay and transition rate asymmetries. The PMOS or pull-up control voltage labeled DLL_PBIAS in Figure 3.7 and Figure 3.8 is converted to an equivalent NMOS or pull-down control voltage using a current mirror and labeled DLL_NBIAS. Designing the Delay Buffer begins with the individual CSI. The ratio of current starving to inverting device area, the ratio of PMOS to NMOS device area and the absolute area of both pairs of devices were the three design parameters used to achieve the maximum CSI transition rate and minimum propagation delay.

Figure 3.9: 1st Order CSI Model

A first order approximation of the propagation delay through a single CSI stage can be made if the CSI is simplified to ideal current sources and switches, charging and discharging a lumped capacitance. Figure 3.9 shows this simplification and also depicts the input rising and output falling transition. Prior to the switching event, the input signal (IN) is at logic “1” or V_{DD} and the output signal (OUT) is at logic “0” or 0V. As node IN begins to transition and falls through DLL_PBIAS, the PMOS switch begins to conduct current. During the portion of the transition when the voltage at node IN is between

DLL_BIAS and DLL_NBIAS, both switches conduct current. As a result most of the current passes from the supply to ground and the voltage at node OUT changes very little. As node IN transitions through DLL_NBIAS the NMOS switch ceases to conduct current and OUT begins to charge at a rate $\frac{dV_{OUT}}{dt} = \frac{I_{BIAS}}{C_{LOAD}}$. When the voltage at node OUT reaches DLL_PBIAS the following stage begins to transition. The propagation delay through a single CSI stage (T_{DEL_CSI}) can be defined as the time duration between the crossing event of the voltage at node IN with DLL_NBIAS and the crossing event of the voltage at node OUT with DLL_PBIAS. This is also depicted in [3.9].

$$T_{DEL_CSI} \approx \Delta V * \frac{C_{LOAD}}{I_{BIAS}} \quad [3.2]$$

Equation [3.2] shows the basic relationship between the propagation delay through a single CSI stage (T_{DEL_CSI}), the capacitive load (C_{LOAD}), and the CSI bias current (I_{BIAS}). The capacitive load seen by each CSI stage is dominated by a combination of the gate-to-source and gate-to-drain capacitance of the succeeding stage. Using the current equation for a saturated PMOS transistor, equation [3.2] can be expanded to account for the relationship between DLL_PBIAS and I_{BIAS} .

$$\begin{aligned} T_{DEL_CSI} &\approx DLL_PBIAS * \frac{C_{LOAD}}{\frac{k_p}{2} * \frac{W}{L} (V_{SG} + V_{TP})^2} \\ &= \frac{DLL_PBIAS * C_{LOAD}}{\frac{k_p}{2} * \frac{W}{L} (V_{DD} - DLL_PBIAS + V_{TP})^2} \quad [3.3] \\ &= \frac{DLL_PBIAS * 142.4 \text{ fF}}{40 \times 10^{-6} (4.086 - DLL_PBIAS)^2} \end{aligned}$$

Equation [3.3] shows the relationship between DLL_PBIAS and T_{DEL_CSI} .

Transistor specific quantities for the C5 technology have been substituted into this equation which is also plotted in black in Figure 3.10 for accuracy comparison.

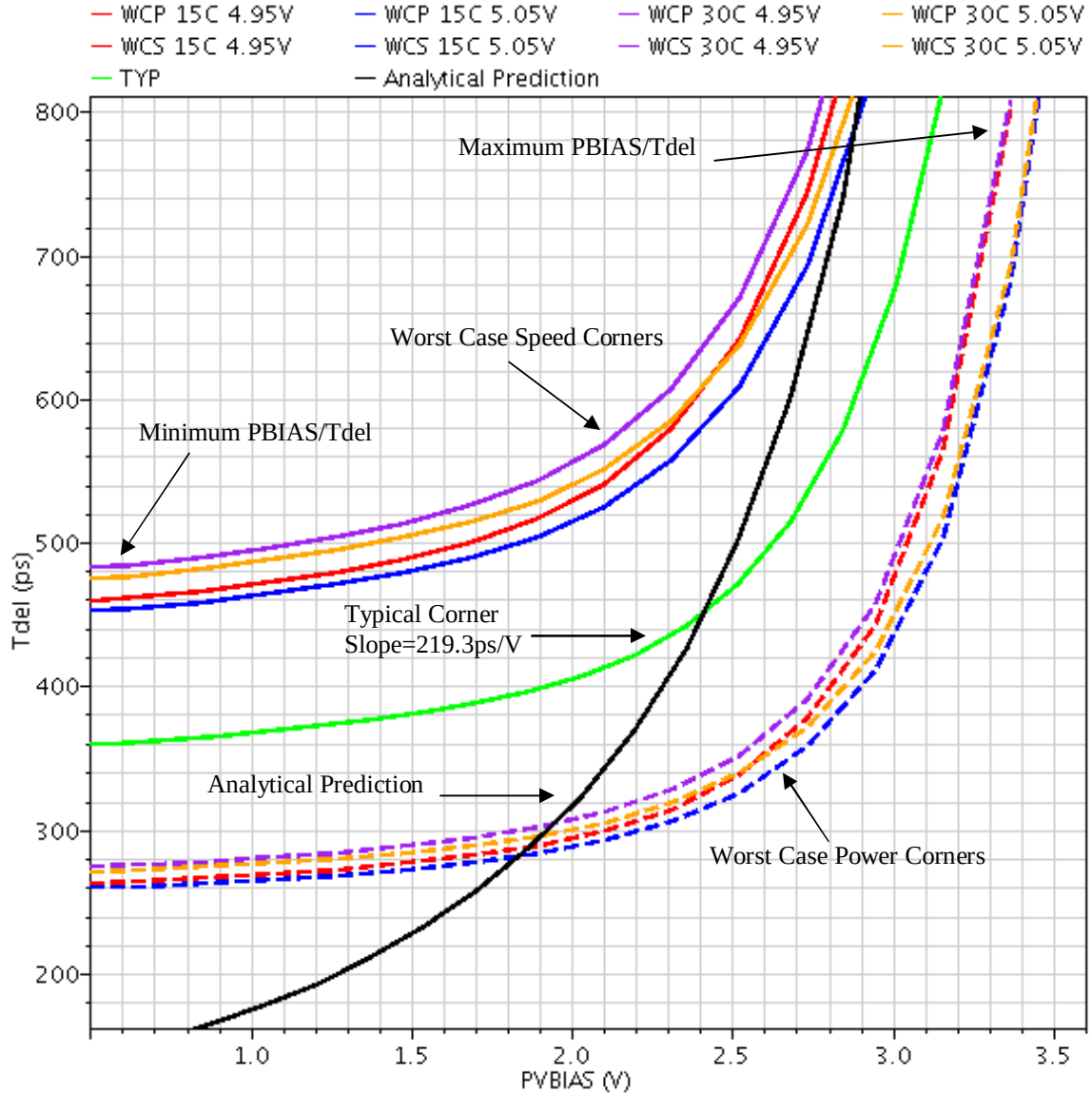


Figure 3.10: Delay of Two Series CSI Vs Control Voltage

It is advantageous to design for the fastest possible transition rate or smallest possible propagation delay to minimize error introduced by switch point variation in the subsequent stages and ultimately minimizes systematic offsets introduced by the PD. In

the DLL control loop of Figure 3.7, DLL_PBIAS is adjusted such that the delay through the chain and each CSI remains constant across the entire PVT window. Figure 3.10 shows the delay window for a pair of CSI, which is bounded by the shortest possible delay under the slowest corner, and the longest possible delay under the fastest corner. The delay of two series connected CSI is shown such that the measurement includes common edges, i.e. the delay is measured from rising to rising or falling to falling edge. At the absolute slowest corner, Worst Case Transistor Speed (WCS), Temperature = 30°C, $V_{DD} = 4.95V$, the fastest reliably achievable propagation delay through a pair of CSI ($T_{DEL_CSI_MIN}$) is 490ps/2 or 245ps. At the absolute fastest corner, Worst Case Transistor Power (WCP), Temperature=15°C, $V_{DD} = 5.05V$, the slowest reliably achievable propagation delay through a pair of CSI ($T_{DEL_CSI_MAX}$) is 800ps/2 or 400ps. While it is desirable to select a number of CSI stages, N, such that the delay through each stage is minimized and the transition rate is maximized, it is good design practice not to push a system to its limits; so I added some guard band and set $T_{DEL_CSI} = 250ps$. Figure 3.10 also confirms that the bias voltage required to achieve the desired T_{DEL_CSI} is within the voltage driving limitations of the charge pump ($V_{DD} - V_{THP} \geq V_{PBIAS} \geq V_{THP}$). It is also important to note that equation [3.3] successfully predicts T_{DEL_CSI} to the first order.

Assuming $T_{DEL_CSI} = 250ps$ and $F_{DLL_REF} = 100MHz$, a 10ns Delay Buffer consists of 40 series connected CSI. This is only true if each CSI in the chain experiences the exact same signal environment with regards to input signal characteristics and output loading. A series of simulations were conducted to determine that four additional CSI stages at the input and output of the Delay Buffer were required to ensure that the input and output transition rate is identical to that of each internal CSI, such that the entire

Delay Buffer consists of 48 series connected CSI. To compensate for the additional 8 CSI in the delay buffer, the Phase Detector reference signal is also buffered with 8 CSI as depicted in Figure 3.7.

The transfer function of the Delay Buffer operating at 100MHz is derived in equations [3.4],[3.5] and [3.6] from the $T_{\text{DEL_CSI}}$ Vs P_{BIAS} relationship depicted in Figure 3.10, assuming a linear relationship around the quiescent operating point of $T_{\text{DEL_CSI}} = 250\text{ps}$.

$$T_{\text{DEL_BUFFER}} = 20 * (219.3e^{-12} V_{\text{PBIAS}} - 77.9 \times 10^{-12}) \quad [3.4]$$

$$= 4.386 \times 10^{-9} V_{\text{PBIAS}} - 1.56 \times 10^{-9}$$

$$\phi_{\text{DEL_BUFFER}} = T_{\text{DEL_BUFFER}} * 360 * F_{\text{DLL_REF_CLK}} \quad [3.5]$$

$$= 157.68 V_{\text{PBIAS}} - 56.16$$

$$K_v(100\text{MHz}) = 157.68 \frac{^\circ}{\text{V}} \quad [3.6]$$

The Digital Phase Detector:

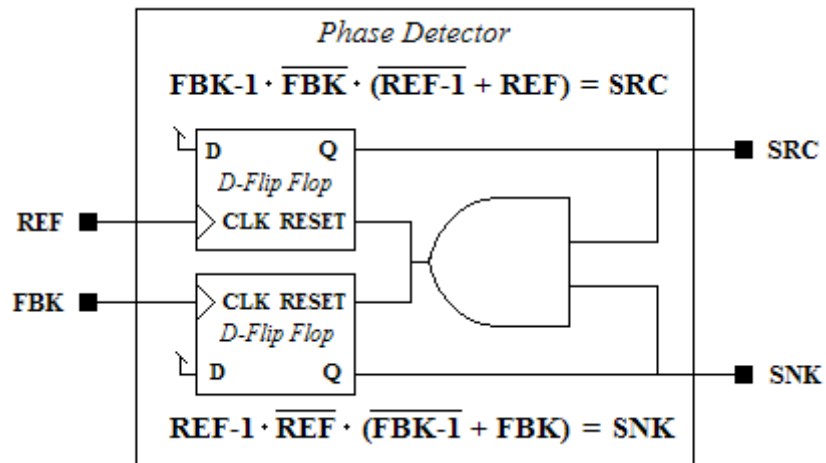


Figure 3.11: Digital Phase Detector Logic Block

The Phase Detector (PD) is depicted in Figure 3.11 as a block of digital logic that presents the results of a phase comparison between two input signals (REF, FBK) as two output error signals (SRC, SNK). Because of its digital nature understanding this circuit at a logical rather than transistor level is much more important. However when designing the logic block it is critical to balance input to output propagation delays thus minimizing systematic offset in the phase error measurement. The inputs to the two D-flip flops are connected to V_{DD} , which causes the phase measurement to trigger on the rising edge of REF and FBK. This topology could be used as a Phase Frequency Detector but in this DLL configuration the frequency is fixed so only the phase detection function is used.

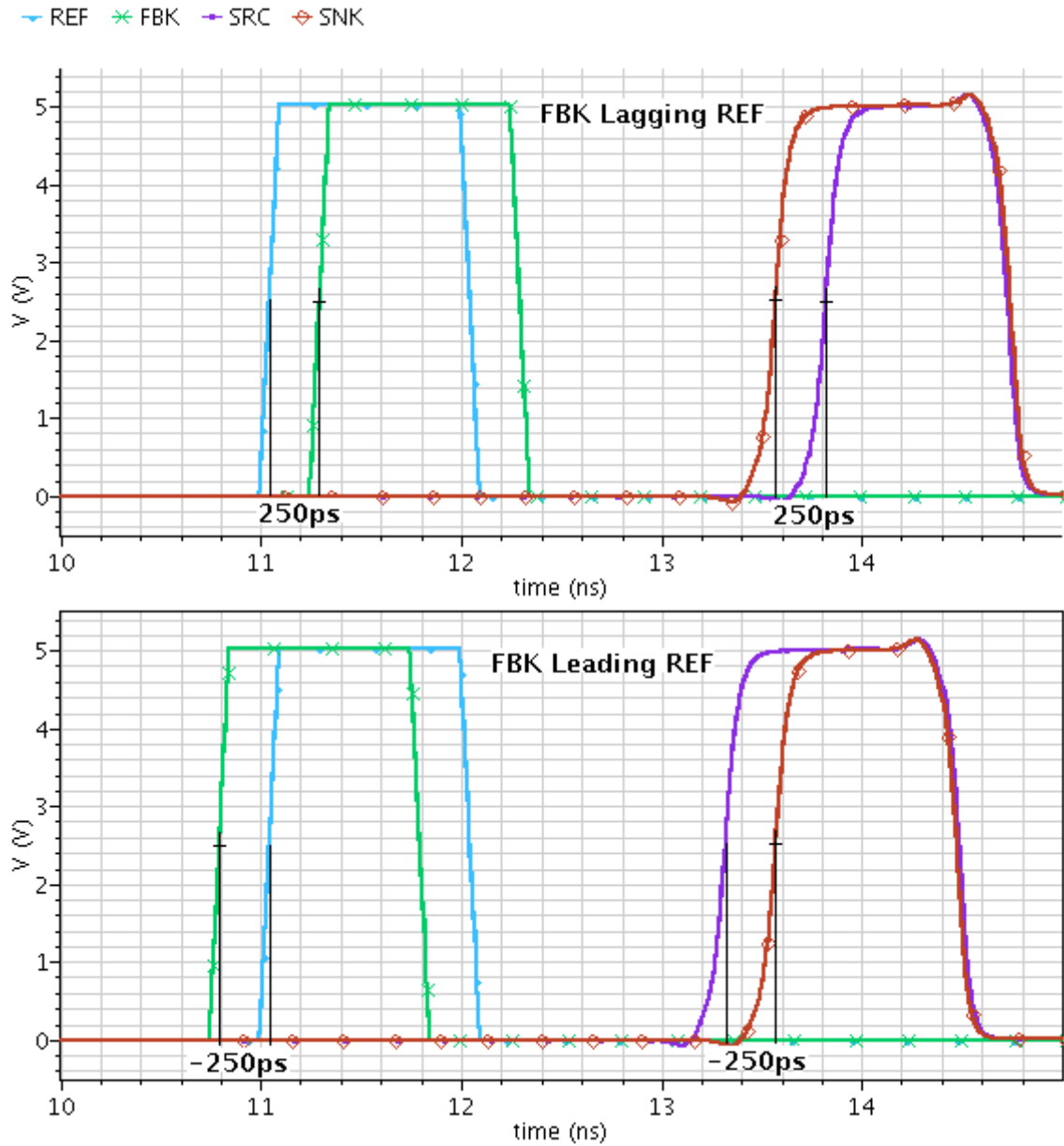


Figure 3.12: Phase Detector Input and Output Signals

Figure 3.12 depicts the relationship between the PD signal inputs and outputs. The PD measures the time or phase difference between the rising edges of input signals REF and FBK. This phase error information is stored in the pulse width difference between output signals SNK and SRC.

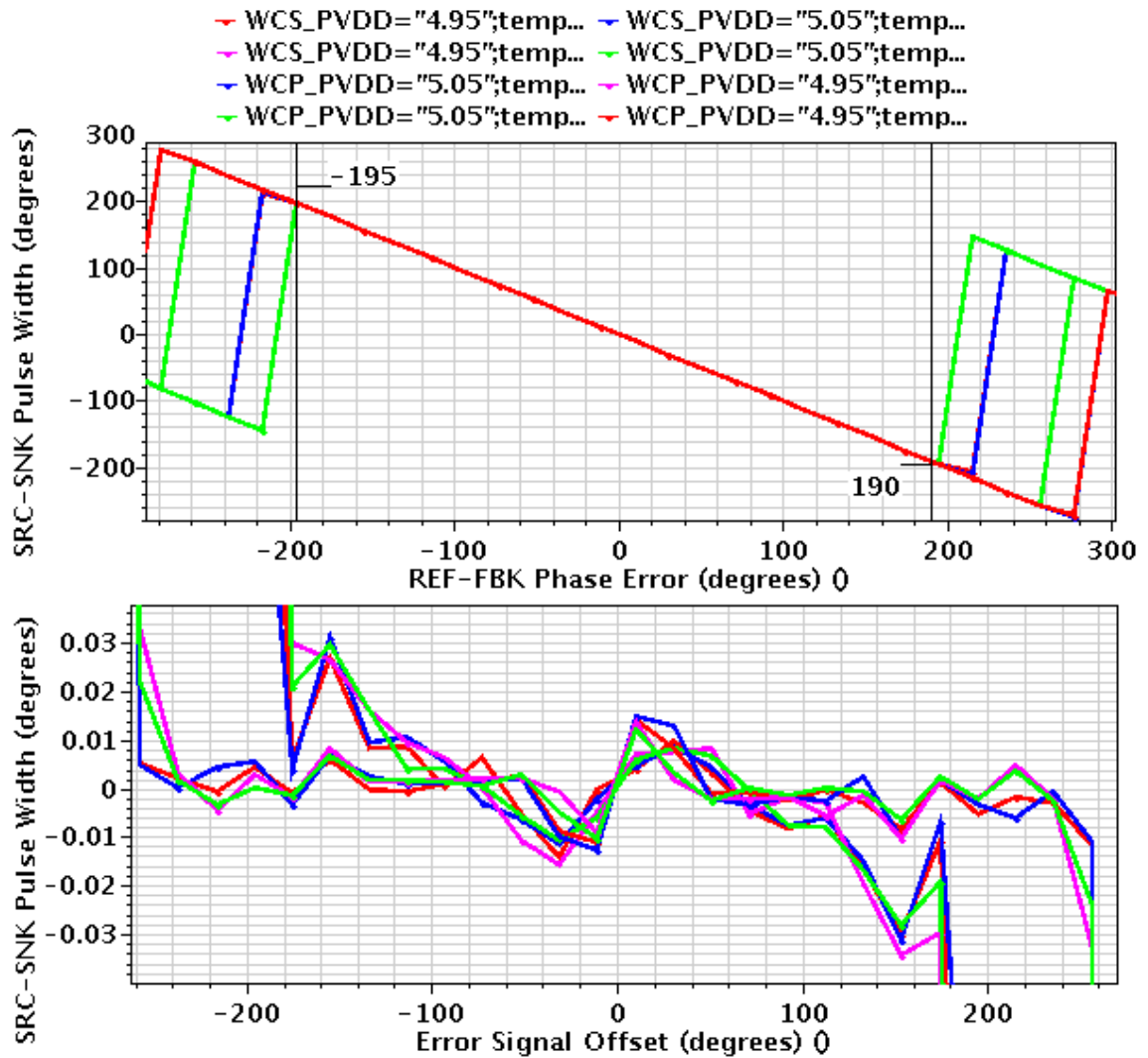


Figure 3.13: Phase Detector Error Signal and Offset

In an ideal situation, the measured phase error represented by the phase difference between the rising edge of SNK and SRC in Figure 3.13 would equal the actual phase difference between REF and FBK for all phase errors from -180° to 180° . This particular topology does a fairly good job, but Figure 3.13 shows the phase difference between SNK and SRC does deviate from ideality as the phase difference between REF and FBK approaches $\pm 180^\circ$. The phase error within the functional bounds of the PD is caused by the inability to perfectly balance signal propagation delays through the PD under all PVT

corners. The inability of the PD to issue an accurate phase error signal over the entire $\pm 180^\circ$ range must be taken into account during the design of the startup circuitry to guarantee the control loop always locks the propagation delay through the Delay Buffer to N/F_{REFCLK} where $N=1$. This can be achieved by chopping off the first rising and falling transition of the reference signal and initializing DLL_PBIAS to 0V resulting in the smallest possible T_{DEL_CSI} at any given PVT corner.

The Charge Pump:

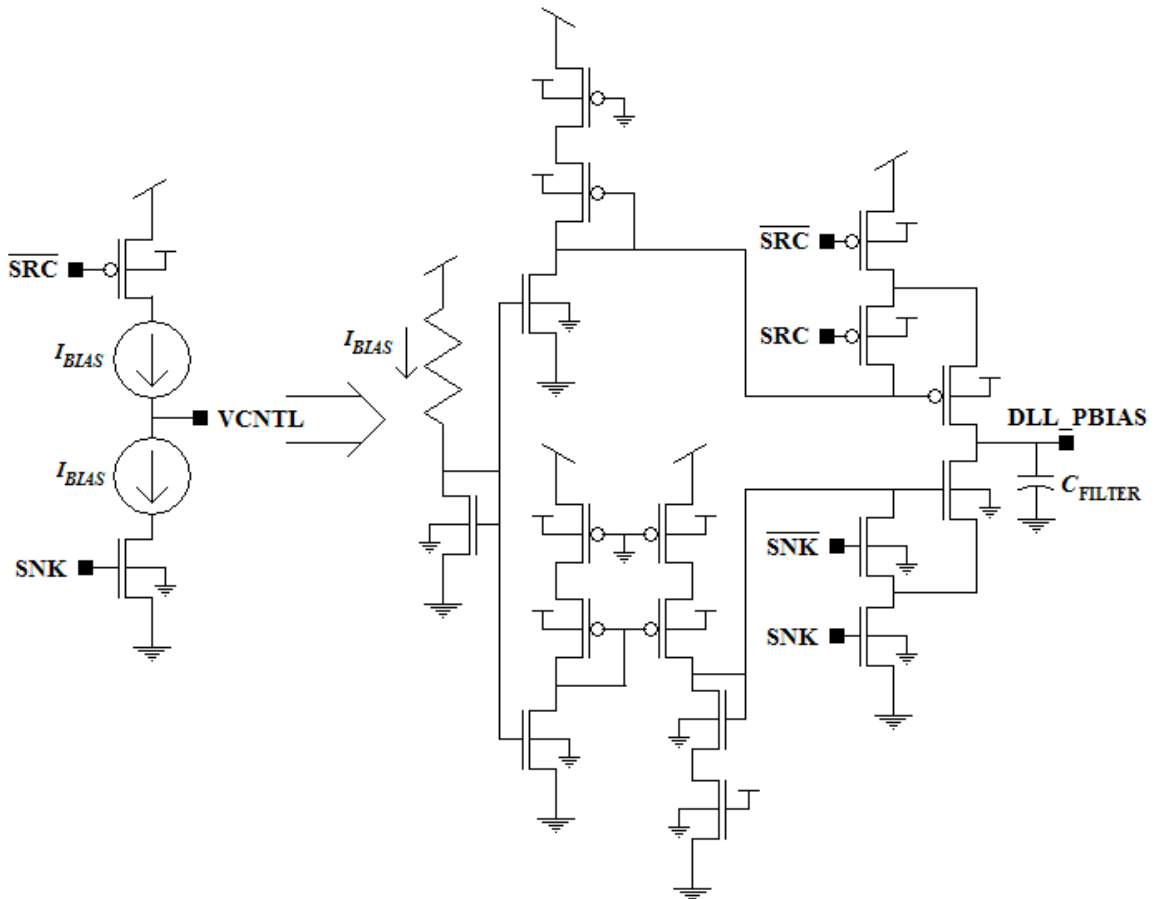


Figure 3.14: Charge Pump Schematic

The primary function of the Charge Pump (CP) depicted Figure 3.14 is to operate on the control voltage (DLL_PBIAS) based on the phase error signals (SNK, SRC) issued

by the PD. When a phase error signal is issued by the PD, node DLL_PBIAS is charged or discharged by the respective I_{BIAS} current source for a time equal to the phase difference (Δt_{ERROR}) between the rising edges of input signals REF and FBK. This basic relationship is used to derive the transfer function shown in equation [3.9] and Figure 3.15

$$\Delta t_{ERROR} = -\frac{\phi_{ERROR}}{360 F_{DLL_REF_CLK}}$$

[3.7]

$$\begin{aligned} \Delta Q_{VCNTL} &= I_{BIAS} \Delta t_{ERROR} = -I_{BIAS} \frac{\phi_{ERROR}}{360 F_{DLL_REF_CLK}} \quad [3.8] \\ &= -1.055 \times 10^{-15} \phi_{ERROR} (C) \end{aligned}$$

$$K_D (100MHz) = -I_{BIAS} \frac{1}{360 F_{DLL_REF_CLK}} = -1.055 \times 10^{-15} \frac{C}{^\circ} \quad [3.9]$$

For this DLL application $I_{BIAS} = 38\mu A$ and $F_{REF/FBK} = 100MHz$ so the relationships can be reduced to equations [3.8] and [3.9].

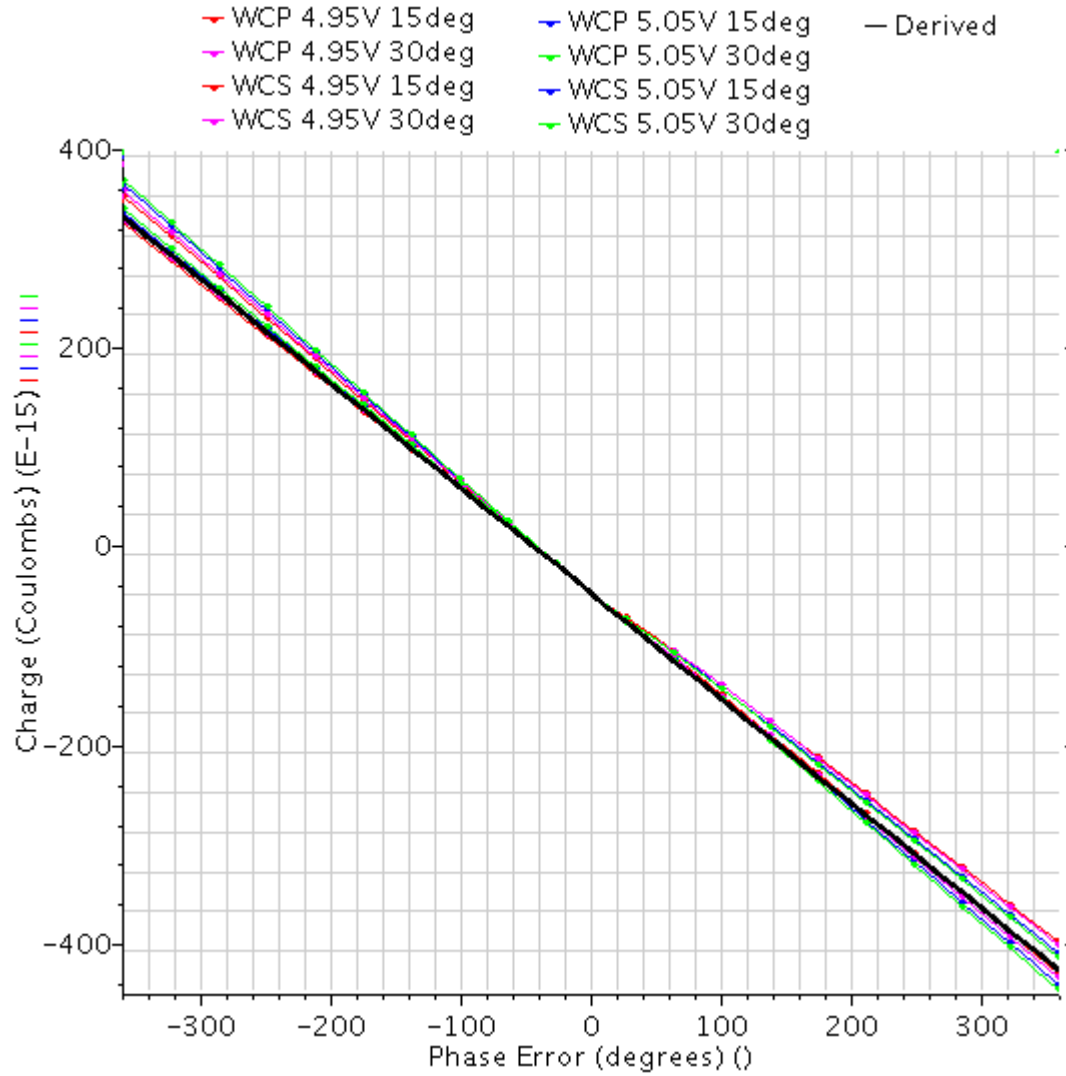


Figure 3.15: Charge Pump Transfer Function

Figure 3.15 shows the simulated and predicted CP transfer function. Equations [3.7], [3.8] and [3.9] assume an instantaneous change in current when the phase error signal is issued. This assumption is sufficient for a first order approximation of the transfer function but in reality there is a finite transition time for the current. The load seen by the CP is not purely capacitive, and additional charge is coupled onto node VCNTL through transistor parasitics. In a later section, a primarily capacitive loop filter will be designed to optimize ΔV_{CNTL} .

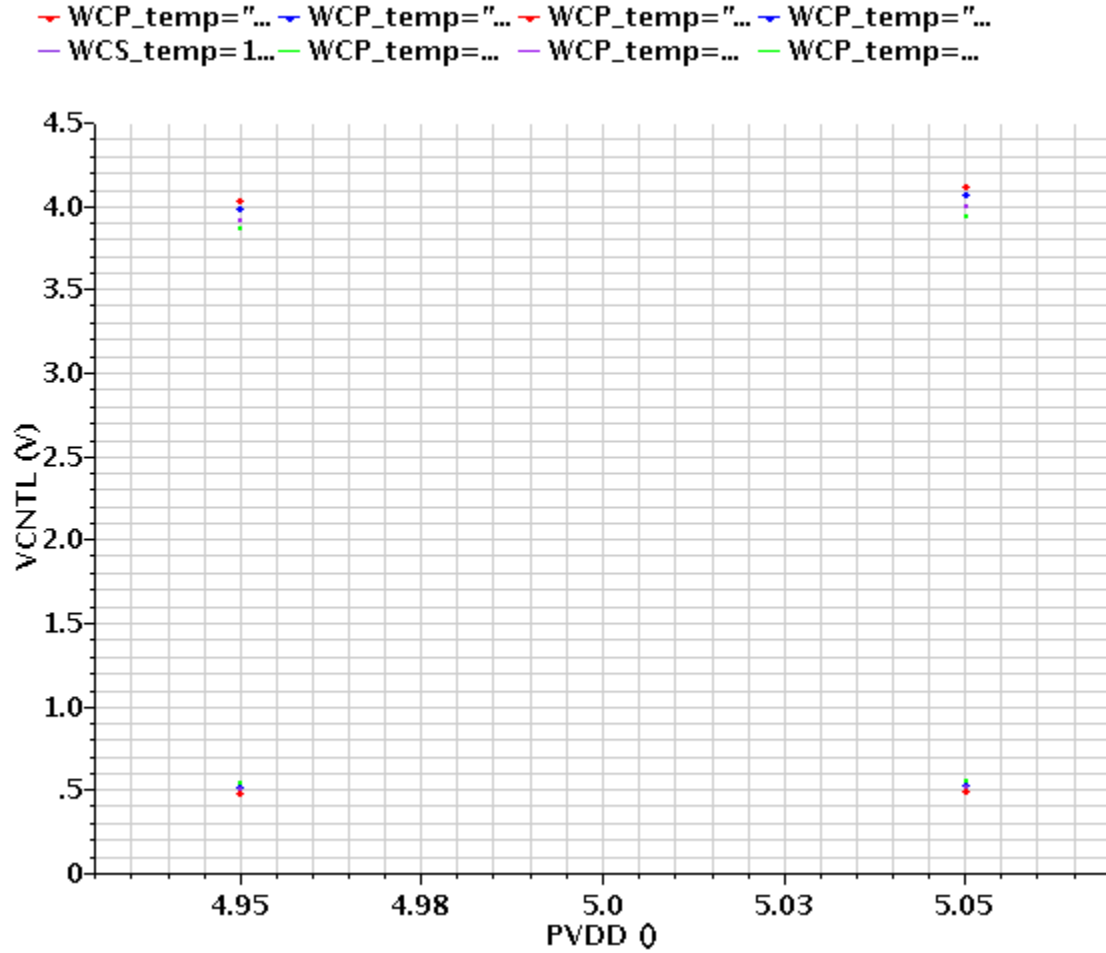


Figure 3.16: Charge Pump Range

This CP topology has a finite voltage range, as depicted by Figure 3.16, over which equations [3.5] and [3.6] apply. The voltage range is determined by the threshold voltages and finite output impedances of the transistors comprising the current sources. A quick check with Figure 3.9 confirms the range of the CP is sufficient to control $T_{\text{DEL_CSI}}$ to 250ps.

The Loop Filter: The DLL is a simple 1st order control loop that only requires a single pole, low pass loop filter composed of a capacitor, C_{FILTER} connected between node VCNTL (i.e. DLL_PBIAS) and V_{SS} in Figure 3.14. The change in node voltage

ΔV_{CNTL} is determined by the magnitude of I_{BIAS} and total capacitance C_{LOAD} associated with control voltage DLL_PBIAS. C_{LOAD} is composed of the loop filter (C_{FILTER}) and the parasitic capacitance ($C_{PARASITIC}$) associated with every device connected to this node.

$C_{PARASITIC}$ was determined through simulation to be 4.45pF and C_{FILTER} was set to 20pF to minimize the effect of noise on the DLL_PBIAS control voltage without unnecessarily increasing the settling time of the DLL. $C_{LOAD} = 24.45\text{pF}$ can be used to relate the phase error signal Φ_{ERROR} to ΔV_{CNTL} and determine the transfer function $H_{LPF}(100\text{MHz})$

$$\Delta V_{CNTL} = \frac{\Delta Q_{VCNTL}}{C_{LOAD}} = 40.9 \times 10^9 \Delta Q_{VCNTL} \quad [3.10]$$

$$K_F(100\text{MHz}) = 40.9 \times 10^9 \frac{V}{C} \quad [3.11]$$

DLL Transfer Function: Now that the transfer functions for each individual block in the DLL have been derived or calculated, the overall DLL transfer function for $F_{DLL_REF_CLK}=100\text{MHz}$ can be determined.

$$\begin{aligned} H_{DLL}(100\text{MHz}) &= K_V(100\text{MHz}) * K_D(100\text{MHz}) * K_F(100\text{MHz}) \\ &= 157.68 \frac{\circ}{V} * -1.055 \times 10^{-15} \frac{C}{\circ} * 40.9 \times 10^9 \frac{V}{C} \\ &= -6.8 \times 10^{-3} \frac{V}{V} \end{aligned}$$

[3.12]

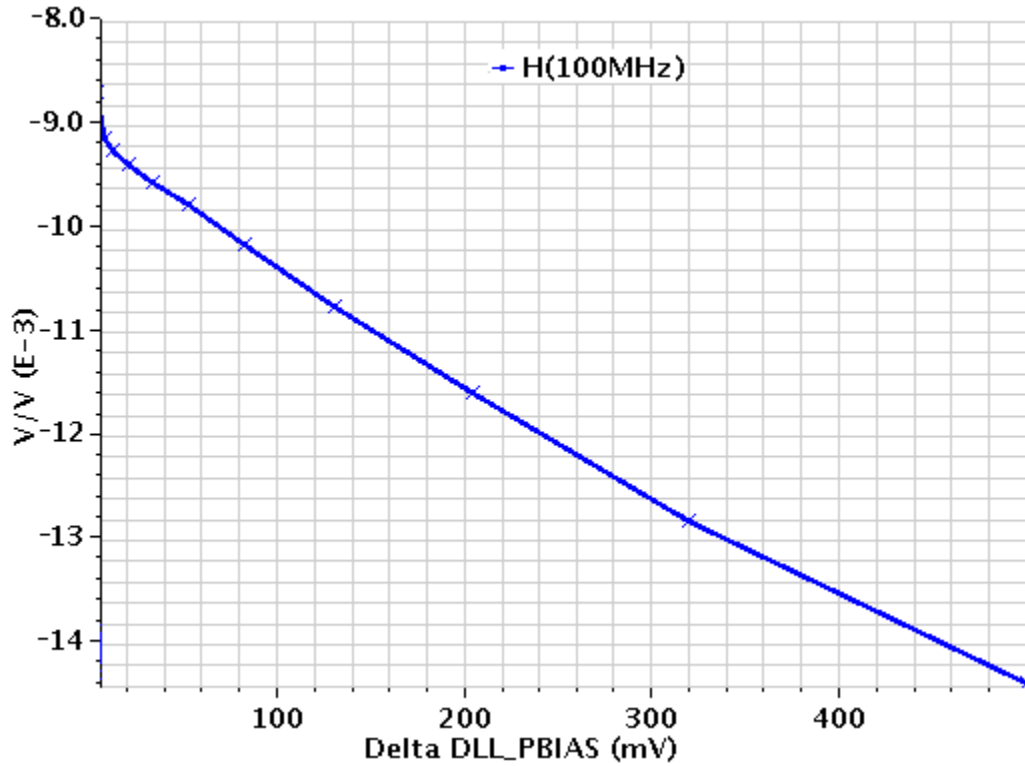


Figure 3.17: DLL Transfer Function at 100MHz for various changes in DLL_PBIAS

Figure 3.17 shows the simulated $H_{DLL}(100\text{MHz})$ for a range of ΔV_{DLL_PBIAS} . The theoretical prediction represented by equation [3.12] is very close to the simulated transfer function as ΔV_{DLL_PBIAS} approaches zero. Figure 3.17 also shows the assumption of linearity is not valid when ΔV_{DLL_PBIAS} becomes large. The discrepancy between the simulated and theoretically $H_{DLL}(100\text{MHz})$ could be caused by the omission of two specific second-order effects during derivations. First, the charge pump has a finite transition time which results in a changing current over the time when the CP is charging or discharging node DLL_PBIAS. Theoretical derivations assume this current flow is constant. Second, charge injection through device parasitics during CP transitions could contribute a significant amount of charge to the node DLL_PBIAS. Charge injection was not accounted for during derivations.

System Level Considerations

Simultaneous Switching:

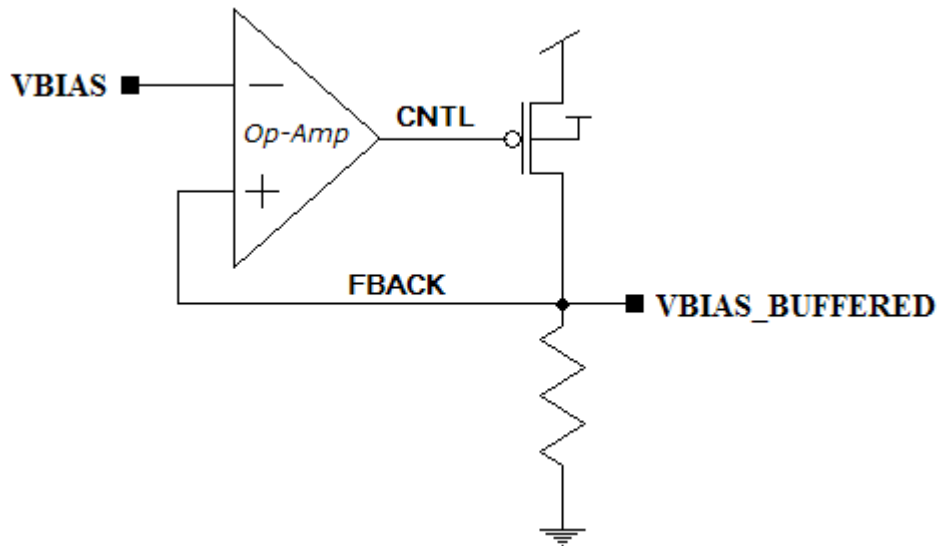


Figure 3.18: Unity Gain Buffer

With the current configuration, a small amount of charge is added or subtracted to DLL_PBIAS and DLL_NBIAS with every CSI transition due to transistor parasitic capacitance. This charge flow can add up significantly, depending on the number of CSI connected to each bias voltage. A unity gain stage, depicted in Figure 3.18, could be used to buffer the master loop control voltages from the SSN associated with slave CSI. This approach tends to average the SSN, but device mistracking in the amplifier will introduce an offset into the bias voltage. Monte Carlo analysis can be used to determine the magnitude of offset voltage and if buffering of the control voltages is a good design tradeoff. In this application, the number of switching CSI in the slave Delay Line is small (12) relative to the number of switching CSI in the master Delay Buffer (48), so I opted not to buffer either control voltage.

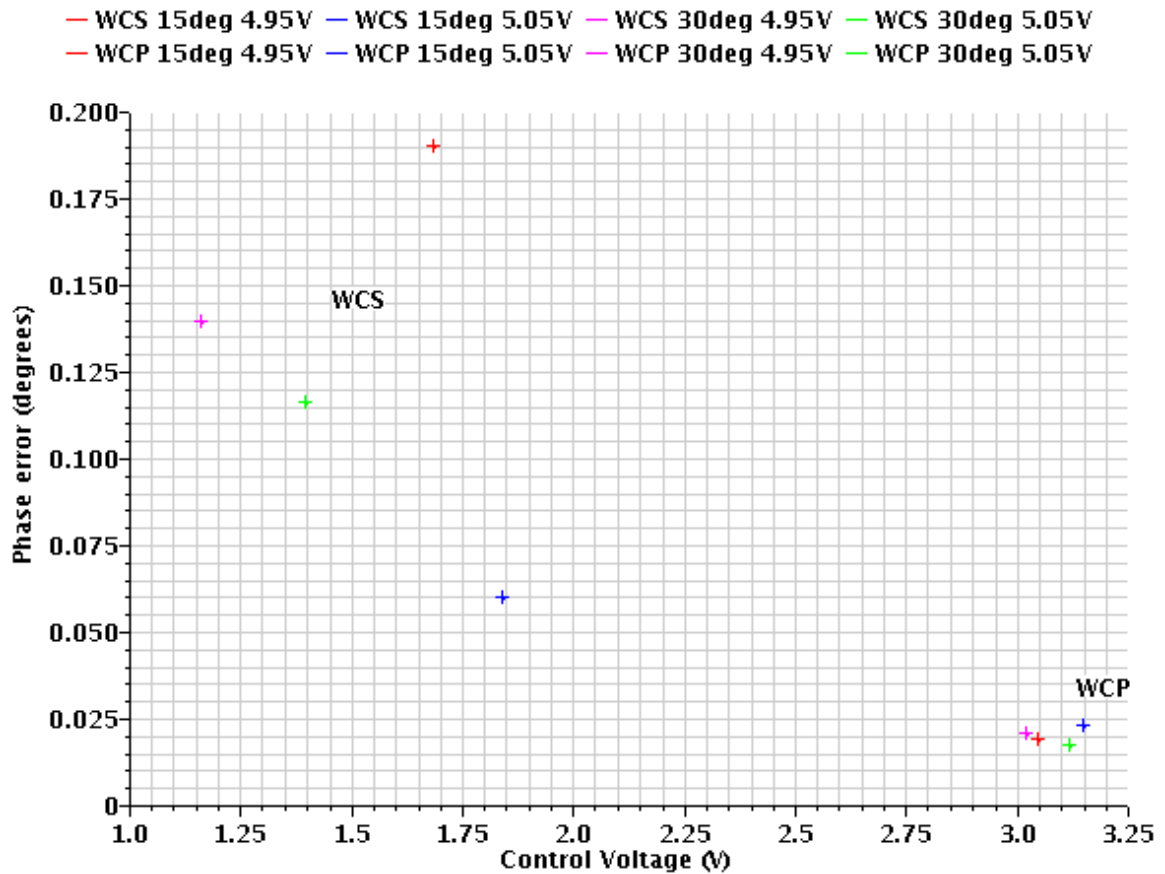


Figure 3.19: DLL Phase Error and Steady State Control Voltage

Figure 3.19 shows two important characteristics of the DLL feedback loop. The final PBIAS control voltage for each of the 8 PVT corners of interest can be ascertained from the X-axis in addition to the phase error associated with each corner from the Y-axis. It's important to note the steady state control voltage for each corner is well within the CP limitations depicted in Figure 3.16. The systematic phase error for each corner was calculated by averaging the time difference between the REF and FBK signals in the PD over multiple clock periods and then converting that time difference to a phase error relative to the 100MHz operating frequency. Figure 3.19 does not provide any information about phase error caused by SSN.

There are multiple sources of systematic offset in the DLL control loop. A buffered version of the reference signal is used as an input to the PD in an attempt to minimize any offset associated with differing edge rates, but both reference and feedback signals at the inputs to the PD do have a finite edge rate. This implies switch point variation in first stage of the PD will have an effect on how well the two signals are delay matched through the PD and CP. The CP requires four input signals (SNK , $\overline{SNK}$, SRC , $\overline{SRC}$), but the PD only provides SNK and SRC . This means the inverted version of each PD output must be logically derived with special care taken to match delays and edge rates between all four CP inputs. Because the logic used to derive the four CP inputs is not identical, delay mismatch can be minimized at one PVT corner but there will be a finite amount of mismatch at other corners. The final source of systematic offset in the DLL loop is the CP itself. To a first order, the CP can be approximated as a linear integration circuit, containing ideal switchable current sources, with infinite impedance and transition rates. The second order, non-linear effects of finite impedance and transition rate as well as mismatch between the SNK and SRC current sources all contribute to systematic offset observed in the loop. Both the DLL and WPLL are very similar from a control loop perspective. A control system analysis of both loops will be conducted in a later section.

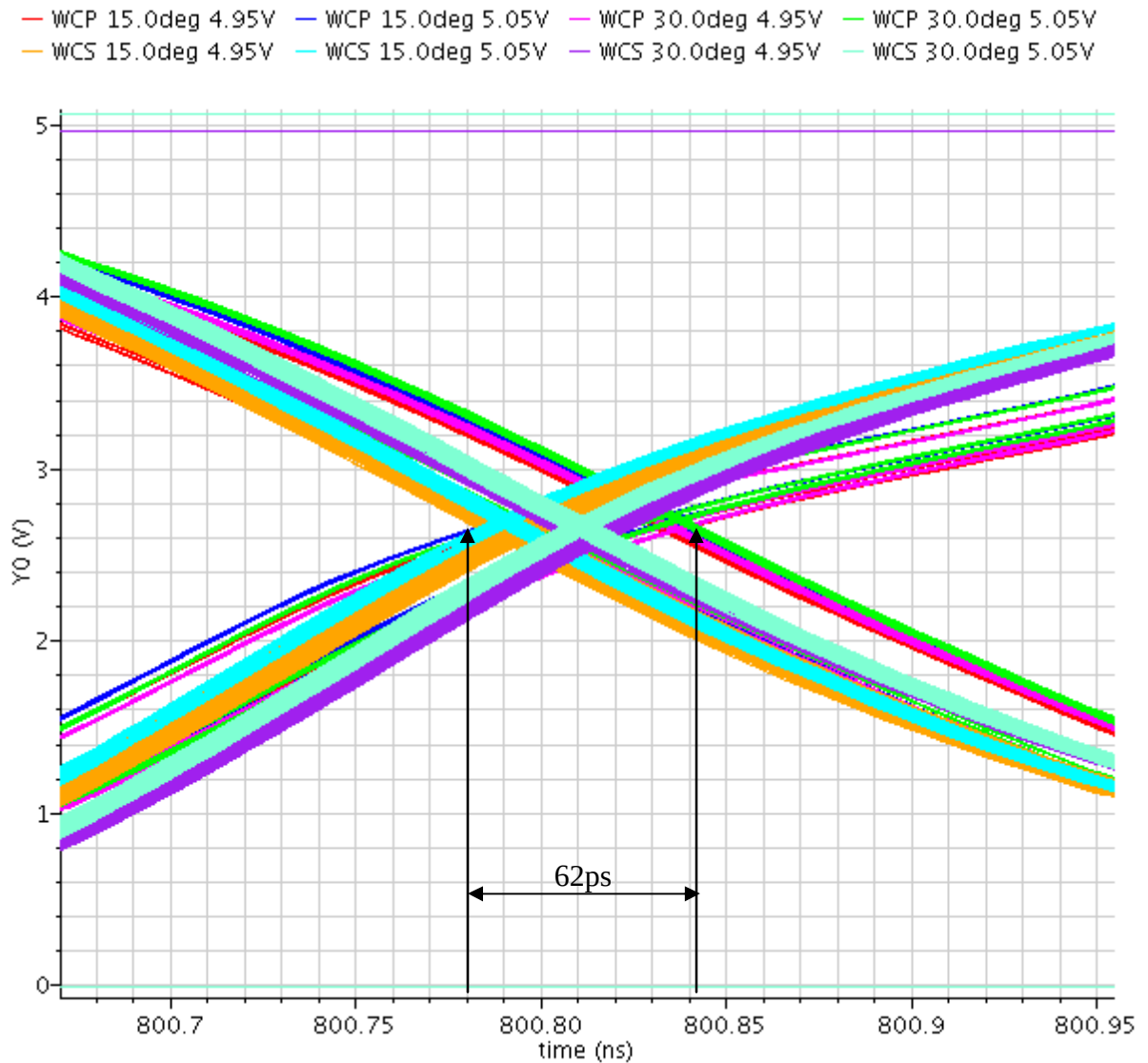


Figure 3.20: Total DLL Phase Error

Figure 3.20 is an Eye Diagram of the DLL FBK signal for each of the 8 PVT corners of interest. This plot shows the total phase variation caused by systematic offset in the loop and SSN to be 62ps which corresponds to 2.23° at 100MHz. The phase variation in the slave 3ns delay line used in the WPLL loop will be significantly less because of the smaller number of CSI. The total DLL phase variation can be divided by

the number of CSI in the DLL Delay Buffer to calculate the phase error contribution of each stage as shown in equation [3.13].

$$\frac{62ps}{20stages} = 3.1ps / stage \quad [3.13]$$

Stability Analysis: Typically stability analysis is conducted by characterizing a feedback loop in the frequency domain over a range of frequencies to ensure the gain and phase margin are adequate. In this type of simulation, each circuit is simplified to its small signal linear equivalent, which drastically reduces the complexity and runtime of the simulation. Unfortunately a full, large signal model is necessary to analyze the loop stability for a circuit that contains both digital and analog components such as the DLL yielding traditional stability analysis techniques invalid.

One simple but crude technique for analyzing the loop stability of circuits with both digital and analog components involves observing the loop step response in the time domain. The loop is broken at a convenient place such as at the control voltage, and a supply is inserted in series. The loop response can be observed by instantaneously stepping the voltage of the ideal supply to some positive value after the loop has converged to its steady-state operating point. A voltage step with instantaneous transition time contains components of all frequencies, so this technique effectively evaluates the loop stability over the entire frequency spectrum. While simulations in the frequency domain are necessary to determine actual values for the gain and phase margin, observing the loop step response in the time domain yields qualitative stability results, i.e. oscillation is induced or not. Additionally, this method does give a good feel for the damping ratio.

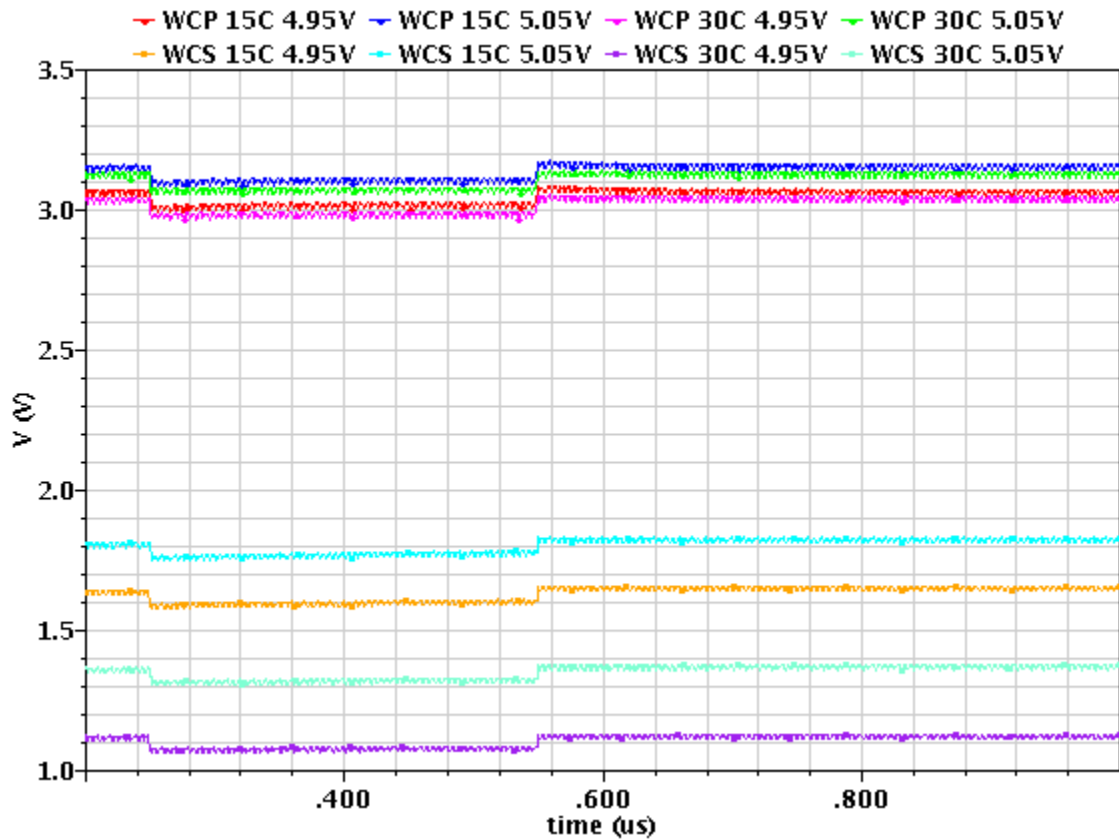


Figure 3.21: DLL Step Response

Figure 3.21 shows the DLL_CNTL control voltage as a function of time. At time $t = 250\text{ns}$ and $t = 500\text{ps}$, a negative and positive 50mV step with 1ps transition time is imposed on the control voltage. Both near instantaneous voltage steps result in the loop compensating without oscillation, and a closer inspection of the loop reaction reveals the characteristic of an over damped system, qualitatively implying that there is sufficient gain and phase margin.

The design point shown in Figure 3.21 is most certainly stable but it can be optimized further to reduce the loop time constant. This is achieved by increasing the gain of one or more of the loop components thereby increasing the total loop gain. Increasing the current or effective strength of the CP is one obvious method for increasing the overall loop gain and reducing the loop time constant but it has drawbacks.

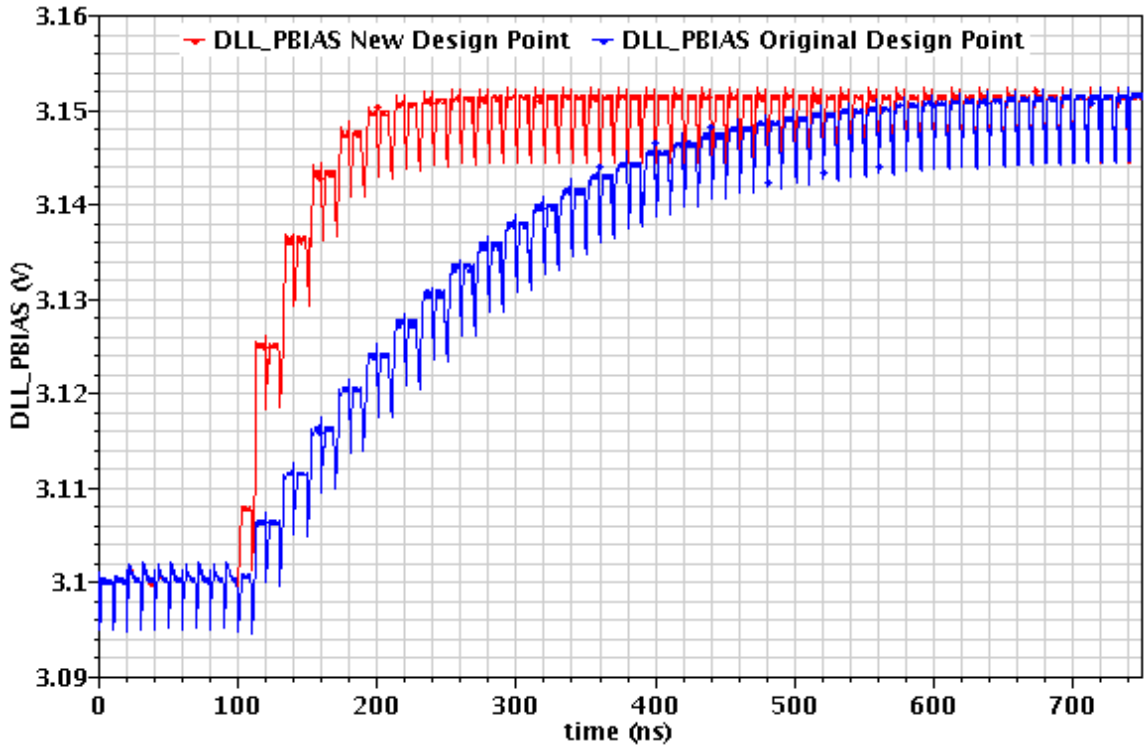


Figure 3.22: Original and Modified DLL response for WCP, 15°C, $V_{DD} = 5.05V$

Figure 3.22 shows the DLL response for the PVT corner that has the fastest loop response (WCP, 15°C, $V_{DD} = 5.05V$). The PVT corner representing the fastest loop response is used during optimization to ensure that under no condition the loop response is under damped. The control voltage is held constant at 3.1V until time $t = 100ns$ when a switch is opened and the loop is allowed to converge on its steady state value. The blue curve representing the original transfer function of Figure 3.15 and response of Figure 3.21 converges much more slowly than the red curve, where the CP reference current, and consequently, the gain have been increased to the point where the total loop response is critically damped. Note the non-ideal transients seen on the control voltage that occur when the CP is turning on and off. These transients, caused by charge injection through switching transistor parasitics, are slightly more pronounced in the new

design point because of the larger reference current and device sizes necessary to achieve the desired increase in gain. The new design point converges in 160ns, which is 3.75 times as fast as the original design point.

The Master ½ Wilkinson & 3dB Attenuator

The Master ½ Wilkinson and 3dB attenuator are designed to minimize the effects of amplifier distortion and match the signal characteristics of the REF and FBK signals entering the PD of the WPLL. Hardware and simulations have shown the sensitivities of the SCAI and Wilkinson w/SCAI to larger input levels so to ensure the amplitude of the input signal is known and easily controllable it is necessary to match the input impedance of the reference network to the system.

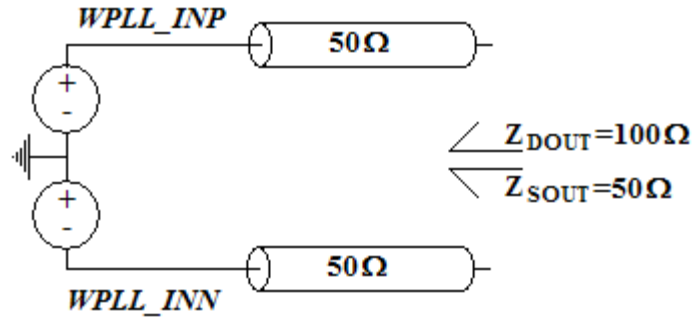


Figure 3.23: WPLL Driving Network

Figure 3.23 shows the differential network that will be used to drive the WPLL and provide a reference signal. The differential output impedance $Z_{DOUT} = 100\Omega$ but the single ended output impedance $Z_{SOUT} = 50\Omega$ to ground.

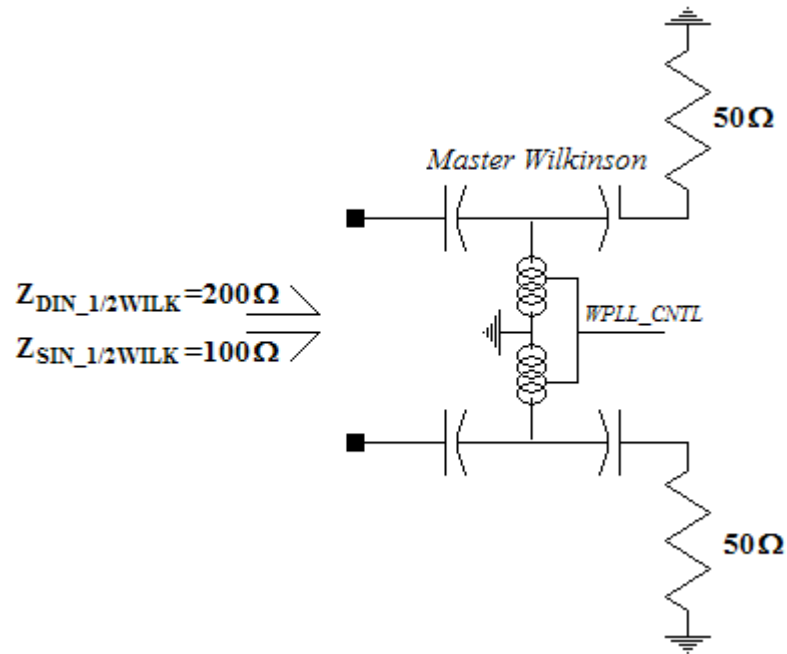


Figure 3.24: Master 1/2 Wilkinson Schematic

When the WPLL has converged and the SCAI has been tuned to the target inductance the reactance of the series capacitors and shunt inductors in Figure 3.24 will cancel presenting a purely real load. The differential impedance $Z_{DIN_1/2WILK} = 200\Omega$ but the single ended impedance $Z_{SIN_1/2WILK} = 100\Omega$ to ground.

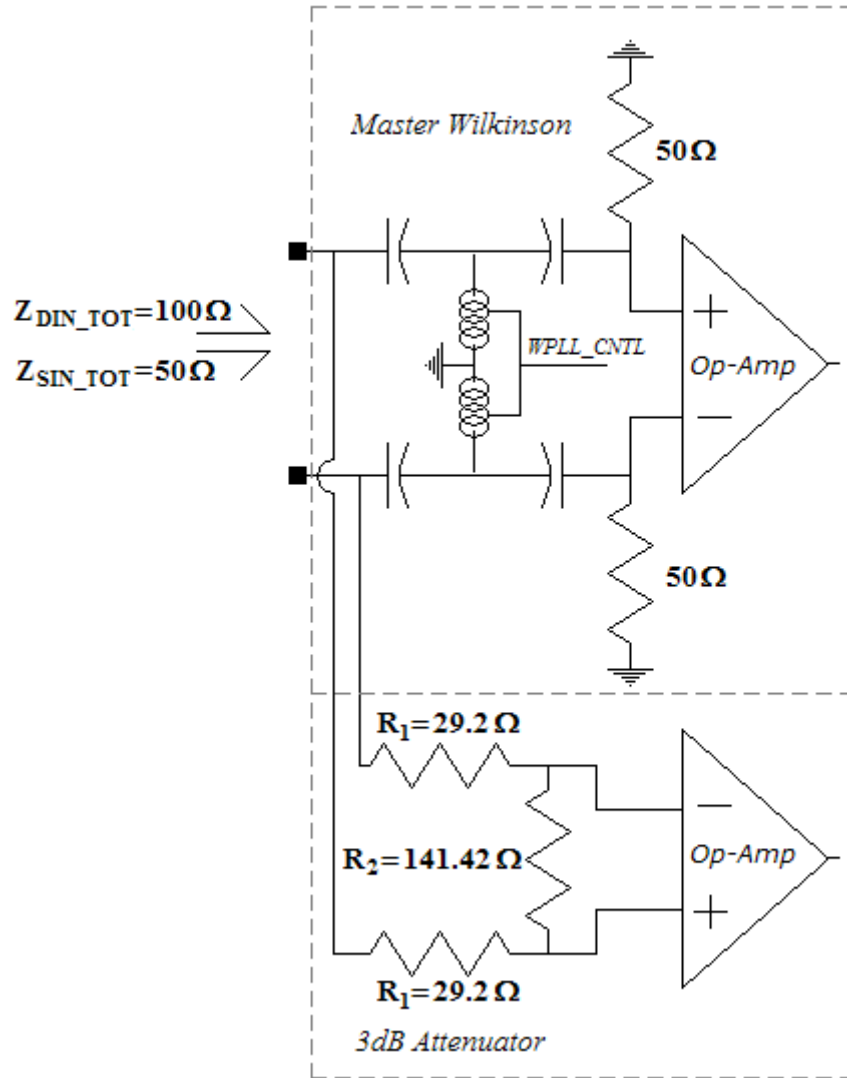


Figure 3.25: Master 1/2 Wilkinson & 3dB Schematic

The 3dB attenuator must be designed to perform two equally important functions, the first to attenuate the input signal by 3dB and the second to match the total impedance looking into the WPLL reference network to the output impedance of the driving network.

$$V_o(V) = \frac{\sqrt{2}}{2} V_{IN}(V) = V_{IN} \frac{R_2}{2R_1 + R_2} \quad [3.14]$$

Equation [3.14] shows the transfer function that yields 3dB of attenuation from input to output. The single-ended and differential impedance of the driving network ($Z_{SOUT} = 50\Omega$, $Z_{DOUT} = 100\Omega$) defined in Figure 3.23, in addition to the input impedance of the Master $\frac{1}{2}$ Wilkinson ($Z_{DIN_1/2WILK} = 200\Omega$) shown in Figure 3.24, implies that the input impedance of the 3dB attenuator (Z_{DIN_3dB}) must be set to 200Ω such that the total input impedance of the WPLL reference network (Z_{DIN_TOT}) matches Z_{DOUT} as depicted in Figure 3.25. These constraints can be used to algebraically solve for $R_1 = 29.2\Omega$ and $R_2 = 141.42\Omega$ which are also shown in Figure 3.25.

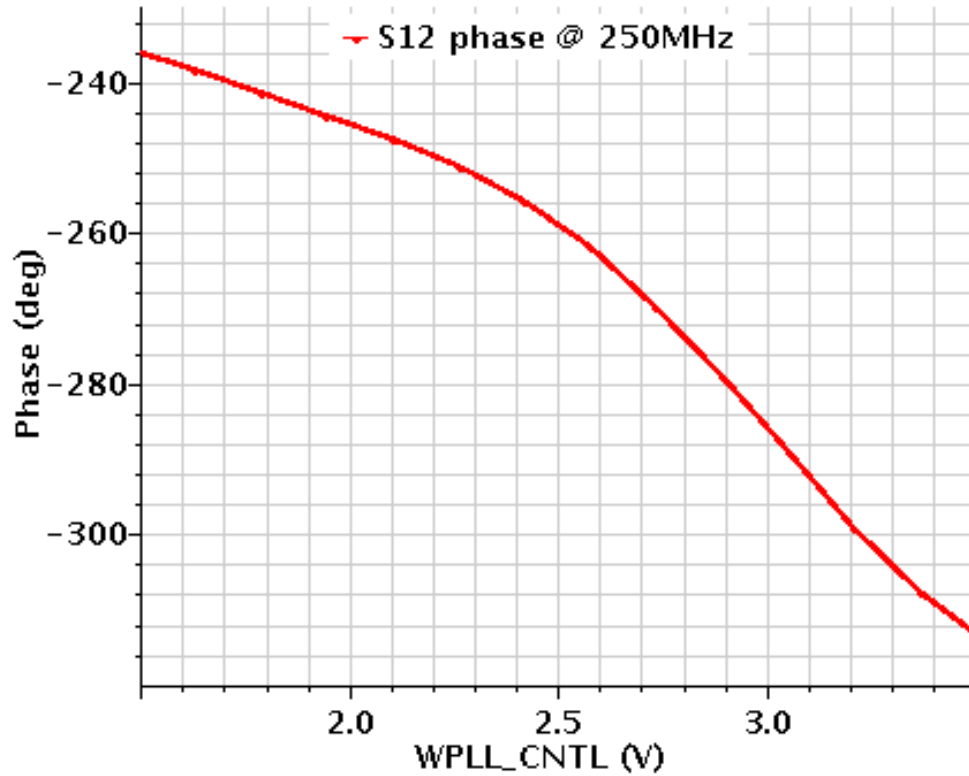


Figure 3.26: Master Wilkinson Phase Vs Control Voltage

Figure 3.26 shows the relationship between the WPLL_CNTL control voltage and the signal phase shift through the Master $\frac{1}{2}$ Wilkinson. The transfer function shown in

equation [3.15] can be derived from Figure 3.26 assuming a linear relationship directly around the steady state operating point of 270° .

$$\phi_{1/2_WILK} = 54.8V_{WPLL_CNTL} + 119.9 \quad [3.15]$$

$$K_V = 54.8 \frac{^\circ}{V} \quad [3.16]$$

The Operational Amplifier

The primary function of the Operational Amplifiers is to convert the two differential input signals from the small signal analog to the digital domain without distorting the phase difference information.

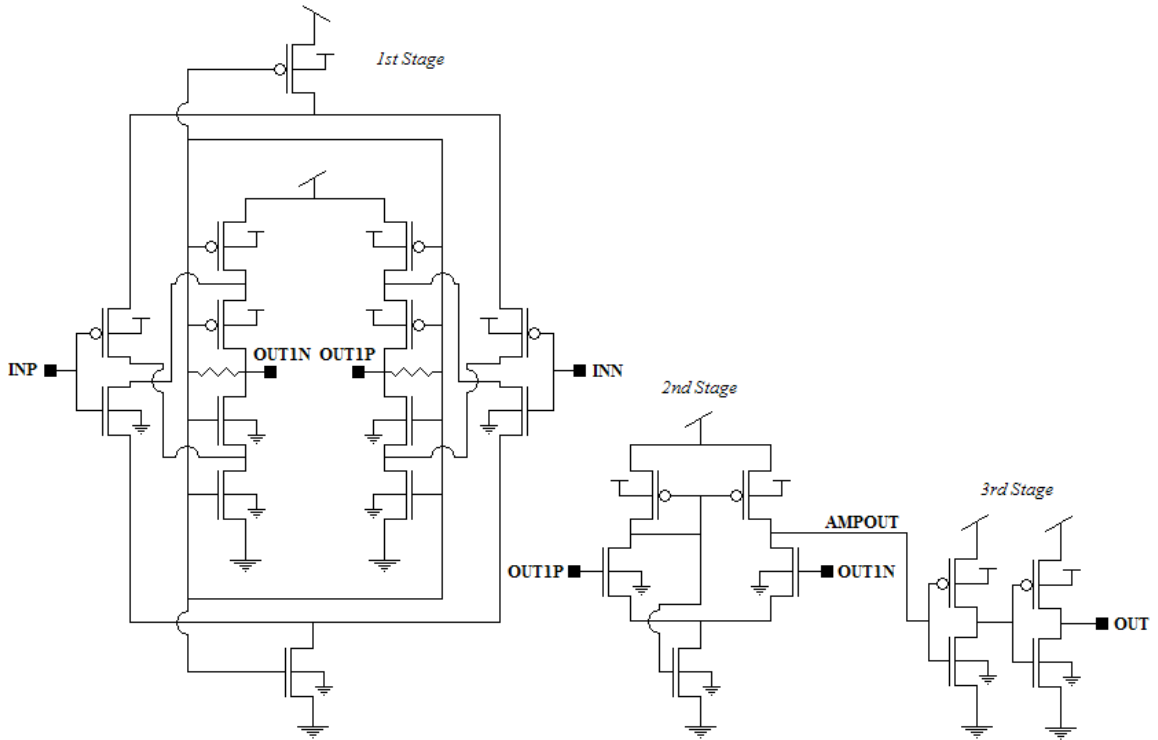


Figure 3.27: Master 1/2 Wilkinson & 3dB Schematic

Figure 3.27 shows a schematic of the multi-stage operational amplifier used in both paths of the WPLL. The topology of the WPLL is such that the absolute delay and

transition rates of the Op-Amp are not of direct concern as long as the signal at node OUT transitions from V_{DD} to V_{SS} at the desired frequency of 250MHz.

The wide-common-mode, fully differential, folded cascode, self-biasing, small signal amplifier used for the first stage was first developed by Bazes [16] but negative feedback was added by Chan [17] to improve the gain and maximum operating frequency. Admittedly, the performance of this first stage could probably be improved with a less complex and therefore lower capacitance topology because the input signal has a fixed common mode of $V_{DD}/2$. However the primary purpose of this research is to prove the viability of an active compensation scheme for the SCAI and while this first stage may not be optimal, it serves the purpose of converting a very small input signal to a level detectable by the following stage. Using an iterative design approach, a gain of approximately 2.5V/V was determined to yield the best signal at the output. The target gain was achieved by adjusting the feedback resistors depicted in Figure 3.27.

The double- mirrored- compensated CMOS receiver used for the second stage was first developed by Chappel [15] to amplify off-chip ECL signals to the digital domain. The topology employs a self biasing scheme similar to a class A/B buffer where the bias voltage of the tail device is connected to the node driving the active load. This biasing scheme enhances the output transition rate of the amplifier by increasing the gate to source voltage of the tail device during a falling transition and decreasing the gate to source voltage of the tail device during a rising transition. The primary function of this stage is to convert the differential signal at nodes OUTP and OUTN to a rail-to-rail digital signal at node AMPOUT. The second stage is optimized by adjusting devices

sizes and therefore the impedance of the active load and the gain of the differential pair such that the gain of the second stage is approximately 9V/V.

The third stage is comprised of a pair of inverters which act to sharpen the edge rates at node OUT. The total gain of the operational amplifier at 250MHz is the product of the individual gain stages or 22V/V. The minimum detectable input signal level was determined through simulation to be 22mVpp or -20.14dBm in a 50Ω system. The characteristics of the Operational Amplifier set the lower bound of the input signal range for the WPLL to 22mVpp while avoiding excess levels of distortion from the embedded SCAI set the higher bound around 80mVpp. In fact, to stay below the -1dB compression point as determined in chapter 2, input levels should stay below -16.1dBm or 35mVpp. An input signal level of 60mVpp was determined to be a good compromise between excess levels of distortion caused by the SCAI and operating too close to the minimum detectable signal level as determined through simulation. Future improvements to the WPLL should include modifying the Op-Amps to support lower input signal strength by increasing the total gain.

The WPLL 3ns Slave Delay Line

At 250MHz a 270° phase shift corresponds to a 3ns propagation delay. The delay per CSI pair was set at 250ps during the DLL design so a 3ns delay buffer corresponds to 12 series connected CSI.

— WCS 15.0deg 4.95V — WCS 15.0deg 5.05V — WCS 30.0deg 4.95V
 — WCS 30.0deg 5.05V — WCP 15.0deg 4.95V — WCP 15.0deg 5.05V
 — WCP 30.0deg 4.95V — WCP 30.0deg 5.05V

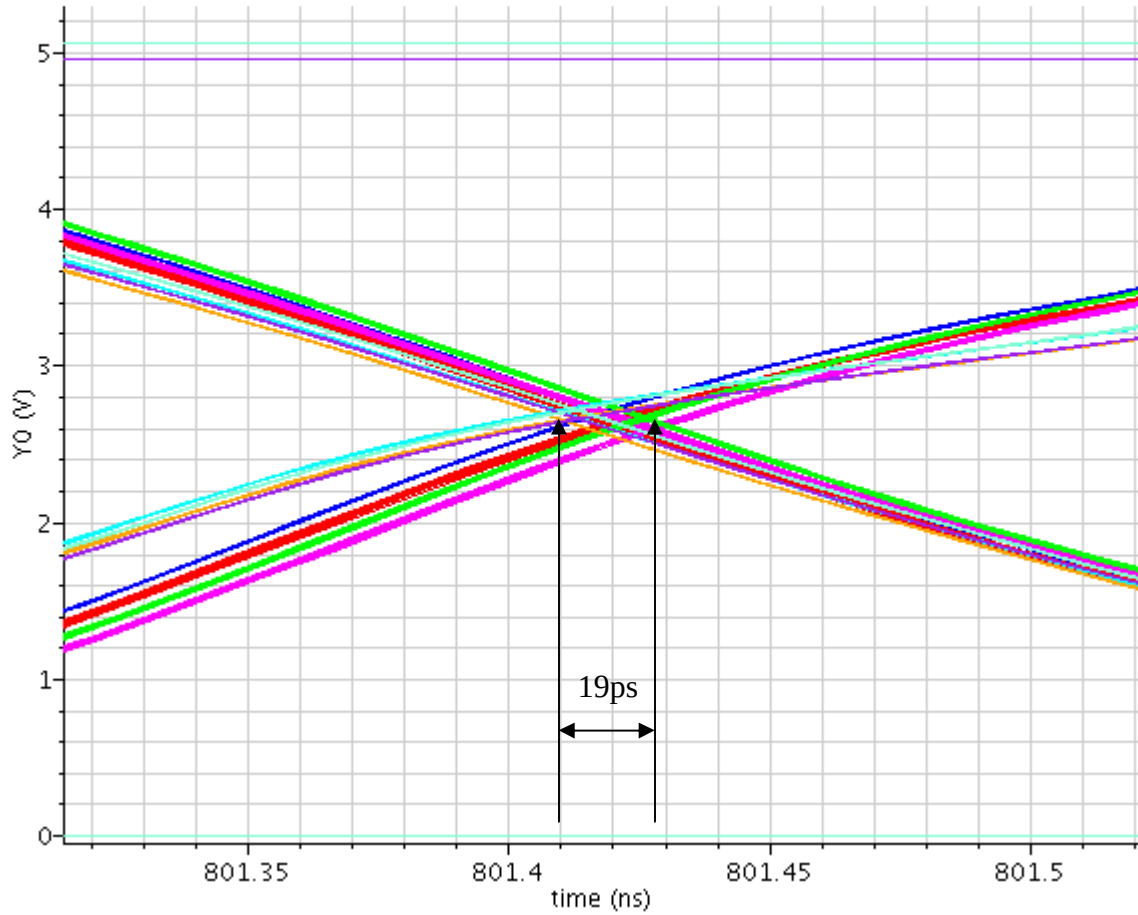


Figure 3.28: Total 3ns DL Phase Error

Figure 3.28 shows the total phase variation of the 3ns DL caused by systematic offset in the DLL loop and SSN noise for each of the 8 corners of interest. The measured phase variation of 19ps corresponds to 1.71° at 250MHz. This phase error can be thought of as the effective tolerance of the time reference in the WPLL. The phase variation of the DL is much less than the DLL loop because the number of stages in the DL is only a fraction of the number of stages in the DLL Delay Buffer.

$$6stages * 3.1ps / stage \approx 19ps \quad [3.17]$$

The WPLL Frequency Divider

A Frequency Divider (FD) is placed in series with both reference and feedback signals which divides the reference frequency of 250MHz down to 62.5MHz to reduce the switching rate within the limitations of the PD and CP.

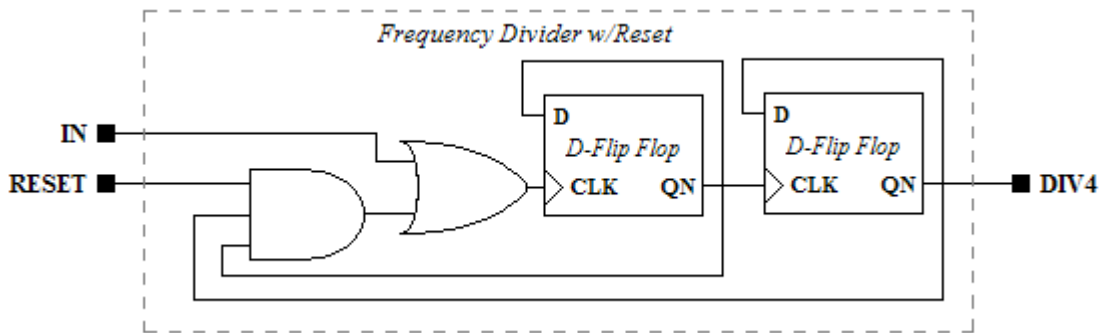


Figure 3.29 Frequency Divide by Four w/Reset Digital Logic Block

The FD depicted in Figure 3.29 is a block of digital logic with a RESET signal used to set internal flip-flops to a known state. If RESET is logic '1', the internal D flip-flops are flushed to a known state and the output DIV4 will be set to logic '1'. If RESET is logic '0', QN of each internal flip-flop will transition on the falling edge of its respective input CLK signal. The result is a counting function such that the output signal DIV4 transitions on every four transition of input signal IN thereby dividing the switching frequency by four.

The WPLL Phase Detector

The WPLL Phase Detector is physically identical to the Phase Detector (PD) used in the DLL and depicted in Figure 3.10.

The WPLL Charge Pump

The WPLL Charge Pump is physically identical to the Charge Pump (CP) used in the DLL and depicted in Figure 3.13 but the frequency of operation is 250MHz rather than 100MHz so the transfer function derived in equations [3.18], [3.19] and [3.20] is slightly different.

$$\Delta t_{WPLL_ERROR} = -\frac{\phi_{WPLL_ERROR}}{360 F_{WPLL_REF}} \quad [3.18]$$

$$\begin{aligned} \Delta Q_{WPLL_CNTL} &= -I_{BIAS} \Delta t_{WPLL_ERROR} = -I_{BIAS} \frac{\phi_{WPLL_ERROR}}{360 F_{WPLL_REF}} \quad [3.19] \\ &= -4.2 \times 10^{-16} \phi_{WPLL_ERROR} (C) \end{aligned}$$

$$K_D (250MHz) = \frac{1}{360 F_{WPLL_REF}} = -4.22 \times 10^{-16} \frac{C}{\circ} \quad [3.20]$$

The WPLL Loop Filter

The WPLL is a simple 1st order control loop that only requires a single pole, low pass loop filter comprised of a lumped capacitance between node WPLL_CNTL and V_{SS}. The primary function of this filter is to minimize the effect of noise on node WPLL_CNTL without unnecessarily increasing the loop time constant. The change in node voltage ΔV_{WPLL_CNTL} is determined by the magnitude of I_{BIAS} and total capacitance associated with WPLL_CNTL. It turns out that the simple parasitic capacitance associated with the devices connected to WPLL_CNTL is sufficient to minimize the effects of noise such that C_{LOAD_WPLL_CNTL} = C_{PARASITIC_WPLL_CNTL} = 1.8pF. C_{LOAD_WPLL_CNTL} = 1.8pF can be used to relate the charge contribution from the Charge Pump to

ΔV_{WPLL_CNTL} (equation [3.21]) and determine the transfer function $H_{LPF_WPLL}(100\text{MHz})$ (equation [3.22]).

$$\Delta V_{CNTL} = \frac{\Delta Q_{VCNTL}}{C_{WPLL_LOAD}} = 5.55 \times 10^{11} \Delta Q_{VCNTL} \quad [3.21]$$

$$K_F(250\text{MHz}) = 5.55 \times 10^{11} \frac{V}{C} \quad [3.22]$$

WPLL Transfer Function

Now that the transfer functions for each individual block in the WPLL with a gain other than 1 has been derived or calculated, the overall WPLL transfer function for $F_{WPLL_REF} = 250\text{MHz}$ can be determined and is shown in equation [3.23].

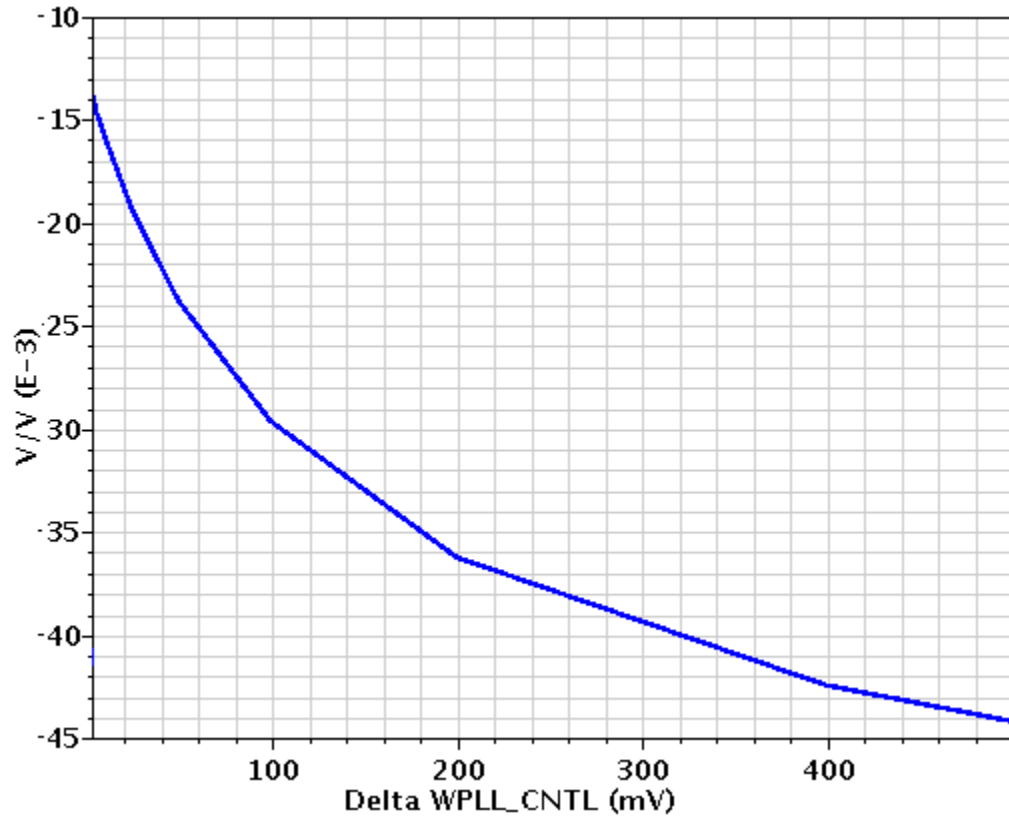


Figure 3.30: $H_{WPLL}(250\text{MHz})$ Vs $\Delta WPLL_CNTL$

Figure 3.30 shows the simulated $H_{WPLL}(250\text{MHz})$ as a function of $\Delta WPLL_CNTL$ node voltage.

$$\begin{aligned}
 H_{WPLL}(250\text{MHz}) &= K_V(250\text{MHz}) * K_D(250\text{MHz}) * K_F(250\text{MHz}) \\
 &= 54.8 \frac{\circ}{V} * -4.22 \times 10^{-16} \frac{C}{\circ} * 5.55 \times 10^{11} \frac{V}{C} \quad [3.23] \\
 &= -0.0128 \frac{V}{V}
 \end{aligned}$$

The theoretical prediction represented by equation [3.23] is very close simulated transfer function as $\Delta WPLL_CNTL$ approaches zero. Figure 3.30 also shows the assumption of linearity is not valid for large changes in $WPLL_CNTL$. The discrepancy between the simulated and theoretically $H_{WPLL}(250\text{MHz})$ could be caused by two false assumptions made during derivations. First, the CP has a finite transition time which results in a changing current over the time duration when the CP is charging or discharging node $WPLL_CNTL$ and theoretical derivations assumed current flow is constant. Second, charge injection through device parasitics during CP transitions could have a significant effect on the control voltage $WPLL_CNTL$.

System Level Considerations

WPLL & DLL Control System Analysis

Both the DLL and WPLL are very similar from a control loop perspective, therefore they can both be analyzed together to determine how the loops react to noise or error injected at different points.

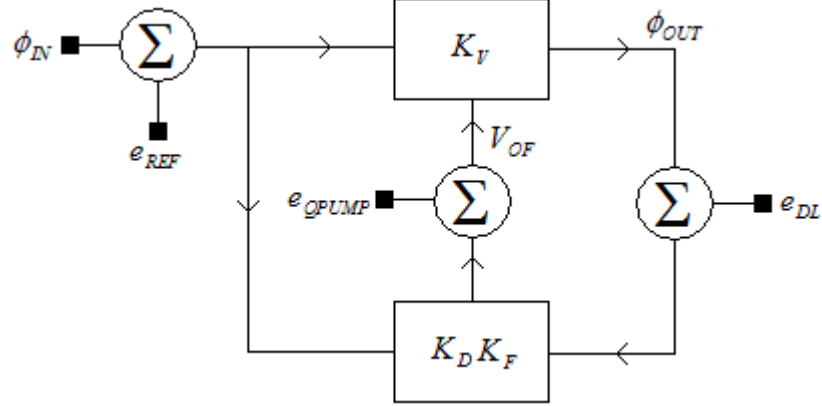


Figure 3.31: WPLL & DLL Control System Diagram

Figure 3.31 shows a high level control system diagram that represents both the WPLL and DLL loops.

$$\phi_{OUT} = \phi_{IN} + t_{DEL} \omega_{IN} \quad [3.24]$$

$$t_{DEL} = K_V V_{OF} \quad [3.25]$$

$$V_{OF} = K_F K_D \phi_{OUT} \quad [3.26]$$

$$\frac{\phi_{OUT}}{\phi_{IN}} = \frac{1}{1 - K_V K_D K_F} \quad [3.27]$$

Equations [3.24], [3.25], and [3.26] show the node equations used to derive the closed loop transfer function depicted in equation [3.27]. It is important to note that the charge pump gain (K_D) is negative which results in a positive denominator for the closed loop transfer function [18].

$$\phi_{OUT} = \frac{\phi_{IN}}{1 - K_V K_D K_F \omega_{IN}} + \frac{e_{REF}}{1 - K_V K_D K_F \omega_{IN}} + \frac{e_{DL}}{\frac{1}{K_V K_D K_F \omega_{IN}} - 1} + \frac{e_{QPUMP}}{\frac{1}{K_V \omega_{IN}} - K_D K_F} \quad [3.28]$$

Equation [3.28] shows the output phase (ϕ_{OUT}) as function of the input phase (ϕ_{IN}), noise disturbance ($e_{REF}, e_{QPUMP}, e_{DL}$) and gain terms for each individual

stage (K_V, K_D, K_F). This equation describes how the loop responds to a noise disturbance at every point. To no surprise, the loop cannot differentiate between the reference and an error in the reference (e_{REF}) and has the same response. For reasonably large values of the open loop transfer function, a large percentage of an error on the delay line (e_{DL}) will pass through to the output. The effect of an error at the control voltage can be minimized by increasing the gain of the charge pump and loop filter ($K_D K_F$). It is also important to note that as the sample rate of the loop or the reference frequency increases, the effect of e_{REF} on the output is reduced while the effect of e_{QPUMP} and e_{DL} becomes more pronounced.

Term	DLL		WPLL	
	Original	Conversion	Original	Conversion
K_V	$157.68 \frac{\circ}{V}$	$4.386 \times 10^{-9} \frac{s}{V}$	$54.8 \frac{\circ}{V}$	$6.09 \times 10^{-10} \frac{s}{V}$
K_D	$-1.055 \times 10^{-15} \frac{C}{\circ}$	$-3.8 \times 10^{-5} \frac{C}{s}$	$-4.22 \times 10^{-16} \frac{C}{\circ}$	$-3.8 \times 10^{-5} \frac{C}{s}$
K_F	$40.9 \times 10^9 \frac{V}{C}$	$40.9 \times 10^9 \frac{V}{C}$	$5.55 \times 10^{11} \frac{V}{C}$	$5.55 \times 10^{11} \frac{V}{C}$
$H(s)$	$-6.8 \times 10^{-3} \frac{V}{V}$	$-6.8 \times 10^{-3} \frac{V}{V}$	$-12.8 \times 10^{-3} \frac{V}{V}$	$-12.8 \times 10^{-3} \frac{V}{V}$

Table 3.1: Gain Term Conversion Chart

Before the impact of each error term can be evaluated for the particular DLL and WPLL design points analyzed in this research, the units of K_V and K_F need to be changed so they add properly when separated. This conversion, shown in Table 3.1 has no effect on the actual value of the open loop transfer function.

$$\phi_{OUT_DLL} = 2.3 \times 10^{-7} \phi_{IN} + 2.3 \times 10^{-7} e_{REF} - 0.99 e_{DL} + 6.43 \times 10^{-7} e_{QPUMP} \quad [3.29]$$

$$\phi_{OUT_WPLL} = 4.9 \times 10^{-8} \phi_{IN} + 4.9 \times 10^{-8} e_{REF} - 0.99 e_{DL} + 4.74 \times 10^{-8} e_{QPUMP} \quad [3.30]$$

Equation [3.29] and [3.30] show the closed loop output phase as a function of the input phase and the contribution from each error source for the specific DLL and WPLL design points proposed in prior sections. As expected, the large charge pump and loop filter gain minimizes the contribution of an error on the control voltage while an error in the delay line or master Wilkinson directly adds to the total systematic offset. This implies that special care must be taken during development of the delay line to minimize potential for systematic offset. Sensitivity to error in the delay line also highlights the dependency of the WPLL on the DLL controlled phase reference. Any error in the DLL will directly add to systematic offset in the WPLL due to the serial relationship between the two control loops.

½ Wilkinson Static Phase Variation

— WCP 15deg 4.95V — WCP 15deg 5.05V — WCP 30deg 4.95V — WCP 30deg 5.05V
 — WCS 15deg 4.95V — WCS 15deg 5.05V — WCS 30deg 4.95V — WCS 30deg 5.05V

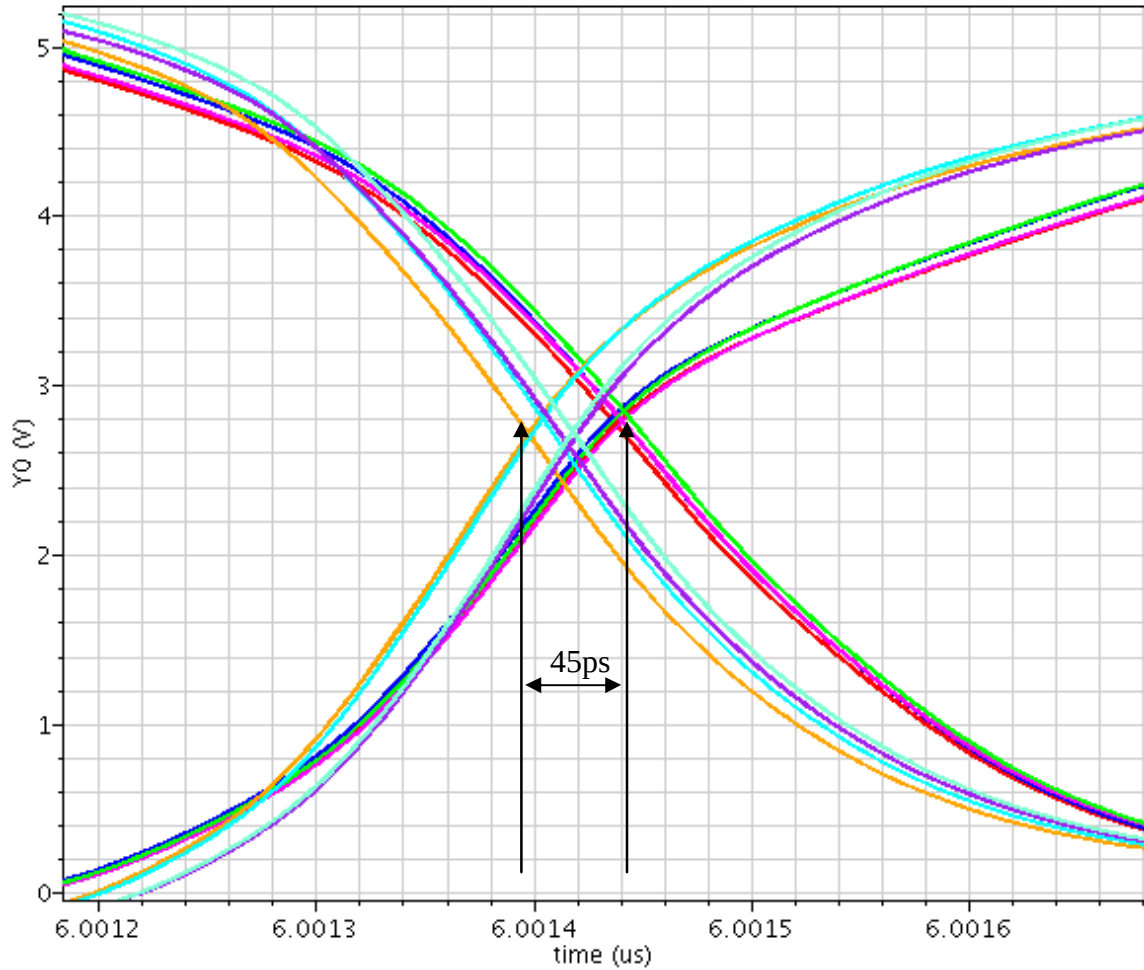


Figure 3.32: ½ Wilkinson Phase Variation

Figure 3.32 shows the total phase variation in the ½ Wilkinson caused by systematic offset in loop and SSN noise for each of the 8 corners of interest. The measured phase variation of 45ps corresponds to 5.4° at 250MHz.

WPLL Loop Stability

Stability analysis for the WPLL can be conducted using a method identical to that in the DLL, namely the loop is broken at the control voltage and a supply is inserted in series such that the loop is allowed to converge and then the supply is stepped to observe the loop step response.

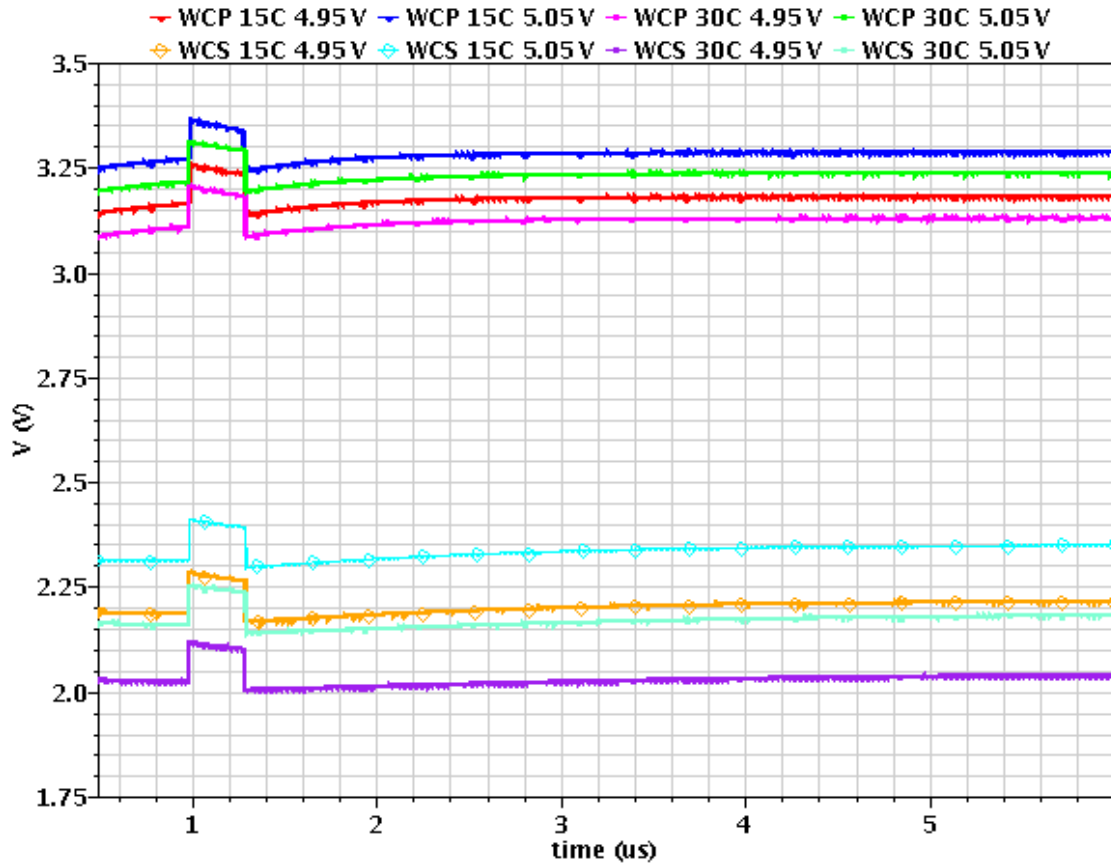


Figure 3.33: WPLL Step Response

Figure 3.33 shows the WPLL_CNTL control voltage as a function of time. At time $t = 250\text{ns}$, a 50mV 250ns pulse with 1ps transition time, is imposed on the control voltage and the loop reacts without oscillation. The characteristic reaction by the loop is that of an over damped system which qualitatively implies there is sufficient if not excessive gain and phase margin.

Like the DLL, the original WPLL design point is most certainly stable but the loop time constant can be reduced by increasing the CP reference current and subsequently the total loop gain.

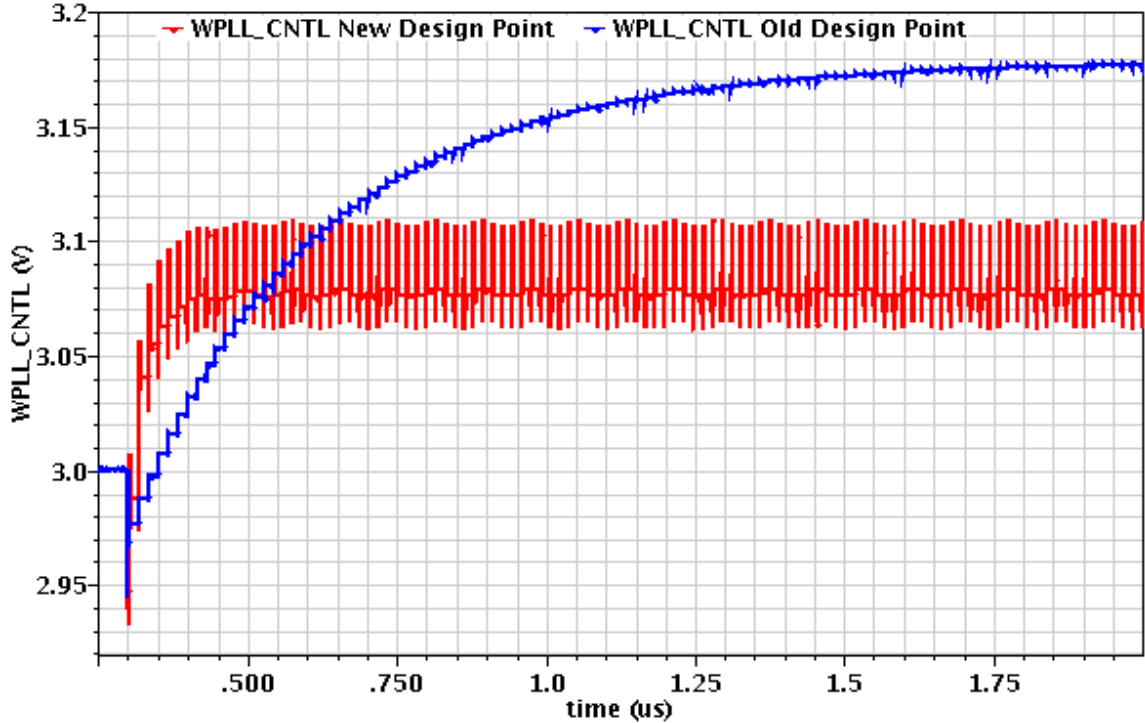


Figure 3.34: Original and Modified WPLL response for WCP, 15°C, $V_{DD} = 5.05V$

Figure 3.34 shows the WPLL response for the PVT corner that has the fastest loop response (WCP, 15°C, $V_{DD} = 5.05V$). The PVT corner representing the fastest loop response was selected for optimization to ensure that under no condition the loop response is under damped. The control voltage, WPLL_CNTL is held constant at 3.0V until time $t = 300ns$ when a switch is opened and the loop is allowed to converge on its steady state value. The blue curve representing the original transfer function of equation [3.20] and response of Figure 3.33 converges much slower than the red curve where the CP reference current, device sizes, and consequently the gain have been increased to the point where the total loop response is critically damped. As in the DLL,

the non-ideal transients seen on WPLL_CNTL, caused by charge injection through switching transistor parasitics in the CP, are much more pronounced in the new design point. The noise on WPLL_CNTL is so great for the critically damped design point the reduction in loop time constant is not worth the resulting increase in phase jitter. In addition, the increase in gain necessary to achieve a critically damped system requires such a large increase in device sizes that the PD sees a much larger capacitive load. This large capacitive load has introduced an offset which can be seen in the differing convergent points. This may be remedied by appropriately resizing the devices in the PD to accommodate a larger load.

Slave Performance

The performance of slave a SCAI compensated by the WPLL control scheme can be simulated in the transient domain or frequency domain which is often times referred to as AC analysis. Transient simulations which tend to more accurately reflect reality; successfully capture the effects of simultaneous switching noise (SSN) on the control voltage WPLL_CNTL and the non-linear behavior of the circuit topology. While they are more accurate, transient simulations are very time and computer resource intensive. Simulations in the frequency domain are much faster and more flexible allowing the designer to simulate many different scenarios in a short amount of time. However, AC analysis relies on simplified or linearized circuit models which don't accurately represent circuit behavior under larger signal conditions. A combination of AC and Transient analysis techniques should be used to verify the desired behavior of a given circuit. Results using both simulation methods are compared in the following sections.

SCAI

The performance of the SCAI can be benchmarked as a standalone circuit by simulating the effective inductance and resistance. The first step requires a transient simulation of the WPLL during which the effective inductance can be measured in the time domain and the converged control voltage WPLL_CNTL can be determined for each process, temperature and voltage corner of interest. The second step involves an AC analysis where the control voltage WPLL_CNTL determine in the first step is used to set the DC operating point and consequently the small signal linear model of the SCAI.

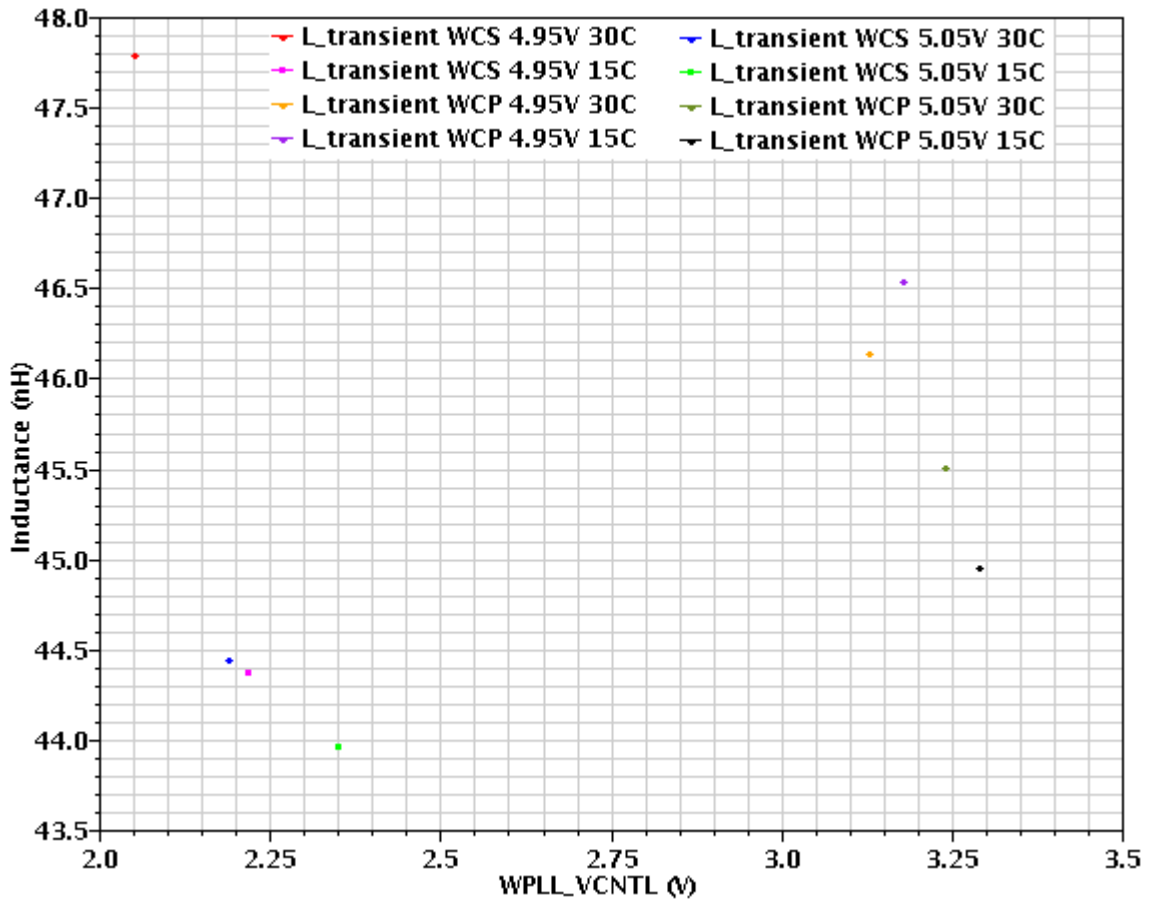


Figure 3.35: Inductance at 250MHz for a Compensated SCAI in the Time Domain

Figure 3.35 shows the effective inductance, derived from a transient simulation, of a slave SCAI for all eight corners of interest. The inductance is calculated using the time variant inductor equation, $v(t) = L \frac{di}{dt}$ and monitoring the instantaneous voltage across and change in current through the SCAI circuit. This calculation method provides the instantaneous inductance which is sampled after the master loop converges to the steady state operating point.

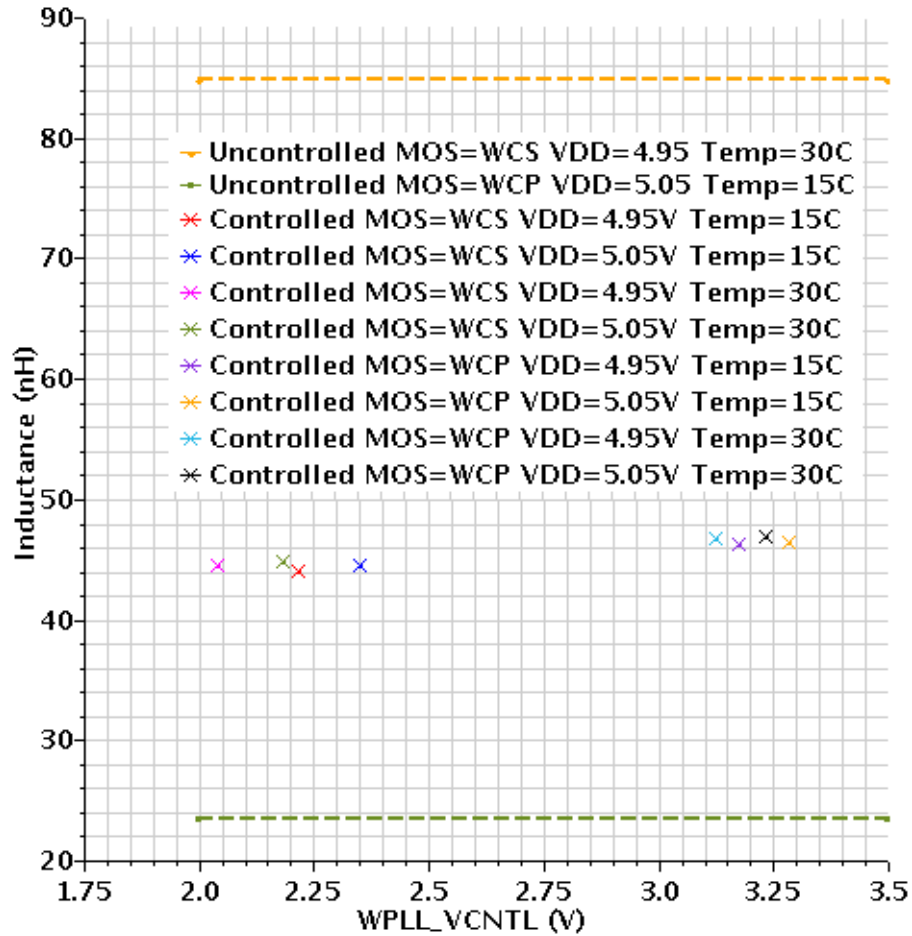


Figure 3.36: Inductance for Compensated & Uncompensated SCAI in the Frequency Domain

Figure 3.36 shows the effective inductance of a slave SCAI for all eight corners of interest as well as the effective inductance of an uncompensated SCAI for the two corners

that bound the inductance range. This AC analysis shows that the WPLL compensation scheme has successfully reduced the effective inductance range of the SCAI across the process voltage and temperature corners of interest from 85nH – 24nH to 46.8nH – 43.8nH respectively. A comparison of AC and Transient simulation methods yields almost identical inductance ranges which validates the AC simulation method.

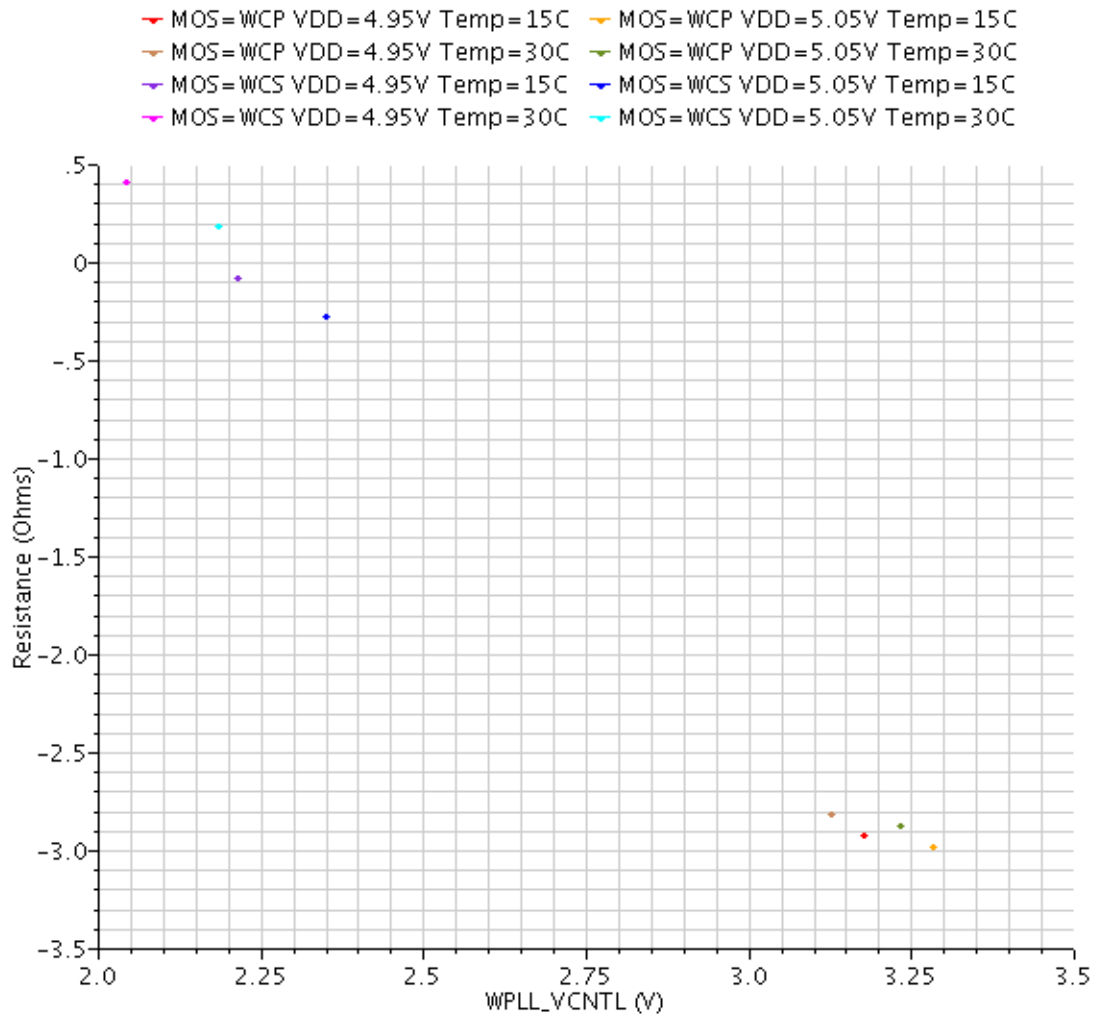


Figure 3.37: Resistance for the Compensated SCAI in the Frequency Domain

Figure 3.37 shows the effective series resistance of a slave SCAI for all eight corners of interest derived from an AC simulation. It is important to note that while

compensating the SCAI does have a small effect on the effective series resistance, the design point of the SCAI in the compensated environment could be further optimized to center the effective series resistance around zero and further maximize the Q at all corners.

Wilkinson

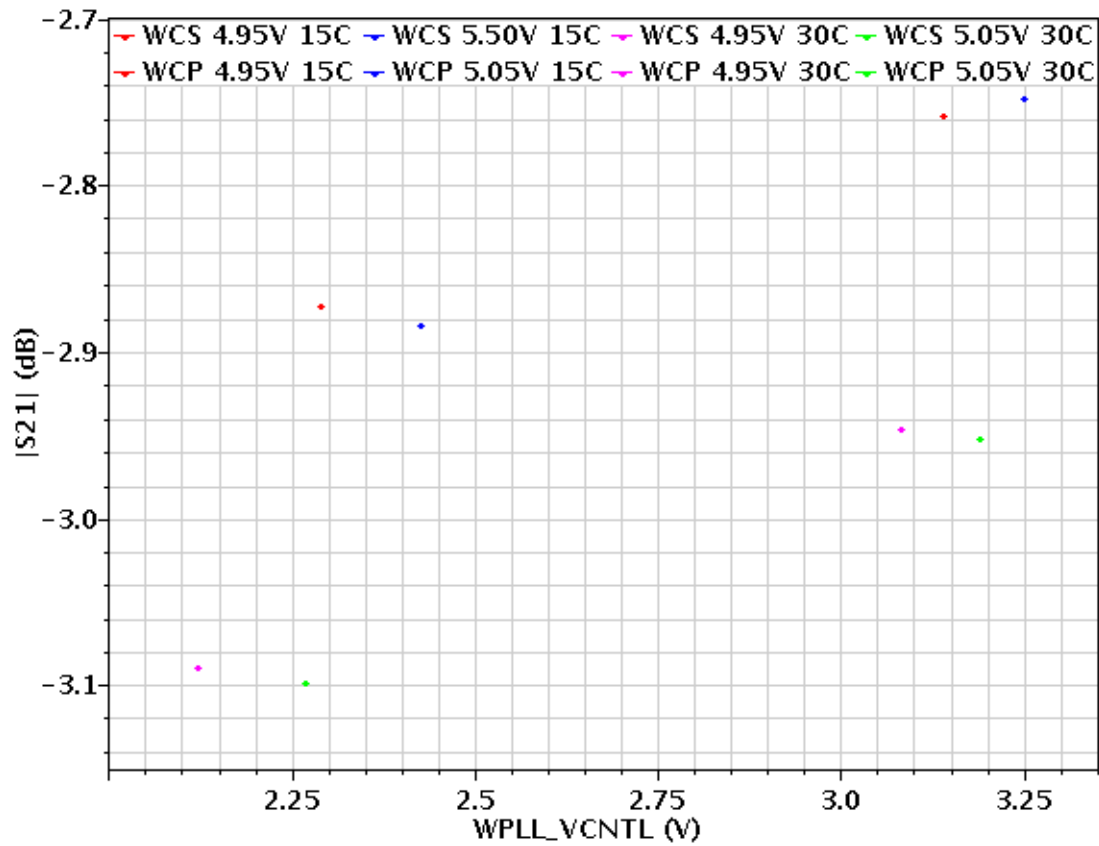


Figure 3.38: $|S_{21}|$ at 250MHz for a Compensated Wilkinson in the Time Domain

Figure 3.38 shows the magnitude of the transmission coefficient S_{21} at 250MHz for a slave Wilkinson over all eight corners of interest as a function of WPLL_VCNTL voltage. During a transient simulation, the S_{21} parameter is calculated by stimulating a slave Wilkinson with a 20mVpp signal at Port 1 and measuring the magnitude and phase

shift of the output signal at Port 2. The magnitude of the input and output signals are then converted from voltage to dB. For the corners where the SCAI has a negative resistance, the resulting $|S_{21}| < -3\text{dB}$ which is a unique characteristic for a Wilkinson composed of one or more active elements.

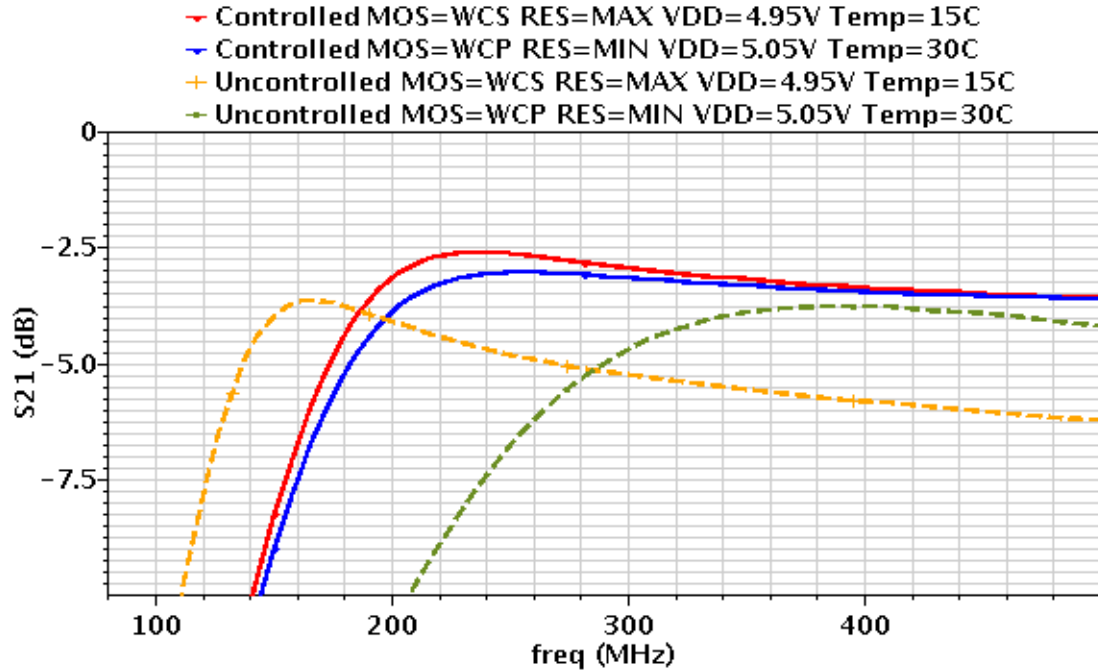


Figure 3.39: $|S_{21}|$ for a Compensated & Uncompensated Wilkinson in the Frequency Domain

Figure 3.39 shows the bounding corners for the transmission coefficient S_{21} of the compensated and uncompensated Wilkinson. This AC simulation shows the WPLL compensation scheme has improved the transmission loss variation at the design frequency of 250MHz from $-6.75\text{dB} - -10.5\text{dB}$ to $-3.1\text{dB} - -2.85\text{dB}$ in addition to significantly reducing the variation of the frequency at which the peak transmission occurs. Again we see the SCAI with negative resistance results in less transmission loss than a typical Wilkinson which implies the SCAI embedded in a Wilkinson could be used to offset resistive losses in the lumped series capacitors. The effects of a negative

resistance on the stability of the Wilkinson will be explored in the next section. Both transient and AC simulation techniques yield almost identical results which further validates the AC analysis method.

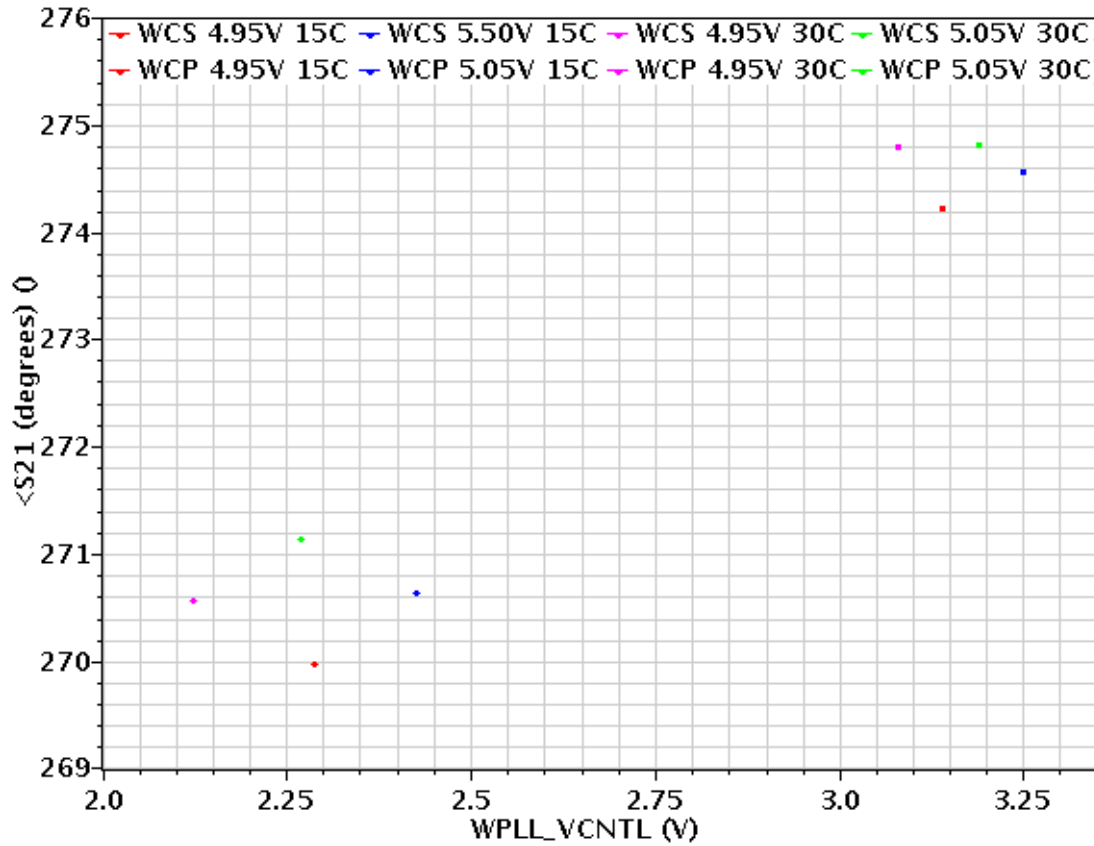


Figure 3.40: $\angle S_{21}$ at 250MHz for a Compensated Wilkinson in the Time Domain

Figure 3.40 shows the phase of the transmission coefficient S_{21} at 250MHz for a slave Wilkinson over all eight corners of interest as a function of WPLL_VCNTL voltage derived from a transient simulation.

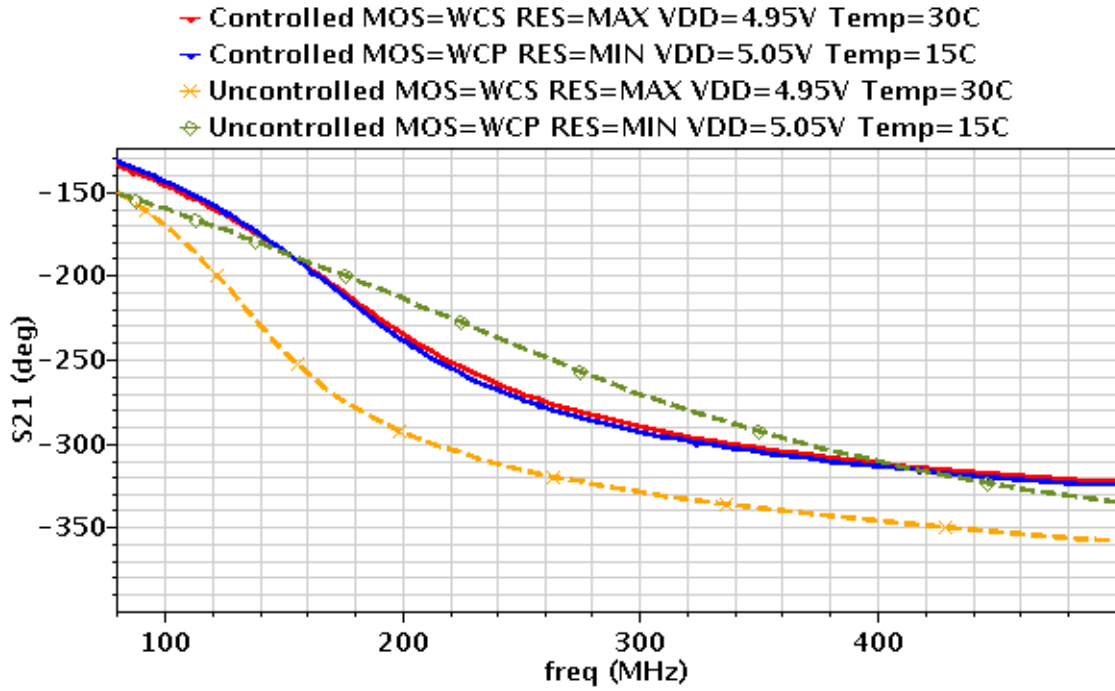


Figure 3.41: $\angle S_{21}$ for Compensated & Uncompensated Wilkinson in the Frequency Domain

Figure 3.41 shows the bounding corners for the transmission coefficient S_{21} phase for a compensated and uncompensated Wilkinson. This AC simulation shows the WPLL compensation scheme has improved the phase variation at the design frequency of 250MHz from 243° - 315° to 269° - 275° . Transient and AC analysis results match very closely.

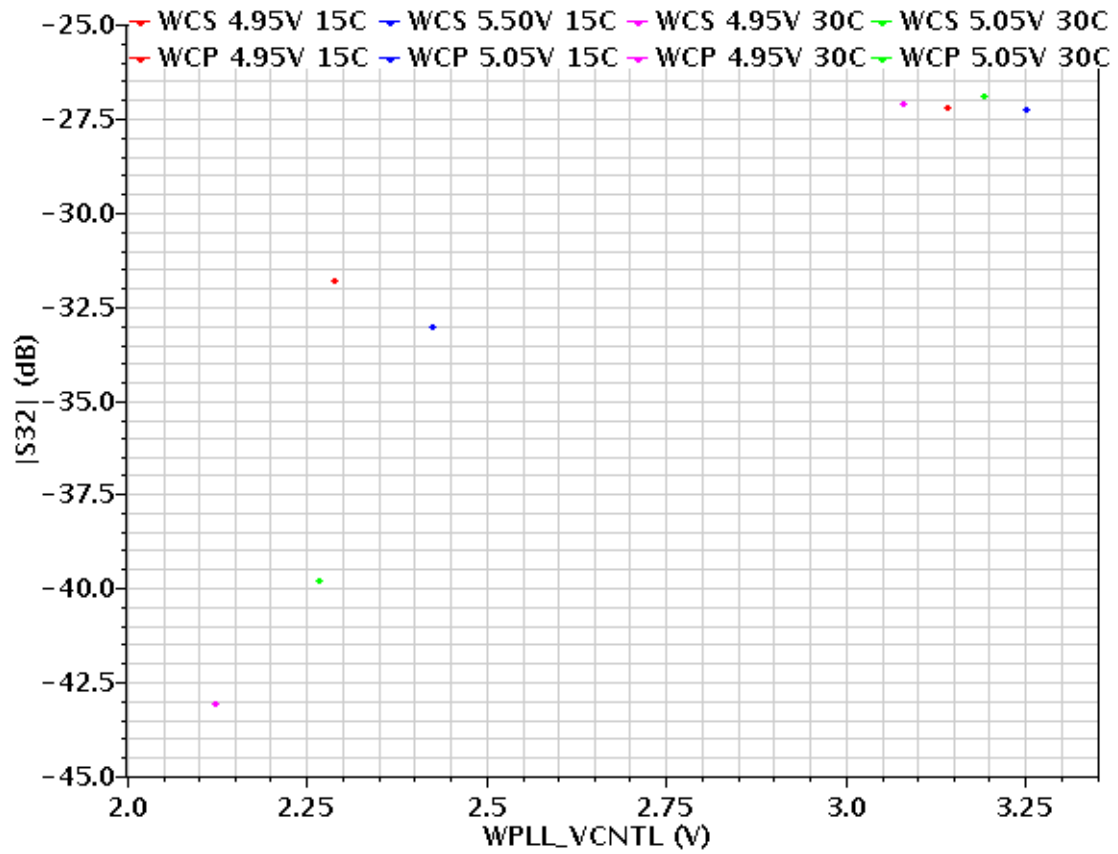


Figure 3.42: $|S_{32}|$ at 250MHz for a Compensated Wilkinson in the Time Domain

Figure 3.42 shows the magnitude of the isolation coefficient S_{32} at 250MHz for a slave Wilkinson over all eight corners of interest as a function of WPLL_VCNTL voltage derived from a transient simulation.

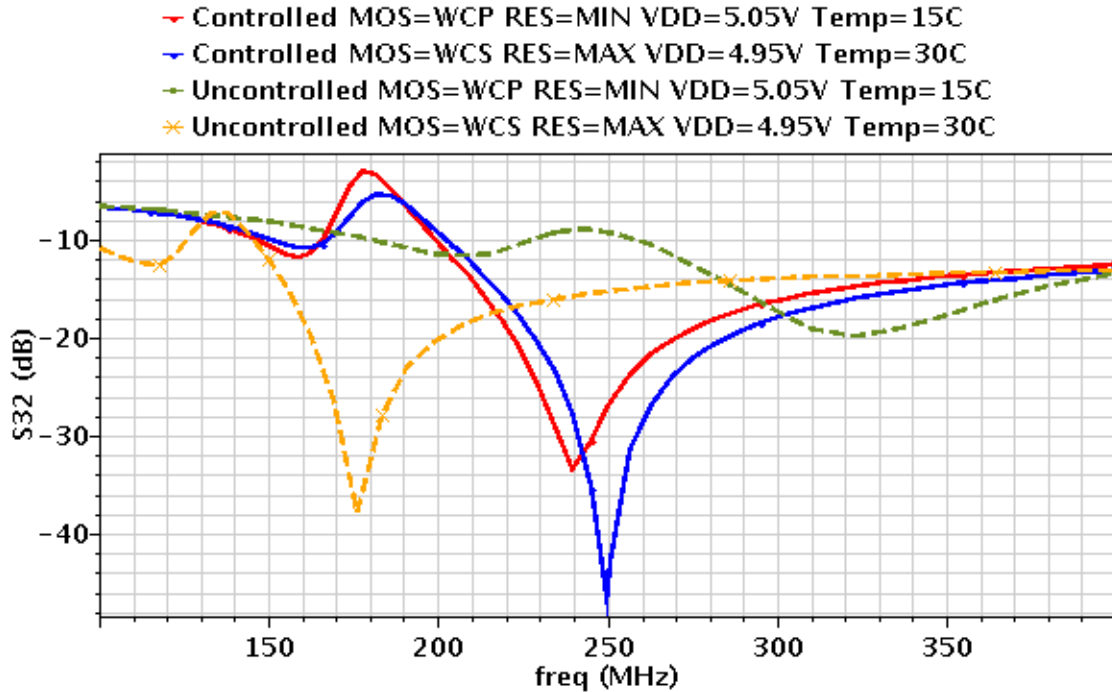


Figure 3.43: S_{32} for Compensated & Uncompensated Wilkinson in the Frequency Domain

Figure 3.43 shows the bounding corners for the isolation coefficient S_{32} for a compensated and uncompensated Wilkinson. This AC simulation shows the WPLL compensation scheme has improved the minimum isolation at the design frequency of 250MHz from -9.3dB to -26.4dB in addition to significantly reducing the variation of the frequency at which the best isolation occurs. A comparison between transient and AC simulation methods yields slightly differing results. This difference is largely an artifact of the unit (dB) used during the comparison. A comparison in the voltage domain yields a difference of only a few millivolts.

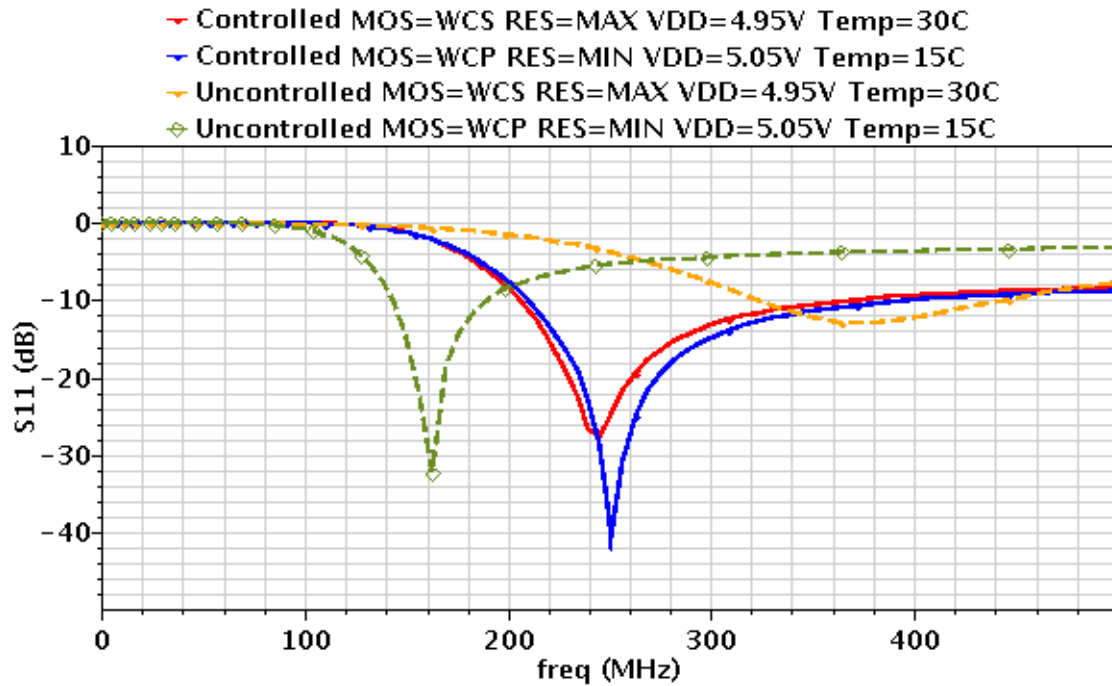


Figure 3.44: S_{11} for Compensated & Uncompensated Wilkinson in the Frequency Domain

Figure 3.44 shows the bounding corners for the reflection coefficient S_{11} for a compensated and uncompensated Wilkinson. This AC analysis shows the WPLL compensation scheme has improved the maximum reflection coefficient at the design frequency of 250MHz from -1.8dB to -24.8dB in addition to significantly reducing the variation of the frequency at which the least reflection or best matching occurs. Measuring the reflection coefficient in the time domain requires a directional coupler Spectre model which is not currently available in the Cadence design suite. As a result it is not possible to compare simulation methods for the S_{11} parameter. However, agreement between the two methods has been shown for S_{21} and S_{32} .

Wilkinson Stability Analysis

Potential for instability arises in a multi-port network when either the input or output impedance has a negative real component. This indicates the magnitude of the

corresponding reflection coefficient is positive or that reflected signals are actually amplified. The impedance of the source or load network is not always well defined during the design process and guaranteeing unconditional stability is a good design practice. This can be achieved by plotting source and load stability circles on a Smith chart thereby defining the source and load impedance stability boundary conditions at one frequency.

As discussed previously, the unloaded SCAI is intentionally tuned such that the real component of the input impedance or the effective series resistance is minimized thus providing the highest possible Q . This design approach inherently results in a few corners (typically the fast transistor corners) where the effective series resistance is negative and the unloaded SCAI is unstable. While oscillation is possible when the SCAI is unloaded, a very small resistive load is typically enough to stabilize the circuit.

A traditional Wilkinson implemented with either lumped elements or distributed transmission lines will be unconditionally stable under all passive loads and source impedances because there are no active elements in the circuit. However, for the case of the lumped Wilkinson with embedded SCAI, unconditional stability is not guaranteed because of the active devices (transistors) comprising the SCAI. While it is highly unlikely that the real component of the impedance could be negative enough to induce oscillation when loaded by the series capacitors in the Wilkinson, it is good design practice to define the boundary of instability. Load and Source stability circles provide a method to determine the source and load impedance values that will result in a stable 2-port system. The Wilkinson is a 3-port network so for the following stability analysis,

port 1 is assumed to be the input, port 2 is assumed to be the output, and port 3 is terminated with a 50Ω resistor.

— LSB WCS 4.95V 15C — LSB WCS 5.05V 15C — LSB WCS 4.95V 30C — LSB WCS 5.05V 30C
 — LSB WCP 5.05V 30C — LSB WCP 4.95V 30C — LSB WCP 4.95V 15C — LSB WCP 5.05V 15C
 rho = 3

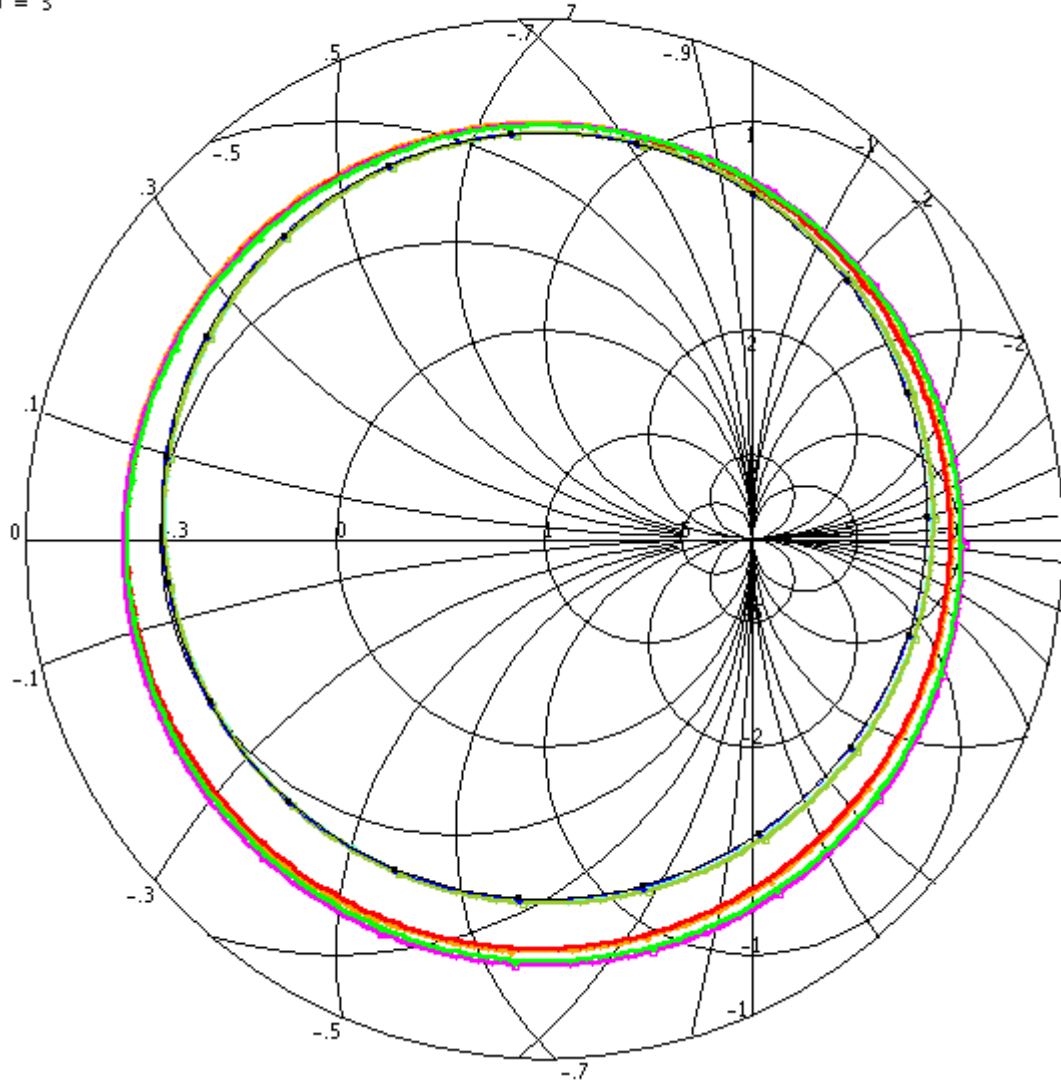


Figure 3.45: Load Stability Circles for a Compensated Lumped Wilkinson at 250MHz

Figure 3.45 shows the load stability circles of the compensated Lumped Wilkinson for the 8 corners of interest at 250MHz on a scale normalized to a 50Ω system. Load impedances represented by the area outside of the circles will result in

instability and oscillation because $S_{11} < 0\text{dB}$ at the design frequency of 250MHz. From these circles, one can conclude the compensated Lumped Wilkinson is stable for all passive loads at 250MHz.

✕ SSB WCS 4.95V 15C ✖ SSB WCS 5.05V 15C + SSB WCS 4.95V 30C ✕ SSB WCS 5.05V 30C
 ◆ SSB WCP 5.05V 30C ✕ SSB WCP 4.95V 15C + SSB WCP 4.95V 30C ✖ SSB WCP 5.05V 15C
 rho = 3

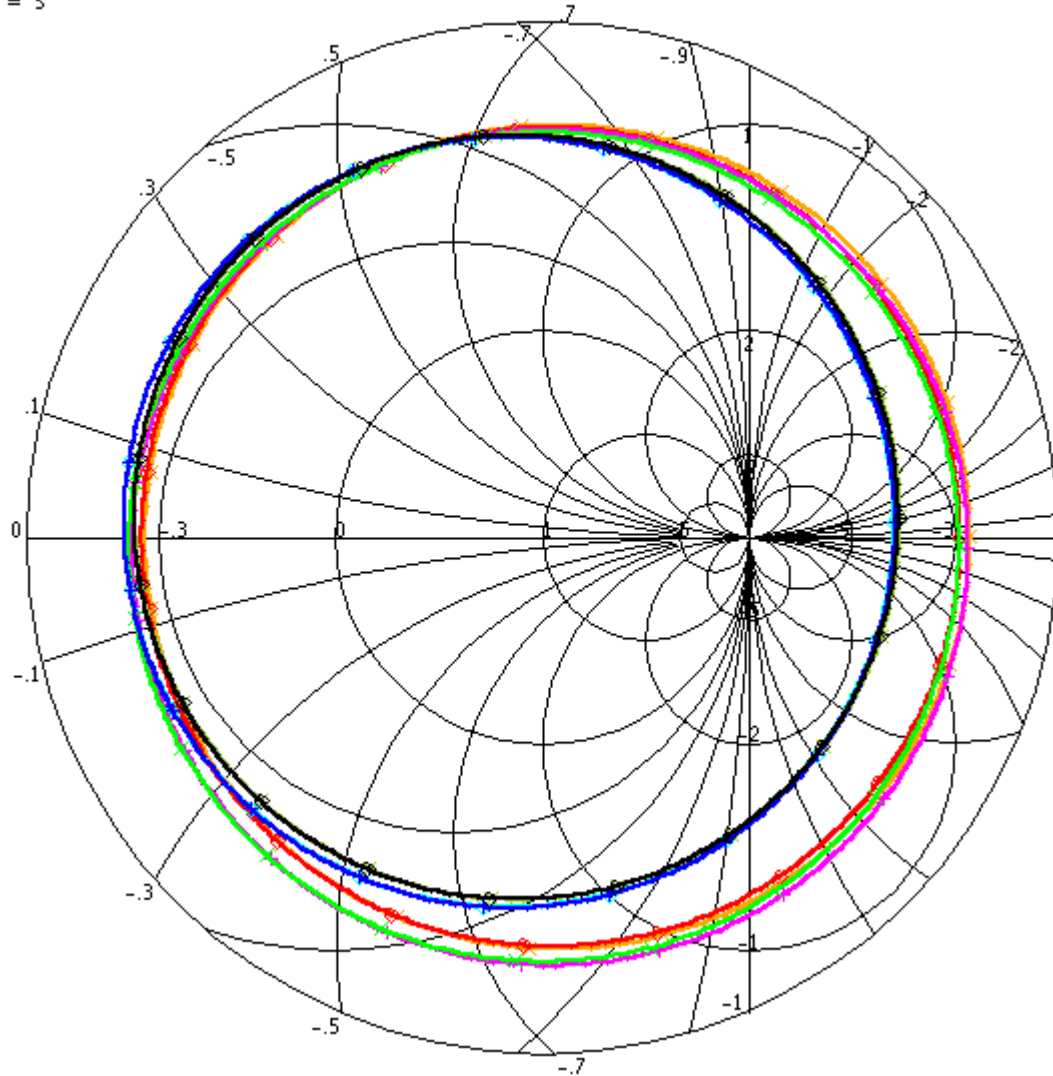


Figure 3.46: Source Stability Circles for a Compensated Lumped Wilkinson at 250MHz

Figure 3.46 shows the source stability circles of the compensated Lumped Wilkinson for the 8 corners of interest at 250MHz on a scale normal normalized to a 50Ω

system. Source impedances represented by the area outside the circles will result in instability and oscillation because $S_{22} < 0\text{dB}$ at the design frequency of 250MHz. From these circles, one can conclude the Lumped Wilkinson is stable for all driving networks that have positive real input impedance at 250MHz.

Wilkinson Input Power Limitations For A Compensated Wilkinson

The power limitations and distortion associated with the SCAI were first broached in Chapter 1 and then observed in hardware that was characterized in Chapter 2. This section will further analyze the degradation of the S_{21} and S_{32} S-parameters in the compensated slave Wilkinson caused by power limitations associated with the SCAI.

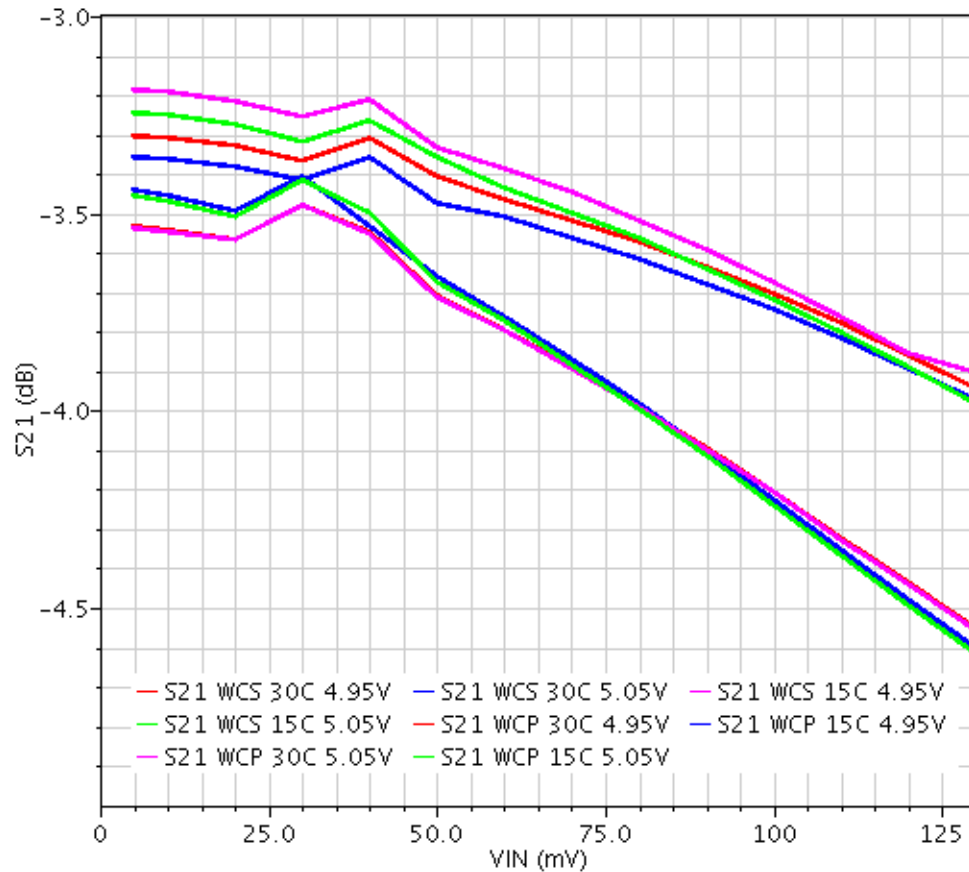


Figure 3.47: $|S_{21}|$ Transmission Coefficient Vs Input Signal Magnitude for a Slave Wilkinson at 250MHz

Figure 3.47 shows the relationship between the input signal magnitude and the magnitude of the transmission coefficient for a slave Wilkinson operating at 250MHz over all 8 corners of interest. A significant deviation from ideal behavior is observed at input signal levels greater than 80mVpp.

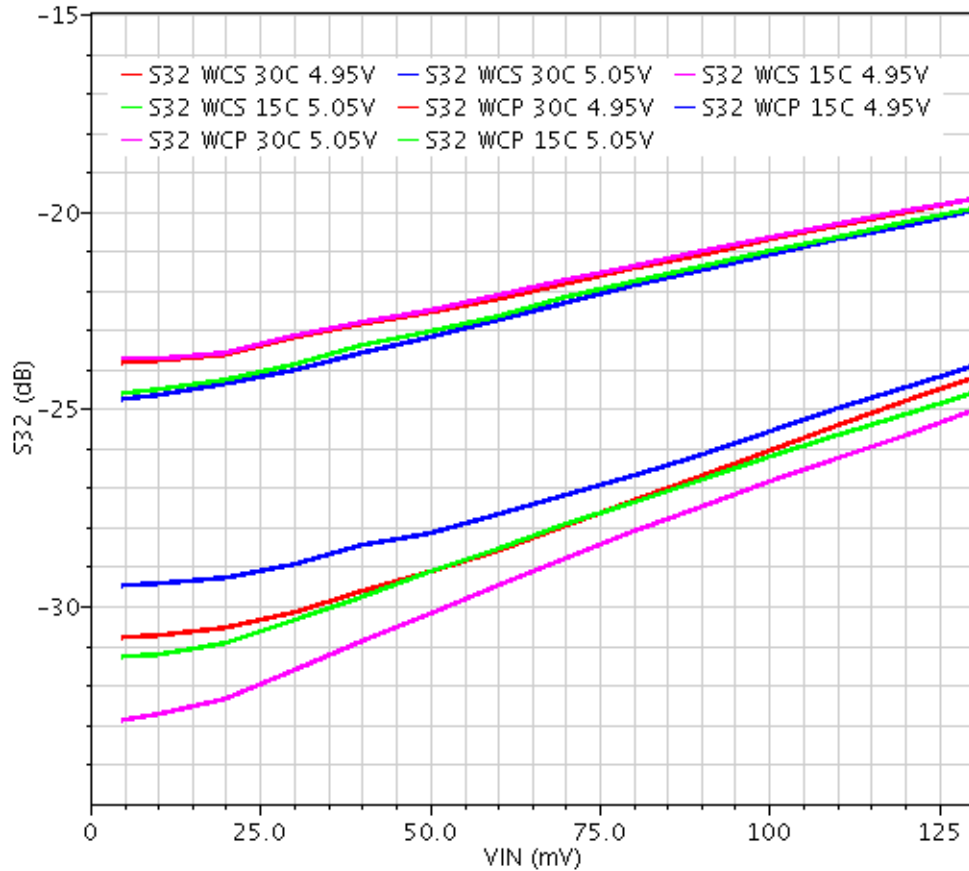


Figure 3.48: $|S_{32}|$ Isolation Coefficient Vs Input Signal Magnitude for a Slave Wilkinson at 250MHz

Figure 3.48 shows the relationship between the input signal magnitude and the magnitude of the transmission coefficient for a slave Wilkinson operating at 250MHz over all 8 corners of interest. A significant deviation from ideal behavior is observed at input signal levels greater than 80mVpp but isolation levels remain sufficient for input levels less than 130mVpp.

Current Consumption

Sub-Cell Name		DC/Average Current (mA)		Peak Current (mA)		Comments
		Min	Max	Min	Max	
DLL at 100MHz	Current Starved Inverters	6.09	6.26	9.32	11.00	Includes All Current Starved Inverters and Bias Generator
	Phase Detector	0.566	0.679	1.79	2.85	
	Charge Pump	0.186	0.207	0.313	0.361	
	Input	-8×10^{-4}	-6×10^{-4}	1.68	2.13	Digital clock signal peak current occurs during transition
	Total Consumed	6.86	8.41	9.72	11.75	Total Consumed is not sum of individual Peak Currents
WPLL at 250MHz	½ Master Wilkinson	26.71	28.12	26.80	28.21	
	Amplifiers	12.90	21.90	13.30	22.50	Includes both Amplifiers
	Delay Line & Current Starved Inverters	6.06	6.55	9.01	9.43	Includes Delay Line and other misc. Current Starved Inverters
	Frequency Divider	1.32	1.58	3.37	5.55	
	Phase Detector	0.363	0.434	1.79	2.81	
	Charge Pump	0.185	0.206	0.312	0.361	
	Input	-2×10^{-5}	-8×10^{-6}	0.173	0.217	
	Total	72.82	82.83	79.60	86.30	Total Consumed is not sum of individual Peak Currents
Slave Wilkinson	SCAI	26.72	28.12	27.20	28.56	
	Input	-2×10^{-5}	-8×10^{-6}	0.173	0.217	
	Total	26.72	28.12	27.20	28.56	Total Consumed is not sum of individual Peak Currents

Table 3.2: DC Power For the WPLL Simple Cascoded Active Inductor Compensation Scheme

The WPLL Simple Cascoded Active Inductor Compensation Scheme consumes a significant amount of power so it is important to understand which portions of the circuit consume the most power.

Table 3.2 shows the DC or average and the instantaneous current demands for each sub-circuit as well as the total compensation scheme. Simulations were run over each of the 8 corners of interest to determine the appropriate ratings. The effective power can be calculated by multiplying the current value by the supply voltage.

Physical Size

Depending on the technology, and desired inductance, an argument could be made that the stand-alone SCAI yields a higher inductance per unit area than its spiral counterpart. However, if active compensation is deemed necessary to control inductance the tolerance, the benefit of the SCAI from a physical area perspective is in question.

	Poly Resistor Area (μm^2)	Poly Capacitor Area (μm^2)	NMOS Area (μm^2)	PMOS Area (μm^2)	Total Area (μm^2)
100MHz DLL	1200	0	800.4	2242.8	4243.2
250MHz WPLL	2274.94	39204	3959.47	2488.9	47927.33
Slave Wilkinson	640	39204	2418.80	136.8	42399.60
Total	4114.94	78048	7178.67	4868.5	94570.11

Table 3.3: WPLL Area Breakdown

Table 1.1 shows the area breakdown on a per device type basis for a compensated SCAI including the WPLL compensation scheme. Obviously the inductance per unit area for the compensated SCAI becomes more attractive as the number of slave SCAI's increases.

While spiral inductors are not readily available in the AMIS C5 design kit, Ross [10] designed and characterized his own 10nH spiral inductor which had a diameter of 447.7 μm and an area of 159,043 μm^2 . A comparison between Ross's spiral and Table 3.3 suggests the compensated SCAI represents a significant area savings in the AMIS C5 technology.

CONCLUSION AND SUGGESTED FUTURE RESEARCH

Summary

This research has focused primarily on analyzing the Simple Cascoded Active Inductor (SCAI) to determine its practicality as an alternative to Spiral Inductors for use in on-chip lumped Wilkinson power dividers. Prior research in the area of active inductors has shown the topology can successfully be implemented in a fraction of the physical space required by its spiral counterpart; however the impact of Process, Voltage and Temperature variation was not adequately explored such that tradeoffs between a spiral and active inductor are obvious to a design engineer. This research explores the SCAI topology quantifying and comparing performance using figures of merit common to all lumped inductors such as inductance variation ΔL and quality factor Q across a reasonable PVT window. Other non-idealities associated with the SCAI and its incorporation as a lumped element into a Wilkinson power divider are explored and characterized in detail with the main impact being active device induced distortion. The relationship between L and Q variation and the Lumped Wilkinson's S-parameters were used to define the maximum allowable inductance variation (ΔL_{MAX}) and minimum allowable Quality factor (Q_{MIN}). These definitions help quantify the usefulness of the SCAI as the inductive component in the Lumped Wilkinson and highlight characteristics that need improvement. To solve some of the pitfalls associated with the SCAI, a modification to the Regulated Active Inductor (RAI) is proposed. The inability of the

stand alone SCAI and RAI topologies to meet the ΔL_{MAX} requirements confirms the necessity of an active compensation scheme for the SCAI.

The Bobcat_V0 test chip was designed and manufactured in the AMIS C5 0.6 μ m CMOS technology to verify the functionality and performance of key components to be used in an on-chip master-slave active compensation scheme for the SCAI. The accuracy of measurements was verified and the impact of the measurement network on results was quantified through the comparison of simple lumped components and calibration standards. The standalone SCAI was characterized and a method for controlling inductance through the I_1 bias current was confirmed. A 250MHz Lumped Wilkinson was characterized and the necessity of a quality RF ground in future implementations was reinforced.

An on-chip master-slave compensation scheme called the Wilkinson Phase Lock Loop (WPLL) was proposed to control the SCAI inductance variation and meet the defined ΔL_{MAX} . The WPLL compensates the SCAI inductance by monitoring and comparing the S_{21} phase of a master Lumped Wilkinson to a phase reference developed using a Delay Lock Loop and Delay Line. The control feedback voltage can be used by any number of slave SCAI in various circuits across chip. Each sub circuit in the control loop was individually characterized in simulation to determine the open loop transfer function at the design frequency of 250MHz. The closed loop behavior of the DLL and WPLL were analyzed determine the sensitivity at various places in the loop to noise error. Finally, the performance of a slave Wilkinson and SCAI were analyzed through simulation.

		Specification	Uncontrolled	Controlled
45 nH SCAI	$\Delta L(\text{nH})$	53.94 – 39.06 $46.5 \pm 16\%$	85 – 24 $46.5 \pm \begin{smallmatrix} 82.8\% \\ 48.4\% \end{smallmatrix}$	46.8 – 43.8 $46.5 \pm \begin{smallmatrix} 0.6\% \\ 5.8\% \end{smallmatrix}$
	Q_{LMIN}	15	26.1	24.47
250 MHz Lumped Wilkinson	$ S_{11} _{\text{MAX}} (\text{dB})$	-15	-1.8	-24.8
	$ S_{32} _{\text{MAX}} (\text{dB})$	-15	-9.3	-26.4
	$ S_{21} _{\text{MIN}} (\text{dB})$	-3.5	-10.5	-3.1
	$\Delta \angle S_{21} (^{\circ})$	$270^{\circ} \pm 5\%$	$315^{\circ} - 243^{\circ}$ $270^{\circ} \pm \begin{smallmatrix} 16.67\% \\ 10\% \end{smallmatrix}$	$275^{\circ} - 269^{\circ}$ $270^{\circ} \pm \begin{smallmatrix} 1.85\% \\ 0.37\% \end{smallmatrix}$

Table 4.1: Summary and Comparison of Uncontrolled and Controlled SCAI and Lumped Wilkinson

A performance comparison between a controlled and uncontrolled SCAI and Wilkinson is summarized in Table 4.1. Source and Load stability analysis was conducted through simulation to fully understand the implications to the Wilkinson network of a potential negative SCAI resistance under some PVT conditions. Finally, the average power consumption of the Master and Slave networks was determined through simulation.

The simulated results of the WPLL, compensated SCAI and compensated Lumped Wilkinson in the transient, frequency and S-parameter domain show the active compensation scheme can significantly improve the tolerance of the SCAI and on-chip Lumped Wilkinson in addition to providing a lumped inductor with a quality factor Q much greater than spiral inductors in most low cost CMOS technologies.

The concept of negative resistance or amplification in a lumped element is rather intriguing. In theory, a negative resistance in one element could balance or compensate the unfavorable effects of a positive resistance in another such that the total impedance of a reactive network has no real component. Chapter 3 discusses a method for maximizing the SCAI quality factor Q by centering the effective series resistance around zero across a defined PVT window. This method could be expanded or modified to include the total series resistance of a multi-component network such that the Q of the total network is maximized.

The SCAI also shows promise as a tunable component due to the relationship between inductance and the I_1 bias current as discussed in chapters 1 and 2. In fact, the WPLL compensation scheme can be used to tune slave SCAI to a variety of different inductive values by varying the frequency of the DLL reference signal and DL propagation delay.

Potential Improvements to the Existing WPLL Compensation Scheme

While the basis for a compensated SCAI has been shown with the existing WPLL topology and manufacturing hardware is clearly the next step in the verification process, there are a multitude of improvements that could be made and should be eventually incorporated into the existing design. The following sections discuss areas of the existing design that may need further simulation based characterization and/or optimization.

Supporting Industry Standard PVT Specifications

As discussed in chapter 2, a relaxed temperature and voltage range was used during the design process of the Bobcat_V0 test chip and the WPLL compensation scheme. These specifications were relaxed, partially due to the controlled environment in the MSU laboratory, and also to expedite the design process and facilitate proof of concept. Now that proof of concept has been shown in simulation, the compensated SCAI would appear much more attractive with a more realistic voltage and temperature range compliant to more stringent industry specifications ($V_{DD} = 5V \pm 10\%$, Temperature = $-20C - 100C$). All of the digital, as well as a majority of the analog circuitry should have no issues operating over expanded temperature and voltage ranges but there are two portions of the topology which may need adjustment.

The Delay Buffer (DB) in the DLL does not have an acceptable dynamic delay tuning range over an extended temperature and voltage specification and will need to be tuned appropriately. If the DLL cannot adjust DLL_PBIAS such that $T_{DEL_CSI} = 250ps$, the result is a systematic offset in the Delay Line (DL) used as a phase reference in the WPLL control loop. Recall Figure 3.10 which was used to set the delay through a single CSI, $T_{DEL_CSI} = 250ps$; extending the temperature and voltage range will require changes to device dimensions and may even require a change in the number of CSI in the DB if $T_{DEL_CSI} = 250ps$ is not achievable.

The SCAI which is embedded in the Master $\frac{1}{2}$ Wilkinson may need to be fine tuned to optimize the dynamic inductance tuning range for use over an expanded voltage and temperature range.

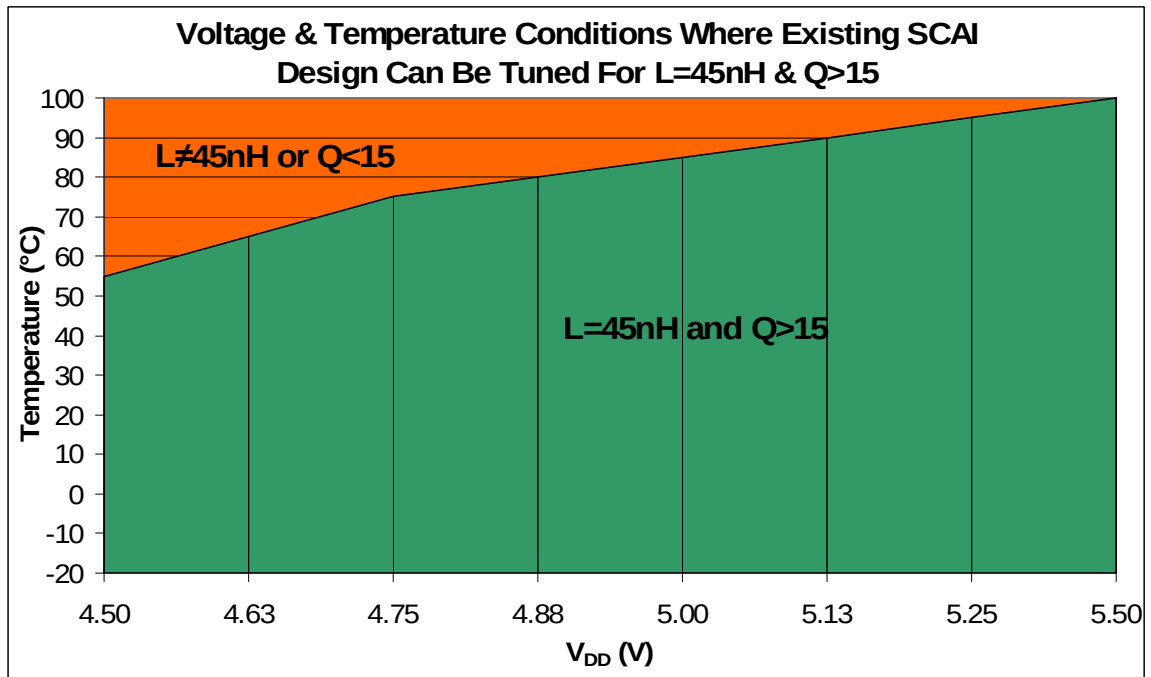


Figure 4.1: Temperature & Voltage Conditions Where Existing SCAI Design Can Be Tuned For 45nH & $Q < 15$

Figure 4.1 shows the temperature and voltage conditions over which the existing SCAI design can be tuned and meet the criteria defined in Table 1.1. While the voltage and temperature range supported by this particular SCAI design point is significantly wider than that defined in Table 1.2, some adjustments would be needed to support the typical industry specification. All of the failing voltage and temperature conditions occur in the WCS process corner indicating it should be possible to tune the SCAI and support an expanded temperature and voltage ranges.

Characterizing the Effect of Device-to-Device and Across Chip Variation

The WPLL compensation scheme, like all master slave control loops, suffers from the inability to compensate for across chip variation or device- to- device mismatch. This effect can be minimized if master and slave devices are localized and good physical design practices are followed. It is possible to hand calculate the contribution of device-to- device mismatch to the overall system tolerance using mismatch information typically provided in device models and design manuals. However, a manual calculation including each device in a circuit this complex would be extremely prone to error. Clearly the only reasonable method is full Monte Carlo simulation analysis. In fact, even the practicality of a simulation based approach is limited by the size of this circuit and available computing resources. This limitation has forced a corners based design approach that should eventually be augmented with Monte Carlo analysis.

The SCAI and Noise

The effect of thermal and flicker noise from the SCAI on the lumped Wilkinson has not been analyzed. Admittedly, the noise in combination with well characterized signal strength limitations could make the usable input power range small enough to question the practicality and usefulness of the SCAI as a design component. In addition to the effect of noise from the SCAI on a higher level network, the effect of noise from the WPLL compensation scheme on slave a SCAI should be well understood and characterized.

Power Supply Rejection Ration (PSRR)

It is essential to understand the effect of power supply noise and non-idealities on the tolerance of the WPLL compensation scheme. A majority of the sensitive analog blocks should reasonably reject supply noise because devices connected to the supply operate in the saturated region and don't present a low impedance path to sensitive nodes. However, purely digital blocks such as the phase detectors and frequency dividers will be sensitive to supply noise. PSRR analysis will identify sensitive portions of the topology, help define supply requirements and determine if off chip supply filters are necessary. Accurate modeling of the supply network can help determine the amount of on-chip decoupling capacitance necessary to minimize the effects of supply noise.

Improved WPLL Operational Amplifier

As discussed in Chapter 4, the Operational Amplifier could potentially be improved or optimized with a less sophisticated design approach because the common mode of the input signals seen by both amplifiers are set by the 50Ω thevenized terminating network to a constant $V_{DD}/2$. The wide common mode capabilities of the existing amplifier front-end may be traded for higher gain and more sensitivity to support a lower WPLL input reference signal strength such that the compensated SCAI operates in a more ideal manner.

DLL & WPLL Lock Signals, Initialization and Reset Circuitry

The WPLL contains two control loops, the Master Wilkinson loop and the DLL, the first of which is dependent on the other. To prevent unintended interaction between

the two loops, a fully automated startup or reset sequence should consist of the following steps.

1. Initialize the DLL control feedback (DLL_PBIAS in Figure 3.8) and WPLL control feedback (WPLL_CNTL in Figure 3.5) to the proper startup voltages and flush the flip-flops in the Frequency Dividers
2. Enable the DLL and wait for it to “Lock” or converge on its steady state operation point
3. Enable the Master Wilkinson Loop and wait for it to “Lock” or converge on its steady state operation point

The steady state operating point, often referred to as “Lock”, in both the Master Wilkinson Loop and DLL can be identified when there is a minimal amount of phase error between the feedback and reference signals of each phase detector. A WPLL “Lock” signal could be used to notify any slave SCAI that the control voltage is ready (or not ready) to be used. There is a multitude well known lock detection circuits that adequately provide the functionality discussed above but they will not be addressed in this research.

An auto-reset circuit for the WPLL may also be desired to detect a situation where the Master Wilkinson loop cannot recover from some unforeseen catastrophic event. This type of circuit would detect the situation where the WPLL control voltage (WPLL_CNTL) approaches either edge of the charge pumps functional output voltage range. Resetting the Master Wilkinson loop consists of setting WPLL_CNTL to the startup value of $V_{DD}/2$ and flushing the flip-flops within the in the Frequency Dividers similar to step one of the initialization sequence above.

WPLL Reference Signals

As defined in chapter 3, the WPLL topology requires two input reference signals, a 100MHz digital reference for the DLL and a 250MHz small signal sine wave for the master Wilkinson control loop.

The DLL Reference Signal: The 100MHz digital DLL reference can easily be derived from an off-chip crystal oscillator using techniques common to all on-chip PLL reference generation. Any frequency distortion on the DLL reference signal will have a direct negative impact on the DLL phase jitter which in turn will have a direct negative impact on the WPLL phase jitter and the overall SCAI inductance tolerance.

The Master Wilkinson Reference Signal: Thus far, all simulations and development of the WPLL assume an ideal 80mVpp 250MHz sine wave reference. Frequency distortion of this signal will certainly have a negative impact on the overall inductance tolerance of compensated SCAI. The Master Wilkinson Reference Signal could be accurately generated off-chip but care must be taken during the transmission of the signal on-chip to minimize corruption and introduction of erroneous frequencies. Another approach would generate the WPLL reference signal on chip but the quality of the signal may be limited by the lack of a decent on-chip inductor and sine wave generator.

Recommendations for Future workThe Modified Regulated AI & Compensation Scheme

A further complicated Enhanced Regulated Active Inductor compensation scheme could be developed to control the series resistance and quality factor in addition to the effective inductance. This scheme would incorporate a third control loop to operate on the series resistance of the ERAI in addition the circuitry contained in the existing WPLL. The effective series resistance of the ERAI could be monitored by comparing the magnitude of a signal propagated through a Master Wilkinson to a reference generated with a 3dB resistive attenuator similar to the circuit already contained in the Master Wilkinson Loop. As discussed in Chapter 1, the effective resistance of the ERAI can be independently tuned using the I_3 reference current of Figure 1.21. The disadvantages and complexity of a compensation scheme where the interaction of three control loops would need to be well understood may far outweigh the benefits.

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