

ON-CHIP AUTOMATIC TUNING OF CMOS ACTIVE INDUCTORS FOR USE
IN RADIO FREQUENCY INTEGRATED CIRCUIT (RFIC)
APPLICATIONS

By

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ABSTRACT

The lack of high quality factor integrated inductors is a significant impediment to realizing high performance Radio Frequency Integrated Circuits (RFICs) within conventional digital CMOS. While passive spiral inductors continue to improve with different approaches and fabrication techniques, they tend to be large and lossy. Therefore, an accurate inductance with high quality factor and small chip area would be an extremely useful component for RFIC designers. The focus of this thesis is realizing accurate, high-quality factor inductance using an active circuit approach for implementation in RFIC applications. It is demonstrated that, when implemented in a conventional digital CMOS process, the standard active inductor topology suffers greatly, in terms of performance and stability, over the transistor process corners and thus some form of an automatic tuning approach is necessary for these devices to be used reliably. Consequently, a master-slave tuning circuit was designed and included in order to tune the active inductor over the process corners of the AMIS C5 process. Simulated results are presented that verify the functionality of the proposed active inductor topology. In addition, simulation results utilizing an automatically tuned inductor within a two-way lumped element Wilkinson power divider demonstrates the utility of the chosen approach. Considerations for adapting this approach for use in a scaled CMOS process are discussed.

CHAPTER ONE

INTRODUCTION TO HIGH Q RADIO FREQUENCY INTEGRATED
CIRCUIT (RFIC) CMOS APPLICATIONSIntroduction

CMOS has been the dominant integrated circuit (IC) technology for roughly twenty years and continues to encompass research projects and industry applications because of its ease of integration, versatility, low cost and high-performance. Experts predict that CMOS channel lengths will be scaled down to as small as $0.03\mu\text{m}$ and that CMOS will still be a vital process technology for an additional 20 years [9]. As a process technology CMOS offers many appealing qualities to a design engineer or industry-driven company. CMOS allows very high levels of integration, low static power dissipation in digital circuits, complementary-symmetry devices (PMOS and NMOS) on the same die, sufficient gain capabilities and acceptable noise levels among other qualities.

There are many real world RFIC and analog mixed signal applications that are currently being pursued by universities and industry. Some of the most recent developments have involved Silicon CMOS-based high-frequency wideband wireless ICs, RFIC inductors, low-power and low-noise implementations in the form of amplifiers and Phase-Locked Loops (PLLs), faster, better performing data converters, and high-speed switched capacitor networks. This list of topics merely includes the tip of the iceberg of what this industry and research environment encompasses. Several important RF and frequency-dependent applications demand high quality factor inductors including

power dividers, oscillators, and continuous time filters. The following two sections develop the necessity of high-Q inductors in power dividing and oscillator applications respectively. The current lack of high-Q inductors in CMOS provides the motivation for this thesis research.

Two Way Lumped Wilkinson Power Divider

A two-way Wilkinson power divider is a three-port network that divides or combines input signal power. Originally a distributed circuit design for operation at microwave frequencies, the Wilkinson divider may be realized in lumped element form. An example of such a lumped element equivalent is given in Figure 1.1.

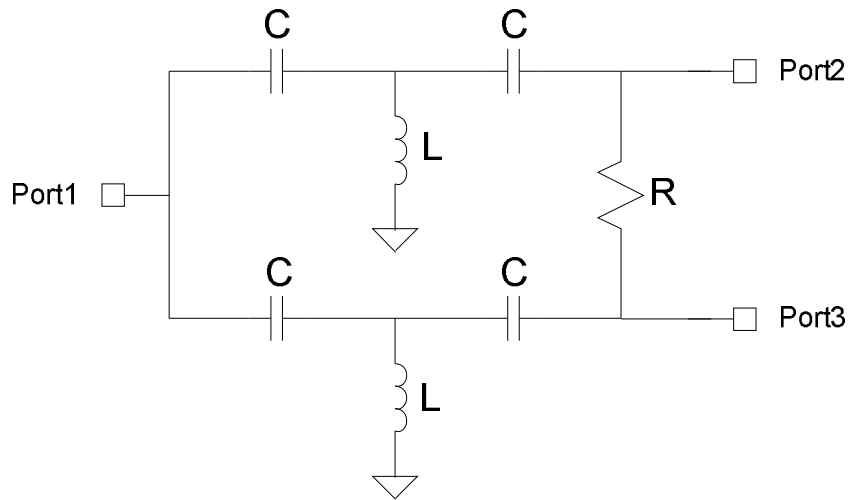


Figure 1.1: Lumped Wilkinson power divider topology.

Given a system impedance (Z_0) to match to and a design frequency (ω), the necessary L s, C s and R can be easily calculated as follows [1]:

$$L = \frac{\sqrt{2}Z_0}{\omega} \quad [1.1]$$

$$C = \frac{1}{\sqrt{2}\omega Z_0} \quad [1.2]$$

$$R = 2Z_0 \quad [1.3].$$

The simulated results presented in this chapter are based on an impedance match in a 50Ω system and design frequency of 500MHz.

For acceptable performance it is necessary that the divider exhibit a close impedance match at each port, a high degree of isolation between ports two and three, and little transmission loss from port one to port two and from port one to port three and vice versa in the power combining scenario [15,11]. The ideal equal-power split Wilkinson divider, with power input at port one splitting to ports two and three, will exhibit a power level of -3dB at both output ports with reference to the input power level. As will be demonstrated, the Wilkinson power divider endures significant performance degradation when composed with low-Q inductors. A series of five simulations using ideal components with varied Q on the inductor was carried out to determine the effect that the inductor's Q factor has on the Wilkinson's performance. Q values of infinity, thirty, twenty-five, ten and roughly four were chosen. The Q of infinity was chosen to demonstrate perfect Wilkinson power divider performance, whereas a Q of a little less than four was simulated because this value was the largest Q simulated of a spiral inductor in the C5 process within this work.

From Figure 1.2 it is clear that undesirable reflections are avoided with large Q. Increased reflection is a direct consequence of the parasitic series resistance incorporated in the inductor as its quality deviates from the ideal scenario (Q = Infinity).

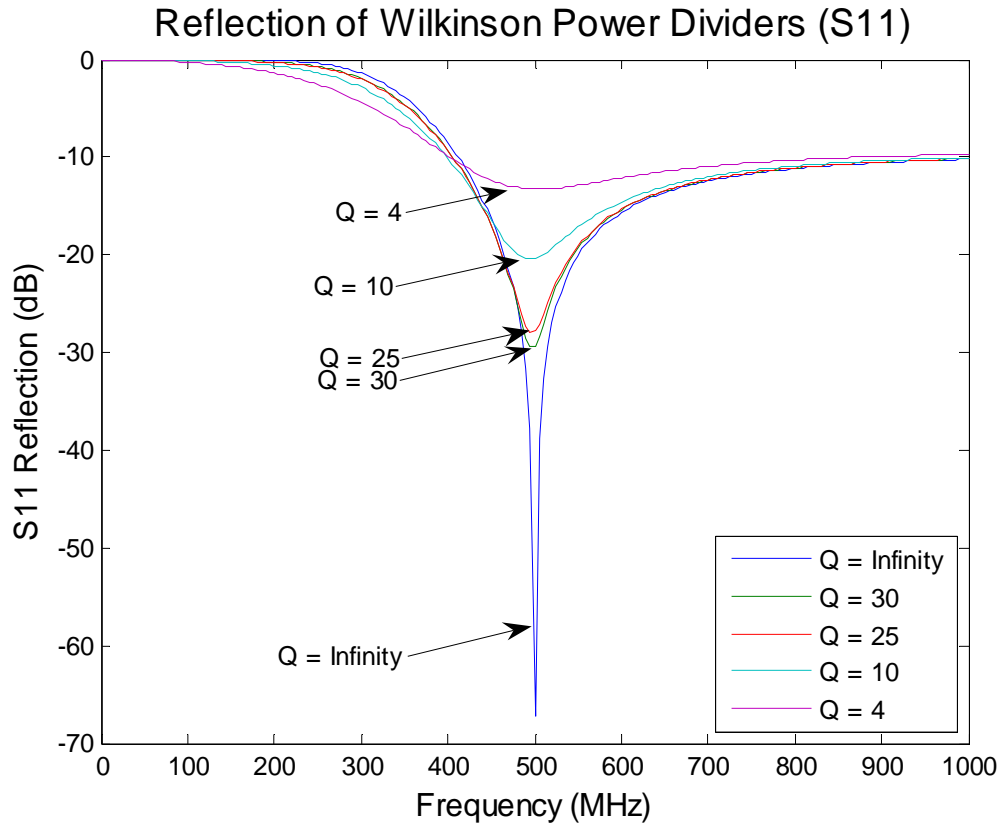


Figure 1.2: Reflection coefficient (S11) of the five Wilkinson power dividers simulated.

The series resistance, which is unavoidable in real inductors and is modeled in the power divider simulations, leads to a degraded impedance match. Theoretically, when Q equals infinity all reflections are completely suppressed at the design frequency. As seen in Figure 1.2, $Q=30$ outperforms the Wilkinson dividers employing the $Q=25$, $Q=10$ and $Q=3.71$ inductors as is expected with degraded quality in the components used.

In Figure 1.3 the 15dB return loss bandwidth is given in percentage form referenced to the design frequency. The 15dB level is a common impedance match metric and corresponds to approximately three percent reflection of power. From the figure it is clear that the Wilkinson designs employing $Q = 25$ or greater portray

sufficient suppression of reflection for most applications. Whereas, below a Q of 10, the Wilkinson divider's 15dB bandwidth drops dramatically.

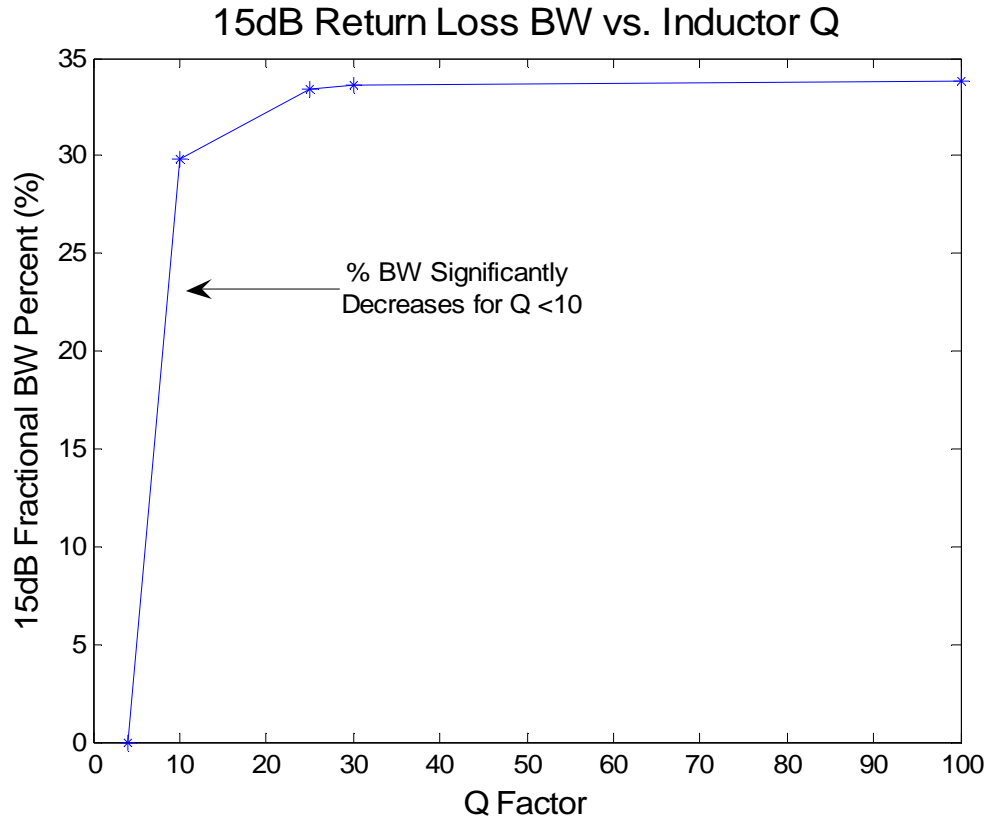


Figure 1.3: 15dB Reflection bandwidth versus the Q factor of the divider. While not shown in the figure, Q of infinity results in a 15dB BW of 33.8%.

The transmission coefficient (S_{21}) provides an idea of how much of the input power has actually traveled to the output. In this work, S_{21} is used as the significant figure of merit to determine the acceptable inductor Q for dividing applications. In the ideal case, the output demonstrates -3dB with respect to the input power level. This result is in accordance with simulated values.

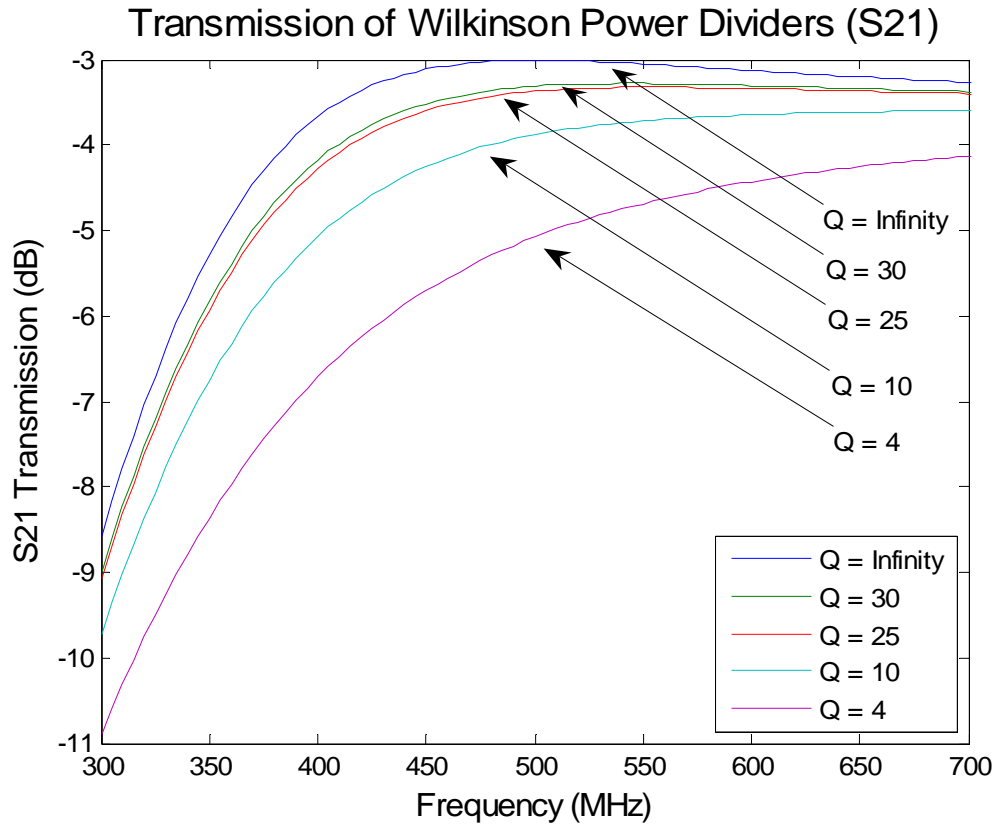


Figure 1.4: Transmission coefficient (S21) of the five Wilkinson power dividers simulated.

At the design frequency, the Wilkinson divider employing the inductor characterized by a Q of 30, has a transmission of -3.312dB, the divider exhibiting a Q of 25 delivered a transmission of -3.371dB, the divider with a Q of 10 delivered a transmission of -3.881dB while the Wilkinson hypothetically employing the spiral inductance exhibited a transmission of -5.077dB.

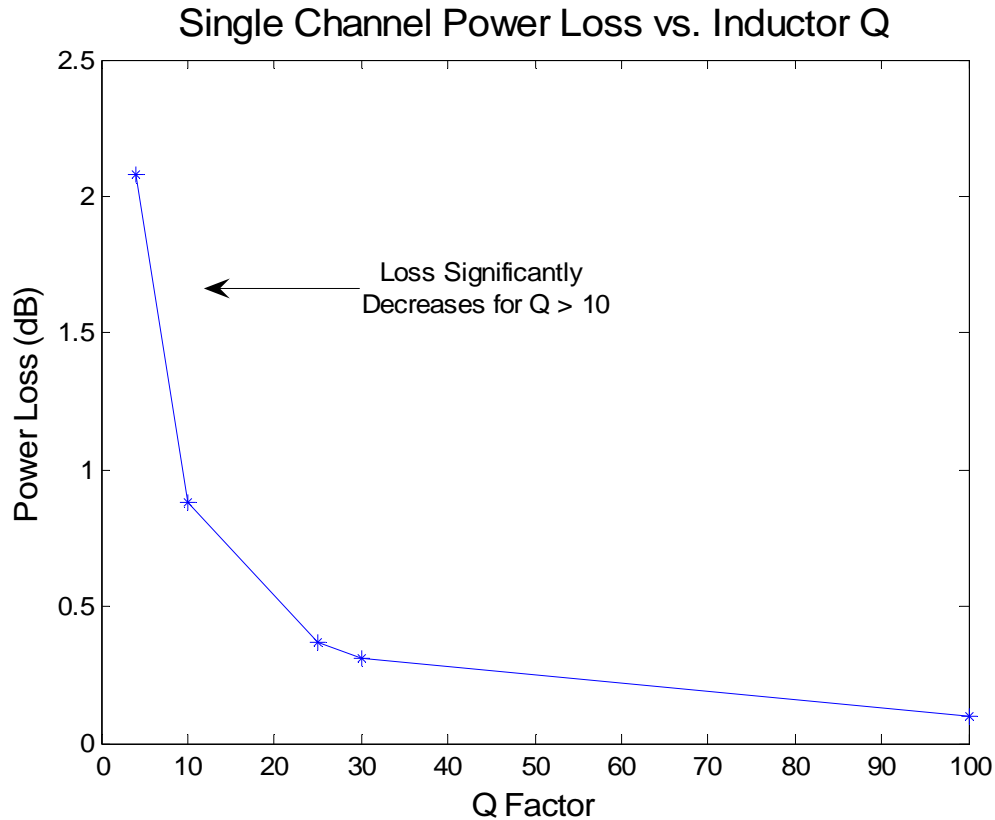


Figure 1.5: This figure relates the quantity of power loss experienced by one channel of a two-port divider to the divider’s corresponding Q value. Although not shown on this figure, the ideal situation where Q equals infinity demonstrates a power split with no loss.

Therefore, from Figure 1.5, it can be concluded that the transmission loss becomes severely degraded as Q continues to drop below 30. As in [1], a Q greater than 30 for Wilkinson power dividers, as a design goal, is therefore declared within this thesis.

The isolation between ports two and three describes how “separated” they are from one another by quantifying how much signal input into one of these ports diverts to the corresponding port. Unsurprisingly, as Q decreases so does the isolation between the output ports in the Wilkinson divider as plotted in Figure 1.6.

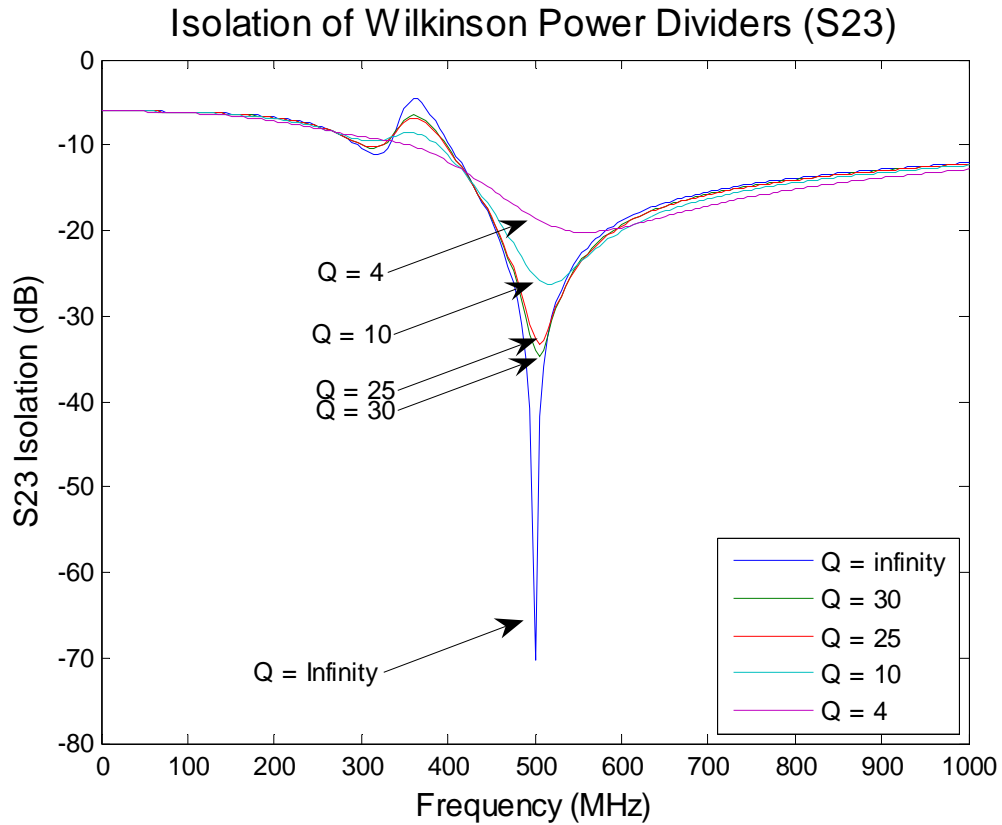


Figure 1.6: Isolation (S23) of the five Wilkinson power dividers simulated.

This section makes clear the necessity of employing high-Q inductors in lumped element Wilkinson power dividers. Primarily, without high-Q components, the transmission loss of the device is unacceptable. The reflection and isolation of the divider suffers as well with low Q inductors.

Colpitt's Oscillator

A Colpitt's oscillator is a common sinusoidal signal source. The most important property of an LC oscillator, besides guaranteeing oscillation, is that it include a high-Q tank. As discussed in [10], because an LC oscillator's signal-to-noise ratio is directly related to Q it is advantageous to maximize the Q of an oscillator's tank. In addition,

assuring a high-Q tank significantly reduces the spectral distortion in the output signal. In other words, the output signal is much more pure, exhibiting mostly the fundamental frequency. Another sequence of simulations is presented in this section that aim to uncover the effect the inductor Q has on the overall performance of a Colpitt's oscillator. Ideal components are used and adding in a series resistance varies the Q of the inductors. The circuit simulated is shown below in Figure 1.7 and is used to model the phenomena of an oscillator circuit employing a resonant LC tank.

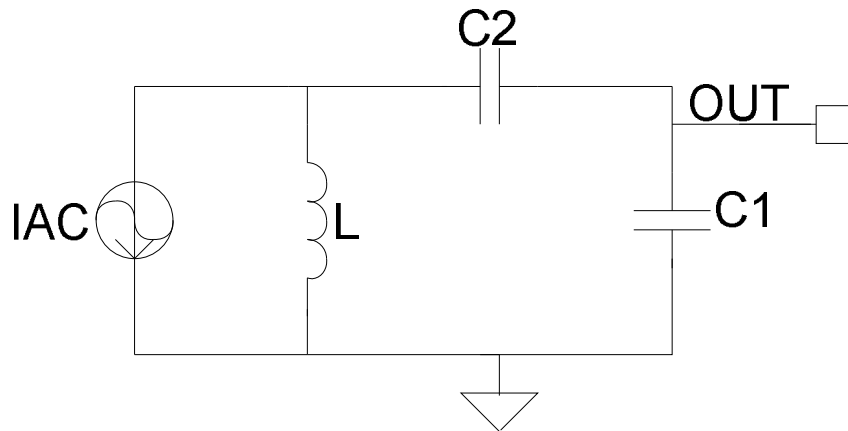


Figure 1.7: Ideal Colpitt's simulation setup.

The circuit simulated consists of a Colpitt's feedback topology with an excitation source in the form of an AC current source at the input [9, 10]. Similar to a transistor's function, the AC signal source supplies energy to the tank circuit that resonates at a design frequency of 500MHz in this case. A common analysis is to look at the output signal over frequency to determine the "tightness" of the frequency response. A tighter frequency response is desired because it implies that there is less variation of the oscillation frequency. The circuit in Figure 1.7 was simulated in an AC environment and the gain (V_{out}/I_{in}) was obtained and plotted.

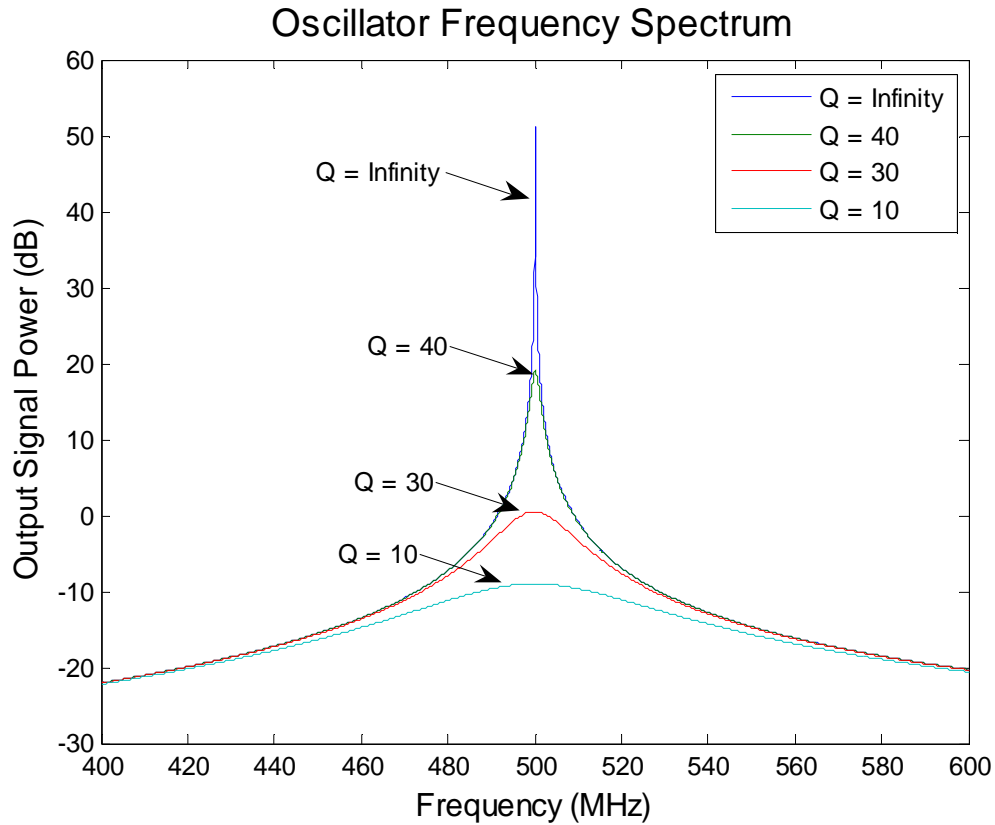


Figure 1.8: Oscillator output spectral density.

It is easily seen from Figure 1.8 that as the LC tank Q is increased the oscillator circuit performance becomes more optimal. Because Q is inversely related to the -3dB bandwidth of the output spectrum it is expected that this property of the oscillator becomes larger with decreasing Q as is the trend in Figure 1.8. Even from the point of view of creating sustainable oscillation, an inductor Q of 30 is hardly acceptable because the gain barely reaches 0dB, which is an essential criterion for the circuit to eventually oscillate. In fact, from the curve in Figure 1.8, a Q of 40 does not deviate much from the ideal case. The only noticeable difference is in peak magnitude.

Again, ensuring high quality factor inductors in the two RFIC circuits considered in this chapter has been shown to be very important in both circuit's operation,

performance, and ability to realize its intended function. However, even with a reputation for poor performance and large Silicon die occupation, passive spiral inductors have still found their way into industry and research-related RFIC applications. Much research funding and effort has been spent trying to realize high quality passive inductors to expand the capabilities of ICs and improve their overall performance. At the same time, different techniques employing gyrator-like configurations, have reported simulated results proposing a promising means of creating inductance actively. These devices, called active inductors (AIs), have been reported to exhibit inductor Q values exceeding 12,000 [3] in simulation while including inductance tuning and realizing a fraction of the Silicon area required for spiral inductors of similar inductance value.

Active Inductor (AI) Literature Review

A handful of papers [1-8], have been written on the topic of Active Inductors (AIs) in CMOS. The proposed topology, an extremely simple feedback loop consisting of two back-to-back transistors, that realizes an inductive input impedance over a range of frequency and is depicted in Figure 1.9. This configuration hypothetically overcomes the short comings of passive inductors or of lengthy transmission lines. In every scenario, the simple topology is enhanced by some method employing additional transistor circuitry. Both corrective and regulating techniques to enhance the AI's operation have been presented in [1-8]. Design techniques such as including cascode stages in both regulated and multi-regulated forms, double-feedback and cascode double-feedback have been simulated and documented. In addition, discussions involving manipulation of the zero and pole locations of the AI and methods to remove unwanted

resistive paths are presented. [1-3] also propose an equivalent circuit, after making simplifying assumptions that offer intuition on how to approach an AI design.

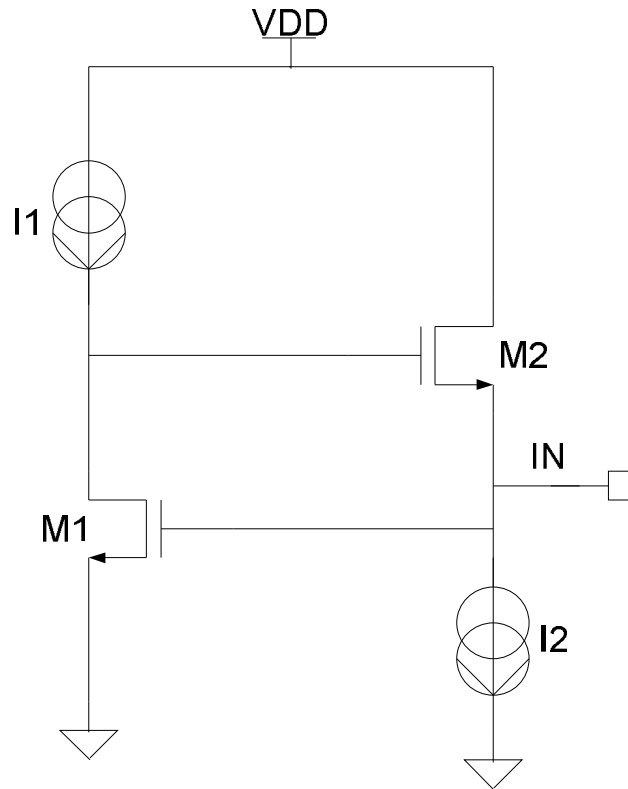


Figure 1.9: Active Inductor circuit topology.

The appeal of AIs, is the potential for a high quality factor inductive impedance generated from the improvement of an extremely simple semiconductor circuit. Promising simulated results are presented in [3]. The authors claim to have designed an AI exhibiting a Q factor of 12,000 in a $0.18\mu\text{m}$ CMOS process. Interestingly lacking in the literature is a discussion of the bias sensitivity of the AI and its process variation characteristics. Most of the literature involving CMOS AIs is simulation-based save for the work of the [1]. For example, in [1] a lumped element Wilkinson is demonstrated using an AI. The authors do not comment on the variability of the AI to bias and process

corners, but do employ an off-chip bias to tune the Wilkinson's operation frequency. In addition to the reduced size of the active inductor in [1] (150 μm by 100 μm) opposed to passive spiral inductors (typically on the order of 400 μm by 400 μm), the paper states "the fabricated circuit exhibits an insertion loss less than 0.16 dB and a return loss better than 30 dB at the center frequency while maintaining good isolation between the output ports." This thesis takes an in-depth look at AIs for implementation in a CMOS process with special attention paid to achieving high Q and maintaining stability over process corners.

Thesis Overview

Chapter two presents a thorough investigation of AIs beginning with the simple grounded active inductor (SGAI). In order to boost performance, a cascode transistor is included to form the topology known as the simple cascode active inductor (SCAI). Due to issues of stability, achievability and reliability of both L and Q values, it is determined that inductor tuning is necessary over process, temperature and voltage variations in order for the AIs to be practical in any RFIC design. A tuning scheme and validating simulation results are presented in Chapter three. Chapter four discusses the use of tuned AIs in applications such as Wilkinson dividing/combing circuits. Concluding remarks and suggestions for future work are commented upon in Chapter five. Included in Chapter five is a brief discussion of considerations for utilizing AIs in scaled processes.

CHAPTER TWO

FULLY INTEGRATED ACTIVE INDUCTORS

Introduction

The property of an electrical device to produce a voltage proportional to a time-varying current through the device is commonly known as inductance. Just as capacitors store electrical energy in the electric field present in the medium between its conducting surfaces, an inductor can store magnetic energy within the volume surrounding the inductor. Specifically, an inductance is defined as the measure of the ability of a device to store energy in the form of a magnetic field [13]. Inductors are classified as passive elements which absorb, or store energy and can only supply energy that has been stored. Inductors exhibit the characteristic of simultaneously resisting changes in a time-varying current [3] signal yet passing DC bias without significant attenuation. This versatility is an attractive property that can be used in such disparate applications as circuit biasing and resonant signal generation in oscillators.

There are several methods of realizing an inductor, the simplest being a coil of wire. In the context of integrated circuits (ICs), monolithic spiral inductors are an interesting topic of intense research focus. This focus has developed because of the extensive functionality and versatility a good on chip inductor would offer and also because of the difficult design challenge spiral inductors have presented. Generally, on chip spiral inductors over Silicon exhibit low quality factor (Q) and large dimensions while also introducing undesirable resistive loss. Dr. Thomas Lee states in [10], "From the point of view of RF circuits, the lack of a good inductor is by far the most

conspicuous shortcoming of standard IC processes.” As a result of this shortcoming, applications that call for high Q inductors are often implemented by going off chip for the necessary inductance. To reduce circuit size, minimize costs and avoid parasitic capacitance of including a pad it would be a tremendous advantage to stay on-chip if possible, thus the significant research activity in the development of high Q monolithic inductors. Interfacing to components off chip causes problems at microwave frequencies because of the resistance and inductance of the bond wire and is therefore undesirable.

This chapter investigates an under recognized, alternative method of realizing inductance using active devices. In the framework of this thesis, these so-called “Active Inductors” (AIs) are considered for use in both oscillators and power combining circuits within a $0.6\mu\text{m}$ CMOS process. To place the results of this research in the proper context such that meaningful conclusions can be drawn with respect to the value of AIs for these distinct applications, it is absolutely necessary that a discussion of key figures of merit, including self resonant frequency (SRF), quality factor (Q), power consumption, noise and chip size be considered accompanied with a separate discussion of existing passive CMOS inductors.

Key Figures of Merit

There are several figures of merit that are used to describe the performance of inductors including SRF and Q. When discussing AIs, issues of noise and power consumption are critical parameters to consider as well. These and the issue of chip size are discussed below for the passive spiral inductors and AIs, both implemented in CMOS. It is interesting to note that depending on the application of a given component,

the definition of a given figure of merit may vary. An example of a parameter whose definition is application-dependent is quality factor as will be discussed in the quality factor section.

Self Resonant Frequency (SRF)

Many frequency-dependent circuits contain the significant, distinguishing parameter SRF. Generally, SRF is the frequency at which the imaginary part of a complex impedance is canceled, or becomes zero, and as a result the total impedance appears purely real. As will be demonstrated, the phenomenon of the imaginary part of impedance becoming zero corresponds directly to a switch in an inductor's behavior between inductive and capacitive at the resonant frequency. Circuits exhibiting a resonant behavior can be used as tanks in the framework of an oscillator. In the general application of inductors, the SRF provides a measure of the frequency up to which the device can be used as an inductor. Beyond the SRF, the inductor's reactance is capacitive thus making the element unusable if inductance is necessary. Since the impedance of an inductor changes dramatically near resonance, in practice when using an inductor in the conventional sense, the frequency limit of operation is well below the SRF. A somewhat unconventional use of an inductor is in relatively narrowband RF choking applications in which the inductor is used around its SRF.

Quality Factor (Q)

Another quantitative and qualitative descriptive parameter extensively used in frequency dependent circuits is quality factor, typically denoted as Q . Due to the existence of several defining expressions, the notion of a Q can be confusing and lead to

misinterpretation of circuit performance in some cases. The underlying Q definition for sinusoidal excitation, from which all other definitions can be derived is:

$$Q \equiv \omega \cdot \frac{\text{energy stored}}{\text{average power dissipated}} \quad [2.1].$$

This versatile equation applies to both resonant and non-resonant circuits and offers no discrimination on how energy must be stored or how power must be dissipated. While a given definition of Q may be valid in specific situations or around a certain frequency, the fundamental implication of Q always applies. Thus, in each situation discussed below, the usage of Q will be explicitly defined.

In the topic of inductors, the Q is derived to be:

$$Q = \left| \frac{\text{Im}[Z]}{\text{Re}[Z]} \right| \quad [2.2].$$

This equation shows that the ratio is a comparison of the amount of imaginary impedance to resistive impedance; it is a measure of how close the inductor is to the lossless ideal.

In situations where the inductor is used at its resonant frequency, the convenient Q definition is directly related to the SRF and inversely related to the fractional bandwidth of the magnitude of the impedance. It can be shown that there is an approximate symmetry, about the SRF, characteristic of the magnitude of impedance of a RLC circuit; therefore, the shape below SRF is the same shape as above the SRF and a -3dB BW can be determined and associated directly to Q [10]. Therefore when an inductor or tank is used at its SRF, Q is defined as:

$$Q = \frac{\omega_0}{BW} \quad [2.3]$$

where ω_0 is the SRF and BW is the -3dB BW of the magnitude of the impedance. In the context of resonator circuits, Q is a measure of the rate of energy loss; therefore, a higher Q implies more persistent ringing in a resonant circuit [10]. Also, for a given resonant frequency, higher Q implies a narrower impedance BW.

Power Considerations

In addition to the connection between power dissipation (loss) and its impact on the value of Q for either a passive inductor or an AI, AIs, as active circuits, require DC biasing. Thus in developing AIs, the designer must maintain power consumption within an acceptable limit determined by each specific application. The DC power P_{DC} supplied to a circuit is defined as $\sum_{i=1}^n V_i I_i$ where V_i is the power supply voltage, I_i is the associated biasing current and n is the number of reference currents. In this work power will be referenced in Watts and a supply voltage of 5V will be assumed unless otherwise specified.

Noise Performance

Noise always limits the minimum signal level that is detectable and has unfavorable effects on the performance of ICs. Inherently, CMOS transistors generate noise voltages. The dominate contributors are thermal noise in the transistor's channel and flicker noise which is a consequence of dangling bonds in Si-SiO₂ semiconductor interfaces. Generally, minimizing noise is desirable and would have to be addressed depending on the specific application. Although, AI noise generation is generally not

commented upon in the literature it is possible that, based completely on noise, the range of AI applications may be limited by this FOM.

Chip Size

The trend of constant chip area reduction and small feature realization is one of the fundamental reasons to explore the capability of AIs. Staying on chip and reducing chip size is always desirable but comes with inherent limitations. Chip size realization and comparisons are commented upon in pertinent sections.

Linearity and Distortion

When implementing active devices, which follow the square law relationship between gate-to-source voltage and drain current, linearity and distortion are always of concern. The imperfection of transistor nonlinearity stems from variation in a transistor's small signal gain relative to the DC input level. Changes in a transistor's transconductance are not favorable for realizing constant active inductance.

Active Inductor Topologies and Theory of Operation

Basic AI Topology

This section presents the fundamental topology used to generate inductance with active devices. Derived transfer functions are compared to other works, simulated results are presented and conclusions are drawn about this simple device.

Fundamental Concept. The underlying concept of the AI is to exploit the parasitic capacitance of the transistors in order to implement the required poles and zeros that

force the overall circuit to behave inductive. As stated in [2], this approach allows the operation of such devices close to frequency of the transistor's unity short-circuit current gain (f_T). This is a desirable quality because it implies that high frequencies can be achieved and suggests that the AI technique of generating inductance will scale with shorter channel lengths. To realize inductance a zero must dominate the impedance transfer function (ZTF) at the frequency of interest. However, a transistor inherently exhibits high-frequency poles that impose limitations on the operation of such devices. Therefore, the key strategy for increasing the frequency band that AIs are inductive is to decrease the frequency of the dominating zero and to push the parasitic pole locations as high as possible.

Active Inductors are generally implemented from a gyrator-type configuration where two transistors are connected in a back-to-back fashion [3] as shown below in Figure 2.1. In this work, the configuration shown below is referred to specifically as the simple grounded AI (SGAI) and this distinction will be made when it is important to make a discrimination. Otherwise, this device may be referred to simply as an AI.

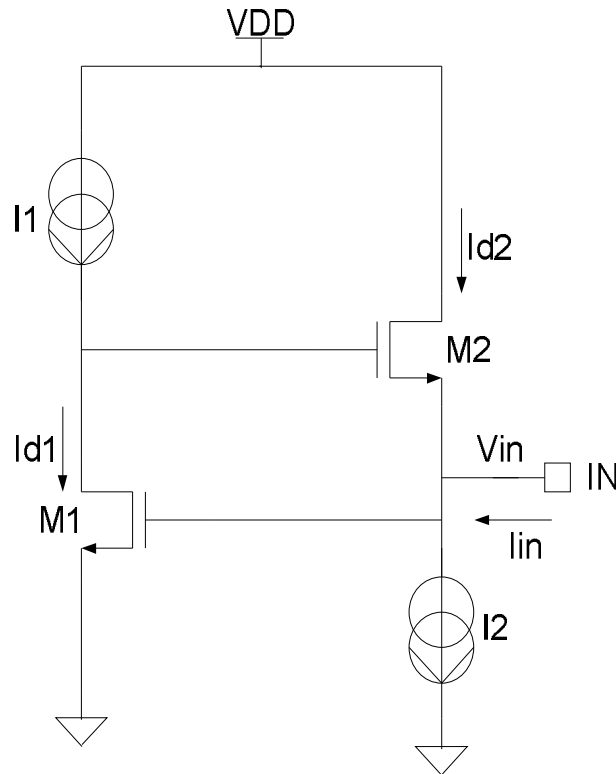


Figure 2.1: Simple grounded Active Inductor (SGAI) circuit schematic.

In order to facilitate the following explanation of the SGAI's operation, each transistor's gate-to-source capacitance C_{gs} has been included in Figure 2.2. As explained in [3], transistor M1 is used to convert the input voltage, v_{in} , into a current for charging the dominant integrating capacitor C_{gs2} . M2 translates v_{gs2} , the voltage across C_{gs2} , to force a specific input current i_{in} in order for I2 to remain constant. Notice that this configuration employs and relies on negative feedback to guide its inductive behavior and stability. From a steady state condition, an increase in i_{in} supplies additional charge at the gate of M1 because at this point $I_{d2} = I2$. Consequently v_{in} , or v_{gs1} , is increased by an amount proportional to this additional input current. An increase in v_{gs1} augments the drain current of M1, i_{d1} . Because I1 is also a constant current source, charge from C_{gs2}

(the gate of M2) must be extracted in order to sum with I_1 and supply the increased current M1 demands.

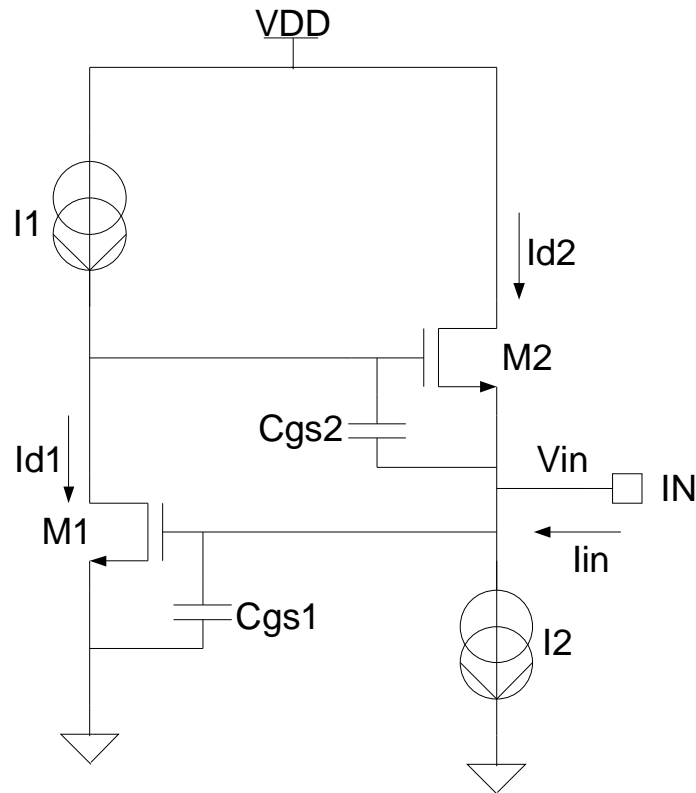


Figure 2.2: An alternative circuit schematic of the simple grounded AI illustrating the parasitic capacitances that help explain the operation of an AI.

Due to the removal of charge from the gate of M2, it is obvious that the gate voltage of M2 will reduce. Furthermore, with the original condition that v_{in} increased, the source voltage of M2 has additionally increased. Hence, an overall decrease in v_{gs2} has occurred and I_{d2} , the current sourced into the input node from M2, decreases. Because the current entering and leaving the input node must be equal and because I_{d2} is reduced, the current must be supplied by either the input branch or the gate of M1. Because the gate of M1 has a limited supply of charge the current is now sourced from

the input node in order for I_2 to remain constant. In essence the circuit has effectively shifted its operation in a collaborative manner to keep the input current entering at the same rate. In other words the SGAI has resisted changes in i_{in} . Alternatively, if i_{in} becomes negative, in the context of the polarity shown in Figure 2.2, ultimately M2 will supply this additional current out of the input. This is easily explained in a similar fashion. A negative i_{in} lowers v_{in} and the current in M1. I1 has nowhere to go so subsequently charge is spread onto the gate of M2 and onto C_{gs2} increasing v_{gs2} and enabling M2 to supply the extra i_{in} current. This characteristic of the circuit using feedback to resist changes in input currents is exactly what an inductor naturally works to do.

It is a goal of the following sections to compare my findings in several different frameworks. First, a simple small signal replica of the AI is developed and an impedance transfer function is derived. Due to the complicated nature of the expression the TF is left un-factored. The derived TF is then compared to the work of A. Thanachayanont and A. Payne in *VHF CMOS integrated active inductor* or [2], my ideal small signal model and also with the AMIS 0.6 μ m process model. Finally, several conclusions are drawn, methods are proposed to realize certain Ls, Qs and SRFs and the common trends of the relationships among the figures of merit are presented.

Derivation of the Impedance Transfer

Function of the Simple Grounded Active Inductor (SGAI). The impedance transfer function (ZTF) was derived for the SGAI using the simple Kirchhoff circuit laws. Each transistor was modeled with a transconductance (g_m), a drain to source output impedance (r_0), parasitic capacitances C_{gs} and C_{gd} and a body effect transconductance

(g_{mb}). Since the body and source of transistor M1 are tied together, see Figure 2.1 for example, M1 is not influenced by the body effect. The body effect was found to add resistance in parallel to r_{o2} thereby lowering the total output resistance of transistor M2.

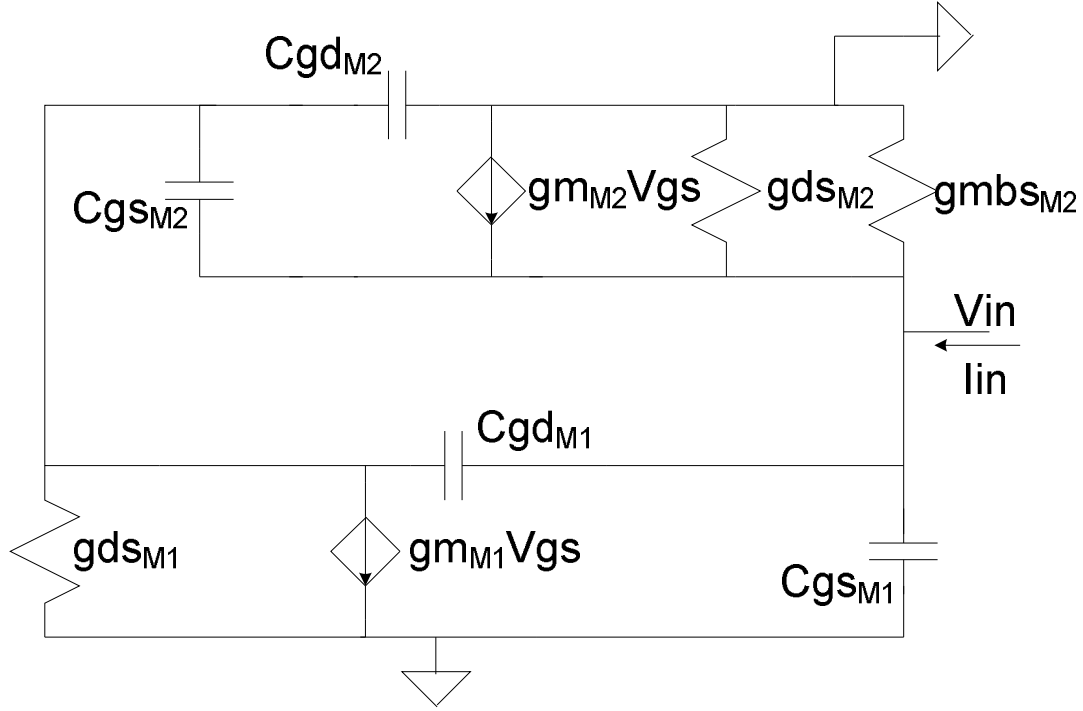


Figure 2.3: Small signal model used to represent the SGAI. This small signal model assumes infinite impedance of both AI current sources.

The impedance transfer function of the SGAI was found to be:

$$Z_{in} = \frac{1}{\left[\frac{s(C_{gs2} + C_{gd1}) - g_{m1}}{s(C_{gs2} + C_{gd2} + C_{gd1}) + g_{ds1}} (s(C_{gs2} + C_{gd1}) + g_{m2}) - s(C_{gs2} + C_{gs1} + C_{gd1}) - g_{m2} - \frac{1}{R_{BODY}} \right]} \quad [2.4]$$

where R_{BODY} is the equivalent parallel resistance of M2's output resistance ($1/g_{dsM2}$) and the resistance that is present between the source and body of M2 ($1/g_{mbsM2}$) and g_{ds1} is the output conductance of M1. Notice that when the terms are multiplied through, the numerator of Z_{in} becomes dependent on g_{ds1} , C_{gs2} , C_{gd2} and C_{gd1} .

In fact, the zero is located at:

$$\frac{g_{ds1}}{(C_{gd1} + C_{gd2} + C_{gs2})} \quad [2.5].$$

Due to the complexity of the 2nd order denominator of the above polynomial, expressions for the pole locations are not presented here. Henceforth, the input impedance expression of 2.4 will be abbreviated LYSON ZTF. The SGAI has been considered by others including Thanachayanont and Payne [2]. In their work, a similar impedance transfer function given. Their expression, which will be abbreviated as VHF ZTF is given below in equation 2.6:

$$\text{VHF ZTF} \equiv \frac{g_{ds1} + s(C_{gs2} + C_{gd1} + C_{gd2})}{(g_{ds1} + g_{m1} + sC_{gd2})(g_{m2} + s(C_{gs2} + C_{gd1}))} \quad [2.6].$$

Clearly, the zero is located the same position as that of the LYSON ZTF. The authors of this paper suggest that the dominant pole occurs at:

$$\omega_p = \frac{g_{m2}}{C_{gs2}}.$$

However, the VHF ZTF fails to include C_{gs1} , g_{ds2} and g_{mb2} . C_{gs1} acts as a shunting capacitor to ground and greatly affects the operation of the inductor. Neglecting g_{ds2} and g_{mb2} omits the parallel resistance that is present between the input and ground. As is demonstrated in the following section, while neglecting C_{gs1} , g_{ds2} and g_{mb2} results in an expression that accurately predicts both the real and imaginary impedance of the SGAI at frequencies well below the AIs SRF, this simplified expression provides a rather poor representation of the actual impedance seen at high frequencies. However, a key

attraction of AIs claimed by the authors of [2] was that they can be used near the high frequency process f_T .

Verification and Comparison

of the Impedance Transfer Functions.

In an effort to both verify the derived expression for the input impedance of the SGAI (LYSON ZTF) and to compare it with a similar expression found in the literature (VHF ZTF), the two expressions were plotted versus frequency, along with the input impedance of the circuit of Figure 2.3 using a commercially available circuit simulator. In simulating the circuit of Figure 2.3, the resistive portion of the input impedance of each transistor was set to infinity and reasonable values for the parasitic capacitance, transconductances and output resistances were used.

As illustrated in Figure 2.4, LYSON ZTF matches the small signal model perfectly in terms of the input resistance. This is to be expected, as LYSON ZTF was derived directly from the small signal model of Figure 2.3. By neglecting C_{gs1} , g_{ds2} and g_{mb2} , VHF ZTF ignores losses associated with the parallel resistance and high frequency shorting capacitors. These assumptions cause a significant difference of prediction versus actual behavior especially at high frequency. The higher resistance realized in the VHF TF is explainable due to the absence of both the parallel resistance of M2 and the parallel capacitance (C_{gs1}) that shorts out the resistance seen at high frequency. Both these effects are approximately inversely related to the real part of the impedance at high frequency. In Figure 2.5, the imaginary part of the impedance is plotted in a similar fashion.

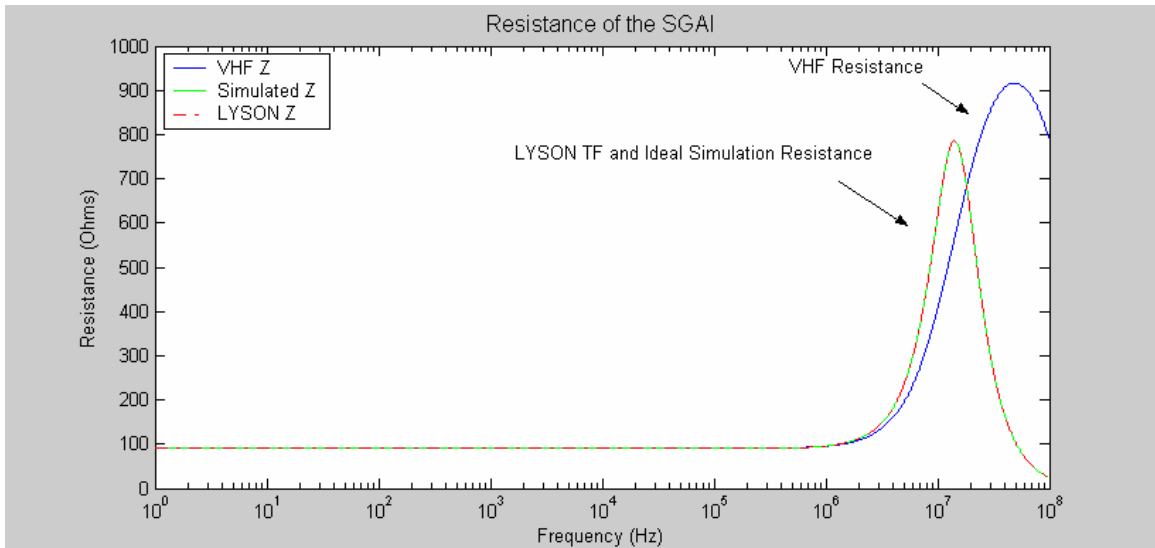


Figure 2.4: Plot for comparison of AI real input impedance vs. frequency for the VHF and LYSON transfer functions and the ideal small signal model simulation results.

Again the LYSON ZTF and simulation curves illustrate a precise match, whereas the VHF prediction deviates from the actual model predicting both a higher reactance and a larger SRF. Once more the greater magnitude of reactance can be explained due to the absence of the parallel resistance and capacitance which would work to lower the reactance with nearly an inverse relationship especially at high frequency. Because the SRF is defined to be $\frac{1}{2\pi\sqrt{LC}}$ the included capacitance of C_{gs1} in the LYSON TF lowers the SRF in comparison to the SRF of the VHF TF. To make a more definitive case for the accuracy of LYSON ZTF, both it and VHF ZTF are compared with transistor-level simulations corresponding to the BSIM3 model of the AMIS C5 (0.6 μ m) process.

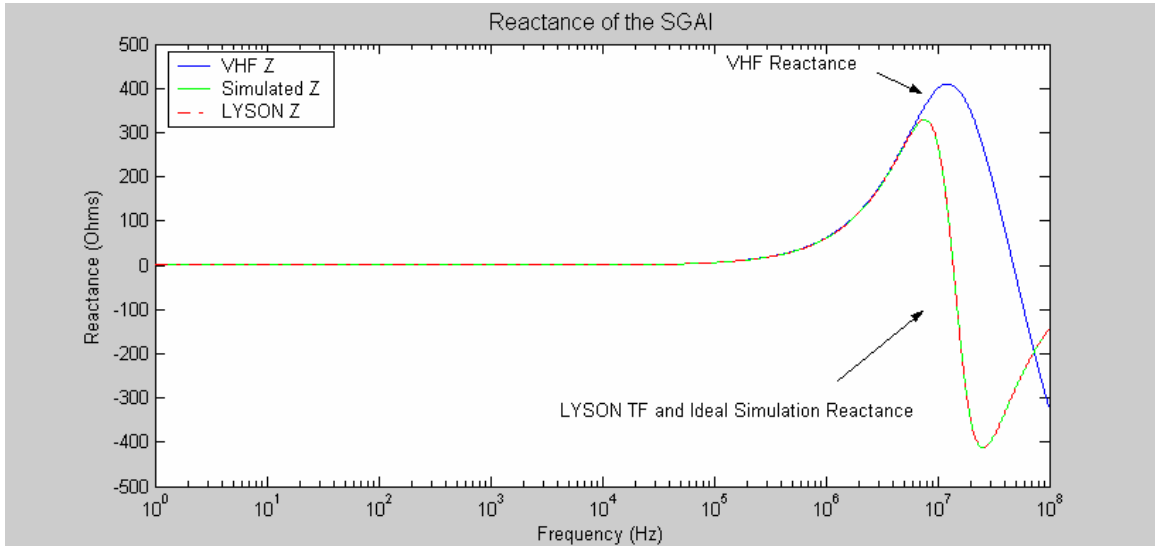


Figure 2.5: Plot of AI imaginary input impedance vs. frequency for the VHF and LYSON transfer functions and the ideal small signal model simulation results.

Comparison of Impedance Transfer

Functions with the AMIS C5 Process. At this point a comparison of the SGAI

using a BSIM3 model of the AMIS 0.6 μ m process with LYSON ZTF and VHF ZTF is presented. For a meaningful comparison it was necessary to run a device operating point simulation of the transistor-level circuit, repeated in Figure 2.6, in order to match the g_m , g_{ds} , and g_{mb} circuit parameters used in the TF representations of the input impedance. The parasitic capacitances, C_{gs} and C_{gd} , were calculated under the assumption that both transistors operate in saturation with strong inversion using the following first order equations:

$$C_{gs} = \frac{2}{3} WLC_{ox} + WC_{ov} \quad [2.7]$$

$$C_{gd} = WC_{ov} \quad [2.8].$$

C_{ox} , the oxide capacitance between the gate and channel per unit area, and C_{ov} , the overlap capacitance per unit width, were both obtained from the C5 BSIM3 simulation

model. The topology chosen for this comparison was a SGAI realizing 7 nH of low frequency inductance and an SRF of 4.32 GHz [SGAI_CH2 schematic]. The corresponding values of the LEVEL 1 SPICE parameters relevant to the two impedance transfer functions are given in Table 2.1. Figure 2.7 provides a plot of the input resistance of the SGAI versus frequency for the two ZTFs as well as the AMIS C5 simulation.

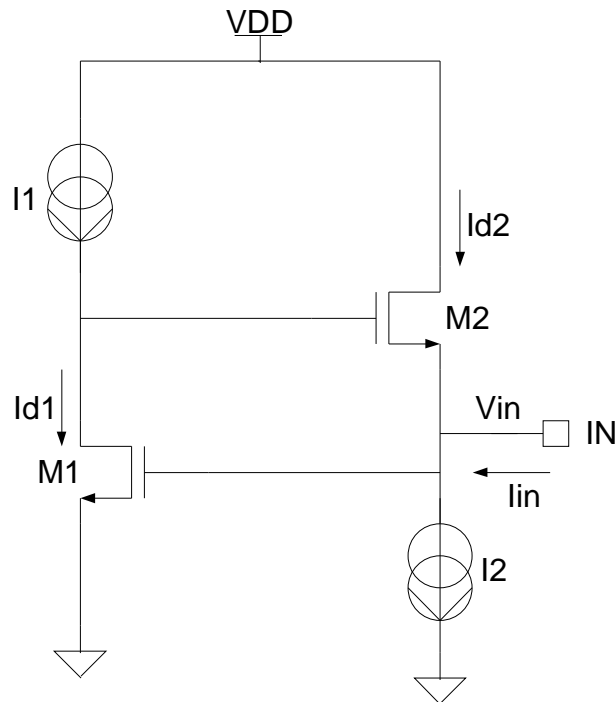


Figure 2.6: SGAI circuit simulated.

Parameter	M1	M2
gm (mA/V)	2.75	6.13
gds (uA/V)	20.452	172.73
gmb (mA/V)	0	0.767
Cgs (fF)	60.61	60.61
Cgd (fF)	10.75	10.75

Table 2.1: Parameters simulated.

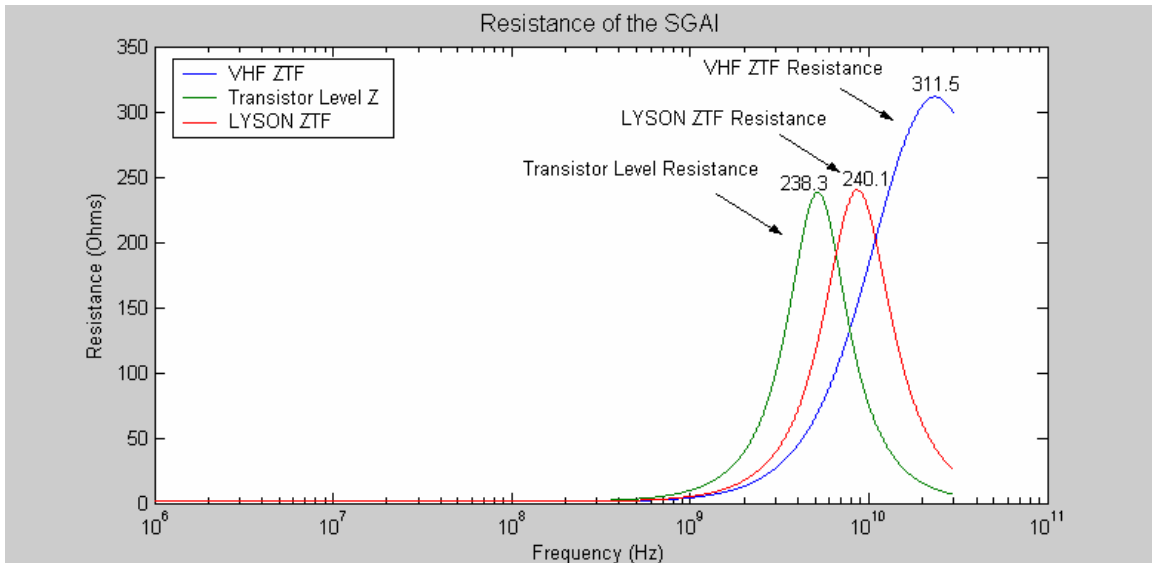


Figure 2.7: The resistance of the SGAI demonstrating the differences between the transistor simulation and the different approximating transfer functions.

Because a first order approximation, in the form of a small signal model, will not exactly represent the behavior of a BSIM3 model of a transistor, both transfer functions deviate from the transistor level simulation. However, the LYSON ZTF does predict the maximum resistance to a close approximation with the transistor simulation whereas the VHF approximation is still rapidly increasing at 10 GHz. Acknowledging that the peak of the resistance curves corresponds to the SRF frequency implies that both the LYSON and VHF ZTFs over estimate the performance of the SGAI. The transistor-level simulation portrays the SRF at 5.17 GHz, the LYSON ZTF estimates the SRF at 8.69 GHz and the VHF ZTF estimates the SRF at 23.7 GHz. Specifically, LYSON ZTF overestimates the SRF by 68% and VHF ZTF overestimates the SRF by 358%. These results suggest that the effective inductance and/or capacitance seen at the input is actually larger than predicted by either ZTF model. Additionally, the VHF ZTF over predicts the peak resistance by 30.7%, whereas the LYSON ZTF over predicts by 0.8%.

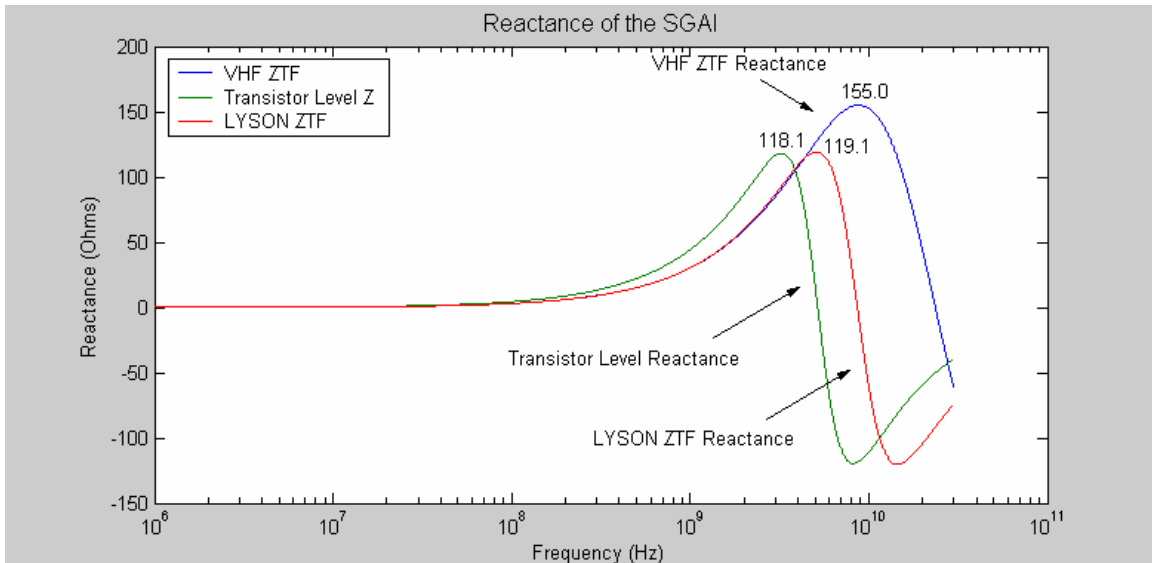


Figure 2.8: The reactance of the SGAI demonstrating the differences between the transistor simulation and the different approximating transfer functions.

The plot of the SGAI reactance vs. frequency (see Figure 2.8) is consistent with the results obtained for the real part of the input impedance. Again the two ZTFs plotted predict larger SRFs than the actual transistor circuit. The LYSON ZTF over predicts the peak magnitude by 0.8% and the VHF estimates a peak 31.2% above the transistor-level simulation. These results again suggest that the effective inductance and/or capacitance are larger in the transistor model.

Effect of Adding Current Mirrors (CMs) to AIs. There is no doubt that if AIs are found to exhibit sufficient performance for commercial applications, they must be supplied by on chip current mirroring devices. Adding active current mirror (CM) devices for the purpose of circuit biasing was investigated for the intention of determining the extent of performance degradation. Adding CMs, in the fashion shown in Figure 2.9, reduces the resistance from input to ground, degrading the inductor's ability to purely oppose high frequency signals. These resistances allow current to leak

from the input to ground instead of to the gate of M1 and reduce v_{gs1} . For this application it is required that v_{gs1} increase for inductive behavior. It must be emphasized that for high Q this parallel resistance is desired to be infinite.

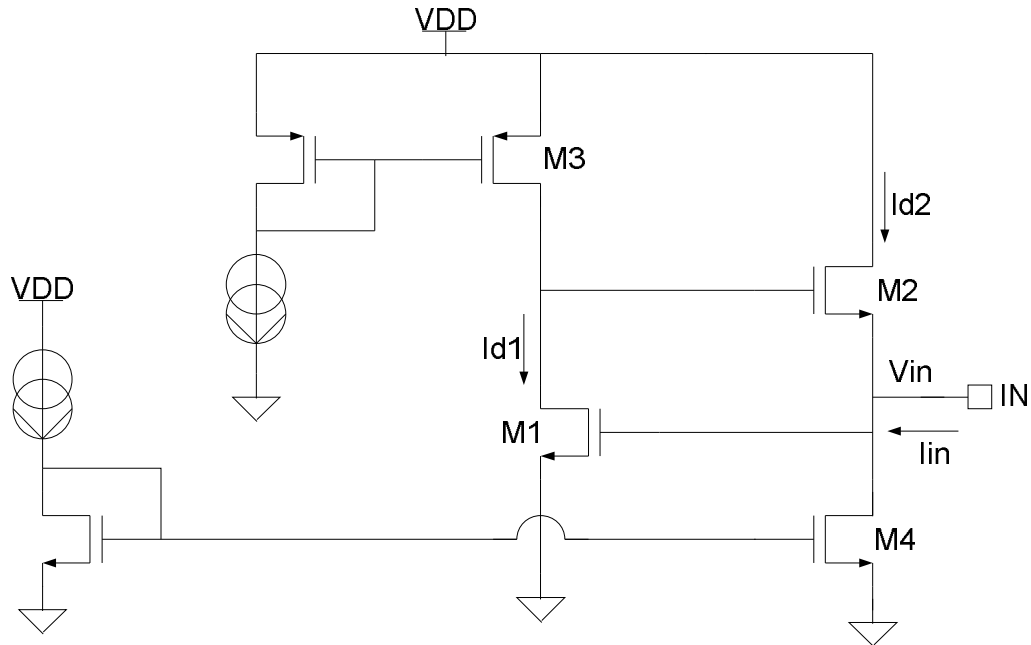


Figure 2.9: SGAI with current mirror devices.

Additionally, the gain and output impedance of the input transistor M1 is now reduced due to the non-ideal impedance added by the CM supplying I_1 . Recall, that it was previously presented that the location of the zero was at:

$$\omega_z = \frac{g_{ds1}}{(C_{gd1} + C_{gd2} + C_{gs2})}$$

Therefore it is expected that the CM will add conductance to g_{ds1} and will move the zero location to a higher frequency. This unfortunate consequence reduces the inductive range of the AI. To get a feeling for what effect adding CMs has on the inductive performance, the real and imaginary parts of impedance were plotted for the separate situations of incorporating ideal current sources and incorporating CMs at the transistor level.

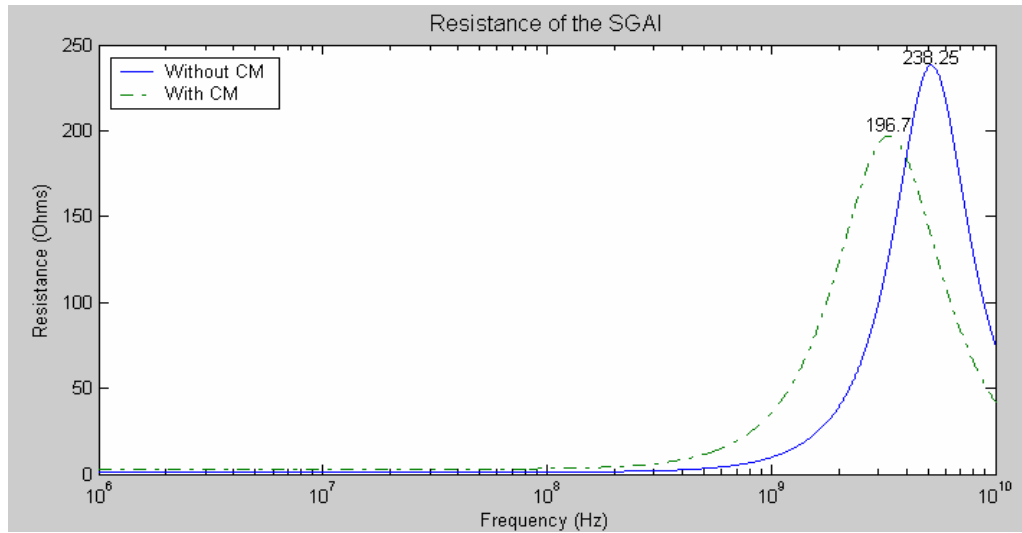


Figure 2.10: Resistance of the SGAI with and without CMs based on BSIM3 transistor-level simulation.

Indeed the added resistance at the input due to transistor M4's output resistance did lower the circuit's overall resistance from a maximum of 238.25 Ω to a maximum of 196.7 Ω . If additional resistance were desired at the input the output resistance of M4 is adjustable by increasing channel length, decreasing bias current or employing a cascode stage.

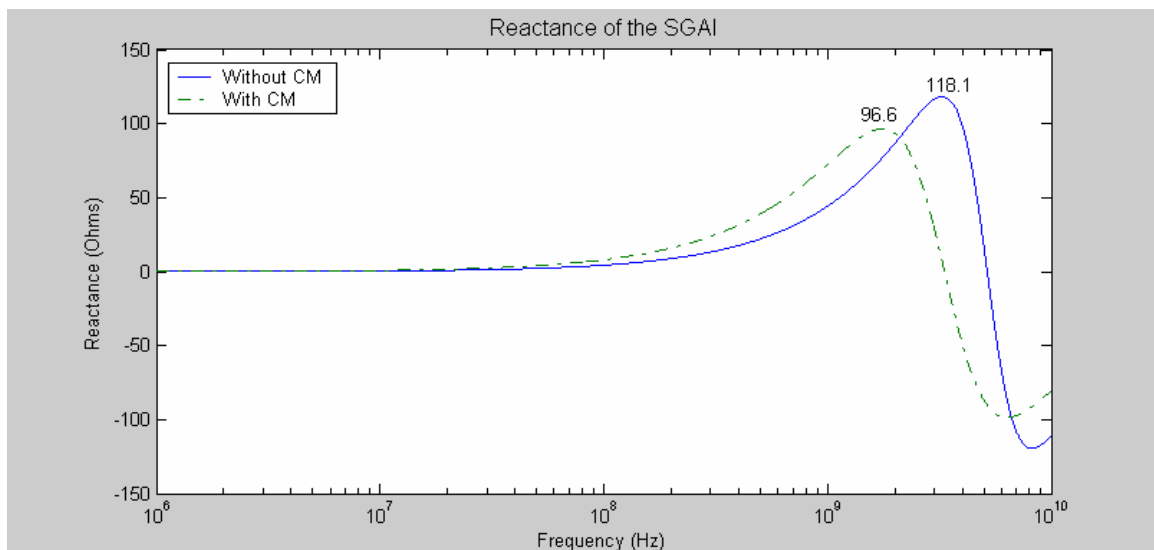


Figure 2.11: Reactance of the SGAI with and without CMs based on BSIM3 transistor-level simulation.

One reason that the SRF may be lowered is due to the added capacitance of M4's drain to bulk and drain to source parasitic. These capacitances are directly in parallel with C_{gs1} and add to the parallel shunting capacitance at the input. This added capacitance also reduces the maximum magnitude of the reactance from 118.1Ω to 96.6Ω .

Quality Factor of the SGAI. It is also informative to discuss the Q factor predicted by each of the transfer functions and simulations. In Figure 2.12, the quality factors from two ZTFs and the transistor simulations with and without CMs are all compared.

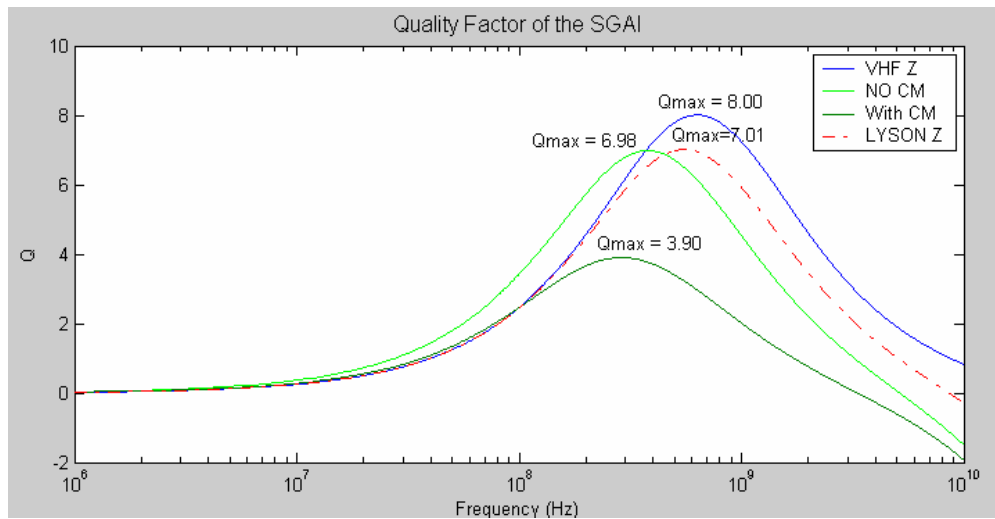


Figure 2.12: Q factor of the VHF ZTF, transistor level simulation, transistor level simulation with current mirrors and LYSON ZTF.

The above plot demonstrates the degrading result of adding the non-idealities of CMs to the model. The added parallel resistance of the CM has the effect of reducing Q by 44%. The plot also provides insight on how the two simulated curves compare to those predicted by the VHF and LYSON ZTFs. It is observed that the peaks of the Q curves

are skewed higher in frequency for the VHF and LYSON ZTFs. This result makes sense from the previous results in Figures 2.7 and 2.8 and recalling that Q is a ratio of the imaginary and real parts of the impedance. Because the LYSON and VHF ZTFs predict higher SRFs, the peaking behavior of the impedance occurs at higher frequency and therefore so does the Q_{max} . The LYSON ZTF results in a close approximation to the value of Q_{max} of the SGAI without CM.

Conclusions and Design

Methods of Realizing a Given L , Q or SRF. From the above discussion it seems clear that the derived ZTF (LYSON ZTF), while more accurate than a similar equation found in the literature, is likely of minor importance when designing a functional AI. This can be appreciated from the demonstrated importance that the CMs have on an AI. Therefore, the design of AIs, like most ICs, is an iterative process. The key is to begin with reasonable choices for each transistor's widths, lengths and bias currents. $W=100\mu\text{m}$, $L=0.6\mu\text{m}$ and $I_{bias} = 1\text{mA}$ tended to be a nice starting point for the SGAI. These circuit parameters design approximately a 7nH inductance with a Q_{max} of 5 at 400MHz and a SRF of 3.75GHz . To reduce the undesired effect of transistor mismatch the two transistors are sized the same. Reducing the widths and reducing the bias current have the effect of reducing the parasitic capacitances and the g_m of both transistors. The combined effect is a reduction in the SGAI's inductance. For a given L the effect of increasing the I_2 bias was to increase Q over all frequencies. An increase of I_1 tends to lower L and Q but increase the SGAI's SRF. Increasing the widths of the transistors in an equal fashion increases the inductance and Q yet lowers the SRF. As is typical there are tradeoffs between the performance metrics.

Relationships Between L, Q and SRF. As described previously, enhancing the performance of one parameter tends to lower the performance of a different parameter. Three inductors, with ideal current generation, were realized in a similar fashion in order to develop and discuss the relationship that exists between the figures of merit. These three SGAs were designed to serve the function of portraying the overall tradeoffs inherent in the design process. None of the AIs were tuned to show a better performance in any given area and are average in their overall functioning. All the supporting figures are plotted versus the inductance realized.

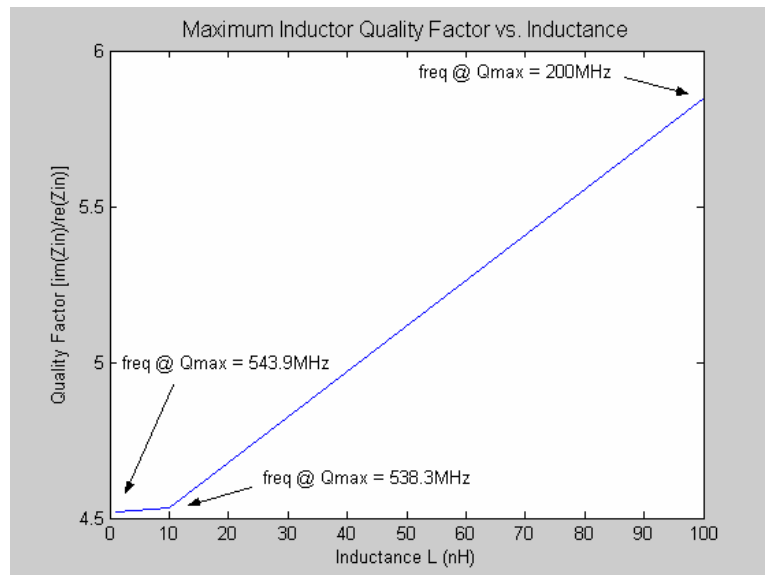


Figure 2.13: Maximum Q factor versus inductance realized.

From Figure 2.13, it is apparent that the achievable maximum Q factor increases as the inductance increases. This makes sense from the Q definition for inductors:

$$Q = \frac{\text{Im}[Z]}{\text{Re}[Z]}$$

Because the Im[Z] is larger it seems reasonable that the Q factor can be realized larger, since the Re[Z] for the AI doesn't scale directly with Im[Z].

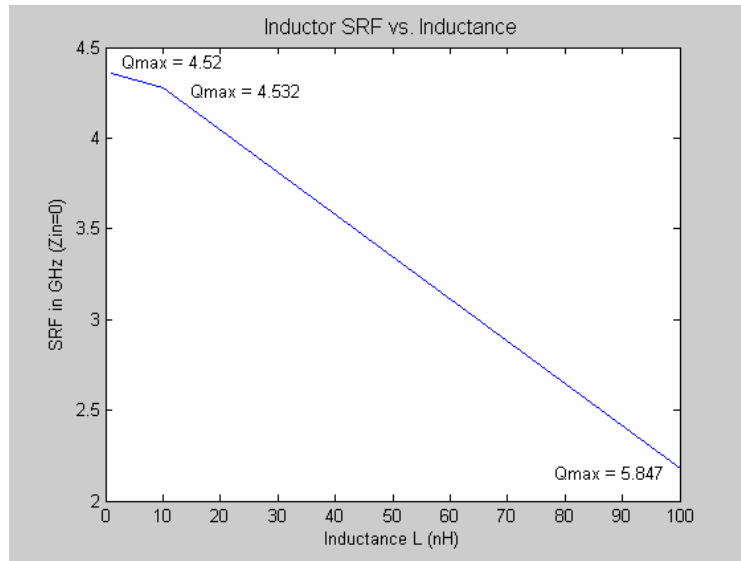


Figure 2.14: SRF versus inductance realized.

From the Inductor SRF vs. Inductance plot, it appears that although Q_{max} gets larger with larger inductances, the SRF of the SGAs decreases with increasing inductance.

This also makes sense due to the inverse relationship of SRF and L .

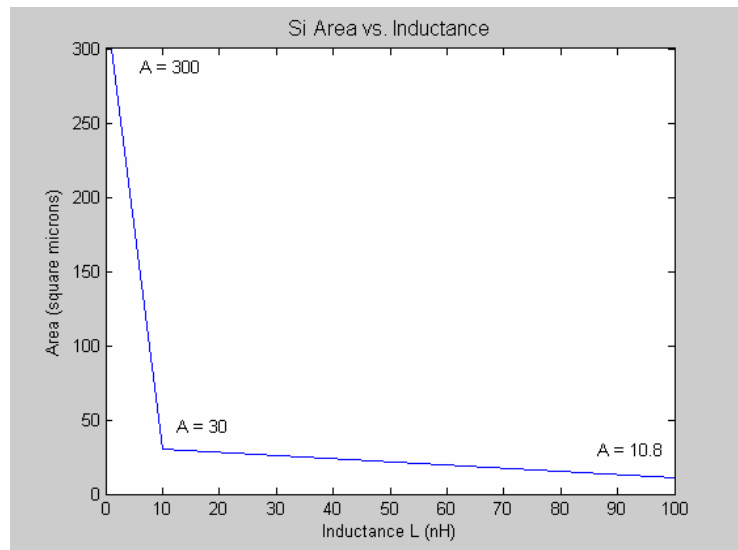


Figure 2.15: Si Area versus inductance realized.

Figure 2.15 indicates that inductor area actually decreases with increasing inductance. A dramatic reduction in chip area is realized from $L=1\text{nH}$ to $L=10\text{nH}$ and then the trend is not so radical.

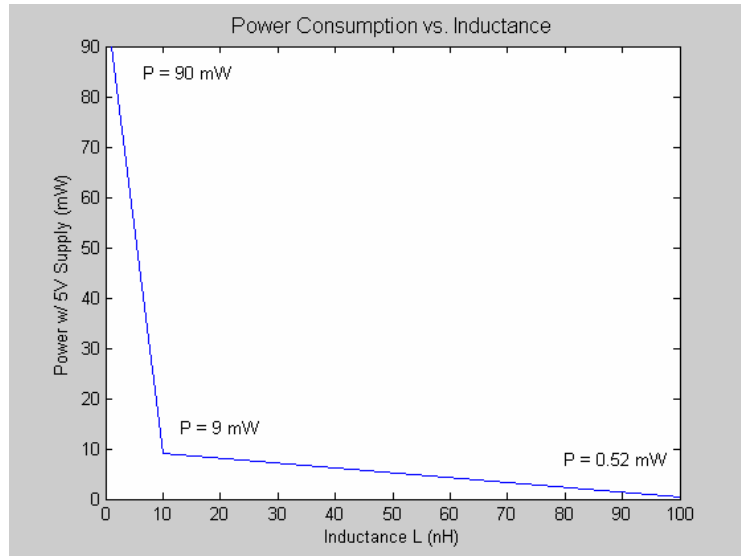


Figure 2.16: Power consumption versus inductance realized.

Figure 2.16 shows that power also reduces with greater inductances. The powers plotted above were simulated with 5 volt supplies. Another tradeoff found was that the power can be increased to increase Q . An increase in Q_{max} from 4.50 to 6.98 was realized by increasing the current I_2 from $950\mu\text{A}$ to 12mA which is a jump of over twelve times the original power consumed. At the same time the 10nH inductance fell to 7.7 nH but the SRF increased from 4.2 GHz to about 5 GHz . The main conclusion is that for any arbitrary application the SGAI can be tuned accordingly to improve the performance parameter of primary concern; however, the quality of the other performance parameters will always be limited.

Simple Cascoded Active Inductor (SCAI)

Basic Concept. In the works of both [3] and [1], a further simplified representation of the SGAI has been presented, in the form of an admittance transfer function and a parallel RLC equivalent circuit. Considering the equivalent circuit leads to the basis for adding a cascode transistor to M1. In [1], the expression for the SGAI's admittance is presented as:

$$Y_{in} \approx \frac{g_{m1}g_{m2}}{g_{ds1} + sC_{gs2}} + g_{m1} + sC_{gs1} \quad [2.9].$$

To further understand the assumptions made in [2.9], the LYSON ZTF, (eqn. 2.4), was inverted to an admittance and simplified to match equation 2.9. Lu and Liao, authors of [1], have assumed that $C_{gs1} \approx C_{gs2}$ and, in the case where a sC_{gs} term in the numerator can be cancelled, that $g_{ds1} \ll 1$ and can be omitted in the denominator. Using the reality that any useful transistor will have gain, then $g_m r_0 = \frac{g_m}{g_{ds}} \gg 1$ or $g_m \gg g_{ds}$ and a few more cancellations can be made arriving at the equivalent circuit illustrated in Figure 2.17 and the design equations 2.10:

$$\begin{aligned} L_{eq} &= \frac{C_{gs2}}{g_{m1}g_{m2}} & R_s &= \frac{g_{ds1}}{g_{m1}g_{m2}} \\ C_p &= C_{gs1} & R_p &= \frac{1}{g_{m1}} \end{aligned} \quad [2.10].$$

In [2.10], L_{eq} and R_s are the quantities that dominate Q factor. Also, it is desired that R_p be infinite and C_p be minimal.

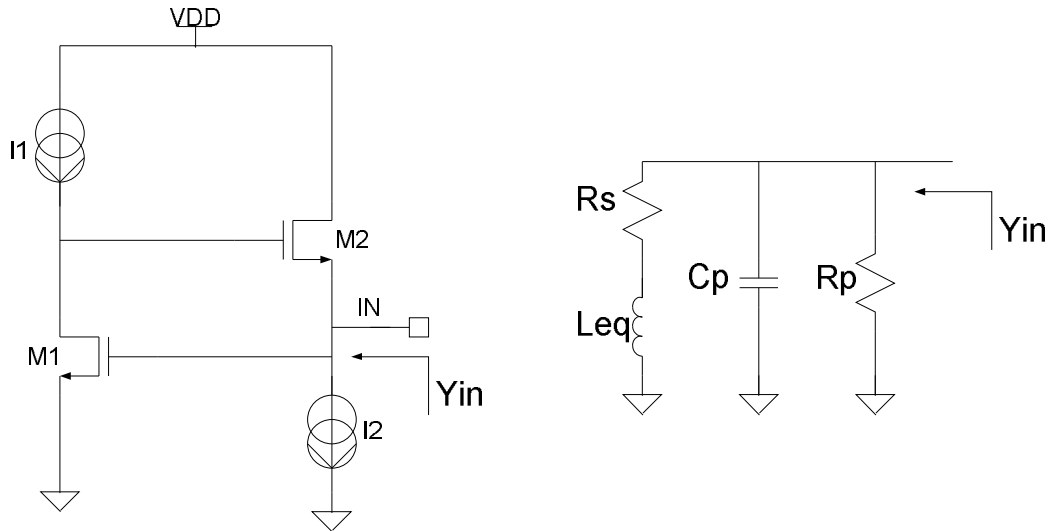


Figure 2.17: (a) SGAI circuit schematic. (b) Equivalent admittance circuit representation.

The idea of adding a cascode transistor, above M1 of the SGAI, stems from the reality that the SGAI suffers from both series and parallel resistive loss. The series resistive loss is inversely proportional to the gain of M1 ($\frac{g_{m1}}{g_{ds1}}$). Therefore, boosting the gain and output resistance of M1 by cascoding in turn reduces the series resistive loss improving Q [3]. Additionally, because this modification reduces the output conductance it also reduces the location of the zero, $\omega_z = \frac{g_{ds1}}{(C_{gd1} + C_{gd2} + C_{gs2})}$ (eqn. 2.5), predicting a larger usable bandwidth. At the same time, the parallel resistive loss can be addressed with this new topology because g_{m1} can be reduced alone while maintaining a high gain and an overall low R_S due to the addition of the cascode transistor. A different way to interpret the SCAI's improved operation is by noting that the increased resistance seen looking into the drain of M3 (see Figure 2.18) increases the likelihood that high frequency signals will integrate the capacitor C_{gs2} instead of propagating to ground

through the real impedance seen at the gate of M2. The integration of C_{gs2} is the basis of the AI's framework. However, adding the cascode device occupies voltage headroom and adds an additional high frequency pole and zero into the circuit in a manner that can lead to instability. The simple cascode active inductor (SCAI) circuit is displayed in Figure 2.18.

The following sections aim to develop the complete investigation of the SCAI and its feasibility in standard IC processes. Simulated results demonstrating the enhanced performance achievable by the SCAI are presented. The design methodology used to realize different inductances is described. Finally, several conclusions are drawn and the practicality of these devices in the C5 process is revealed.

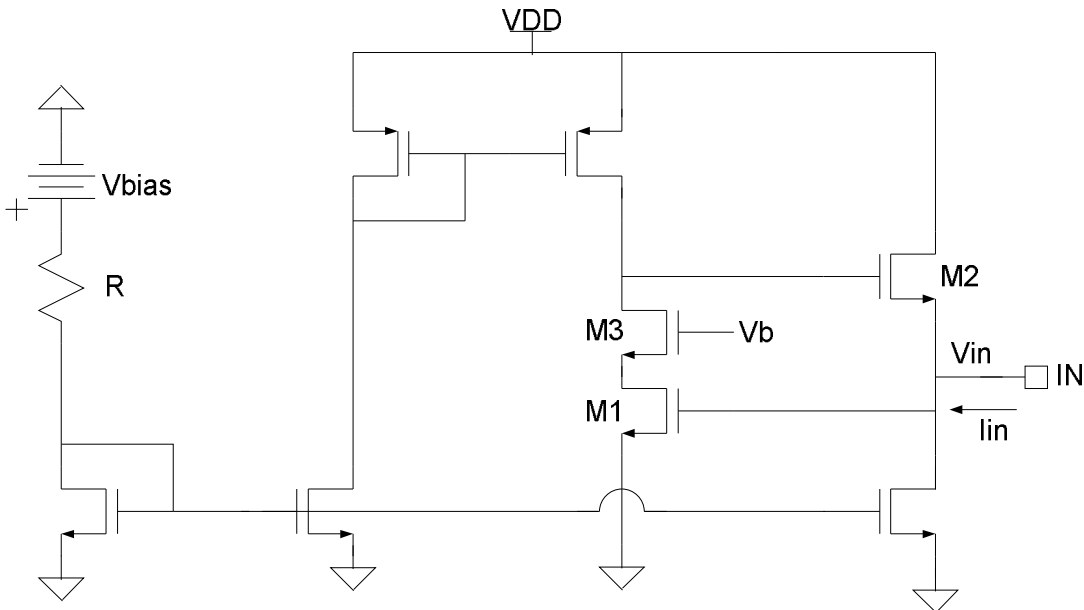


Figure 2.18: Simple Cascode Active Inductor circuit schematic.

SCAI Simulation-Based Performance and Results. A 22.5nH inductor at 500MHz was designed, using both the SGAI and SCAI topologies, and are compared via transistor level simulations in this section. Both designs employ simple CMs for current biasing,

the same supply voltage and simulation setup. The goal of attaining a 22.5nH inductance was initially targeted for possible use in a 2-way Wilkinson power divider operating at 500MHz. The objective was to achieve this inductance while optimizing the achievable Q at this frequency. On the following page, plots demonstrating the real and imaginary impedance of each topology are plotted versus frequency to validate the expected results of adding a cascoding device.

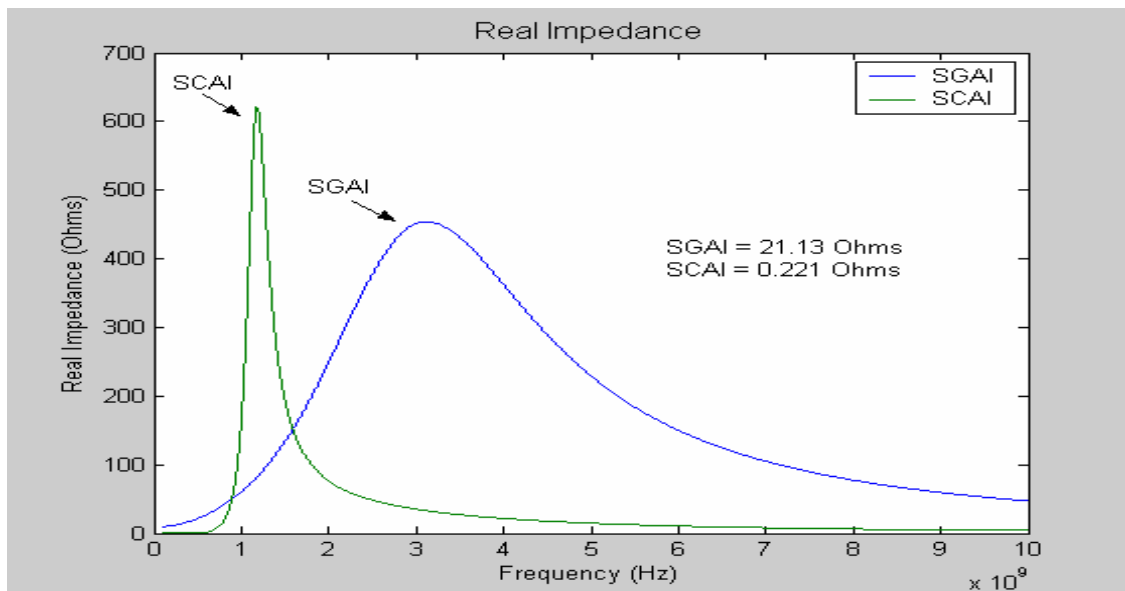


Figure 2.19: Real impedance of the 22.5nH SGAI and SCAI inductors. Note that both quoted R values are at $f = 500\text{MHz}$.

As expected, the SCAI significantly reduced the input resistance at the frequency of interest. This is due to a combination of reduced series resistance and increased parallel resistance. The sharper curve can be attributed to the new pole and zero added to the overall behavior.

Figure 2.20 shows the imaginary impedance of both the SCAI and the SGAI inductors. Because both inductors were designed to be 22.5nH at 500MHz the curves intersect at this frequency. The curves show little deviation from each other at low

frequencies. The plot was graphed on a linear-linear scale to show the linear relationship of the reactance at low frequency.

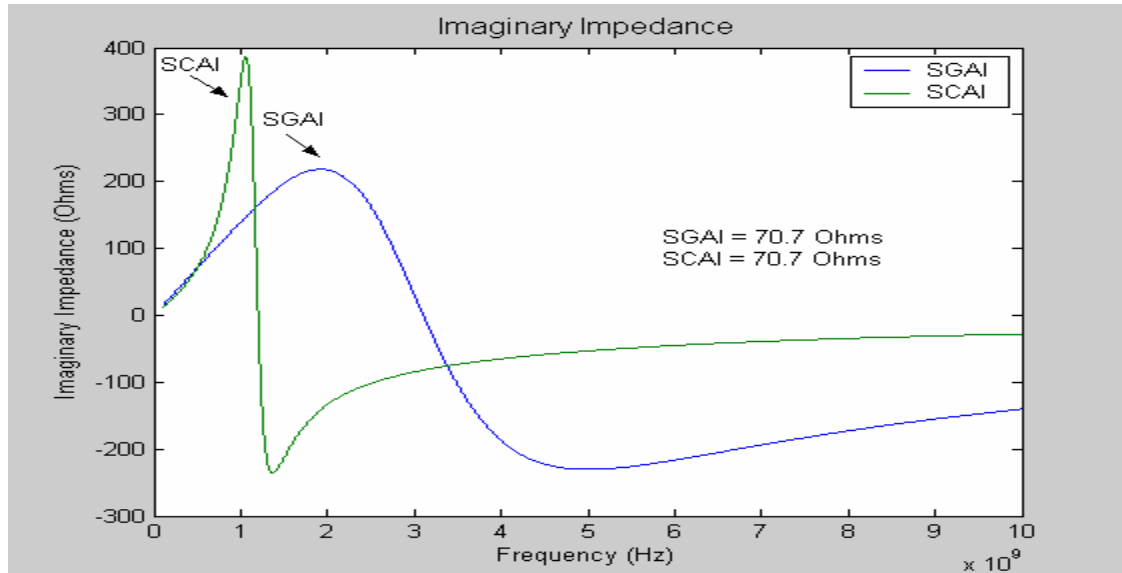


Figure 2.20: Imaginary impedance of the 22.5nH SGAI and SCAI inductors. Note that both quoted X values are at $f = 500\text{MHz}$.

With the chosen sizing and bias of each topology, the effective g_{m1} of the SCAI is larger than the effective g_{m1} of the SGAI design which attributes the lower imaginary impedance seen at low frequency. Again it is easily observed that the imaginary impedance curve of the cascode topology is sharper in character in comparison to the SGAI imaginary impedance curve. Generally, a steeper reactance denotes a better inductor, or resonator, in terms of quality. While near resonance, a valid Q definition, derived from [2.1], is:

$$Q = \left[\frac{\omega}{2R_s} \cdot \frac{dX}{d\omega} \right] \quad [2.11].$$

From [2.11] it is seen that Q is directly proportional to the slope of the reactance in the vicinity of the resonant frequency.

With the realized SCAI significantly reducing the input resistance for a specific imaginary impedance, and recalling that $Q = \frac{|\text{Im}[Z]|}{|\text{Re}[Z]|}$ (eqn. 2.2), this topology has achieved momentous improvement in terms of Q. Figure 2.21 plots the Q factor of each topology versus frequency. The SCAI Q factor towers over the predominately flat Q factor of the SGAI at the frequency of interest.

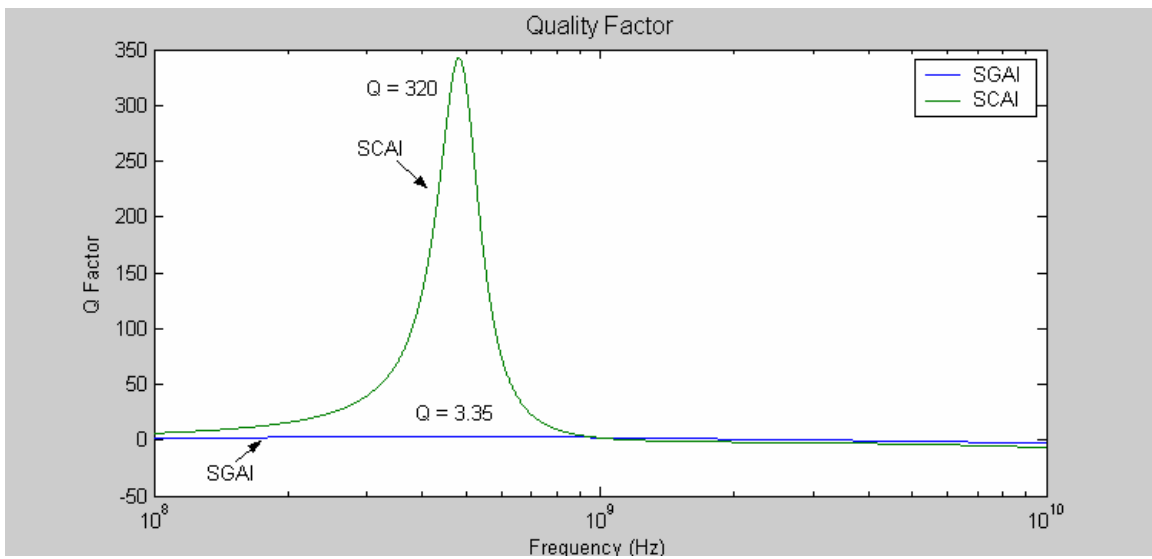


Figure 2.21: Q comparison of the 22.5nH SGAI and SCAI topologies. Note that both quoted Q values are at $f = 500\text{MHz}$.

There is no doubt that the SCAI outperforms the SGAI in terms of Q and appears to be a promising addition to realizable standard IC components. The trend between Q and SRF remains consistent as found previously for the SGAI. Designing for high Q reduces the circuit's obtainable SRF. In addition, by rough estimate, the enhanced performance of the designed SCAI would require approximately three times the area as the SGAI. The SCAI design also requires additional power than the SGAI, 5.1mW

versus 3.4mW. However, all of the inherent tradeoffs are extremely reasonable consequences for the boosted Q.

SCAI Design Methodology. Within the work of this thesis a specific design method was identified to realize SCAIs in a somewhat systematic manner. The methodology used to design SCAIs always began with the design of a SGAI for the targeted inductance. Initially, ideal current sources were used to simplify the design. Once the desired inductance was realized, the cascode transistor, with minimum channel length, was added into the circuit. Using the simulator's tuning capabilities the widths and bias currents were tuned in accordance with the equivalent circuit (Figure 2.17) and its governing equations presented as equation 2.10. After the inductance was realized with acceptable Q and SRF the bias current mirroring circuitry was added to the circuit. It was found that a small current deviation from the ideal current along with the added resistance and capacitance of the CMs caused severe degradation in the realized Q and L. Using cascoded CMs for a higher accuracy of bias generation was attempted but was found to place a constriction on V_{in} , or V_{gs1} , to two overdrive voltages which was undesirable. Keeping the circuit simple along with maintaining the designed size of M1, in order to realize the specific parameter values, was the reason for abandoning the cascode CM idea. The final step in the design process was to use the simulator to perform small tweaks in all of the design parameters until an adequate combination of L, Q and SRF was realized.

It was experienced that the simulated values of L follow the first-hand design equation trends [2.10], in terms of C_{gs2} , g_{m1} and g_{m2} variation, much closer at low

frequency. In fact, at design frequencies much less than the transistor f_T , the inductance could be reliably designed by simply setting the g_m and C_{gs} of each transistor accordingly. At these lower frequencies the VHF ZTF and the LYSON ZTF do not vary significantly in prediction. Therefore, the previously chastised assumptions that were declared in [2] were found to be valid at frequencies much lower than the transistor f_T . This reality still contradicts the author's statement of intended use near the transistor's f_T .

Effect of Process Variation on the SCAI's Characteristics. The previous discussion of the design process outlined the design of a 22.5nH SCAI that was tuned to realize a large Q (320), high SRF (1.2GHz) and an unconditionally stable state of operation for the typical process parameters. By stating unconditionally stable, it is strictly meant that the resistance seen at the input is positive over all frequencies simulated (100MHz to 10GHz). However, after running a process corner analysis, the AI design topologies presented thus far were found to be sensitive to the process variation innate to the C5 process used. Interestingly, none of the referenced sources of literature, on the topic of AIs, have addressed the manufacturability issues encountered in this work. Over the extremity of the corners, it was found that the SCAI's performance, key FOMs and stability vary far too much to prove reliable in a fabrication run. On the next page, Figure 2.22, presents the inductance and Q at the typical process parameter and at each of the process corners.

Observe that, in comparison with the typical process corner, the worst case power (wcp) inductance has been effectively halved. In the case of the worst case speed (wcs) parameters the inductance doubled at 500MHz. In addition, the worst case zero (wc0)

process corner shows instability at the frequency of interested because Q is negative implying that the input resistance is negative at 500MHz. In summary, over the possible processing parameter range, there is far too much variation in the performance of the SCAI and its key FOMs. Because the SGAI did not exhibit acceptable Q values, it was not even considered for a fabrication run or for a corner analysis.

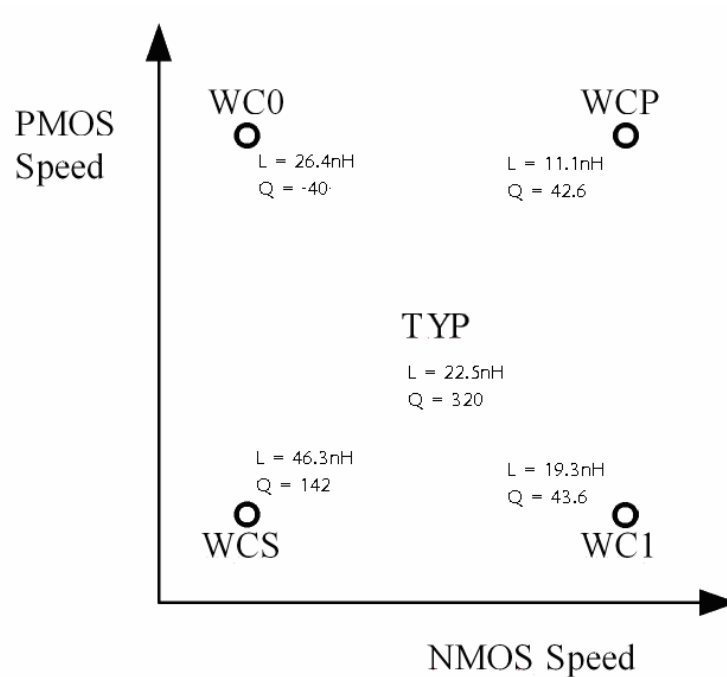


Figure 2.22: Inductance and Q , at 500MHz, for the SCAI over the process parameters.

AI Bias Current Variation. A simple simulation was run to see the variations the typical AI could withstand before skewing too far in both performance and stability. I_1 was swept over several current bias points and the resulting inductance, Q and stability was monitored. Figure 2.23 depicts the results of the simulation run.

From the plot it is seen that on the low end of the spectrum there is a 10% deviation in inductance which is too much to be useful in a Wilkinson application. On the high end of the spectrum the active inductor is pushed into an unstable region

corresponding to a high frequency pole traveling into the right hand plane. A little over a 2% increase in I_1 , for this specific device, produces a negative resistance demonstrating how sensitive the AI can be.

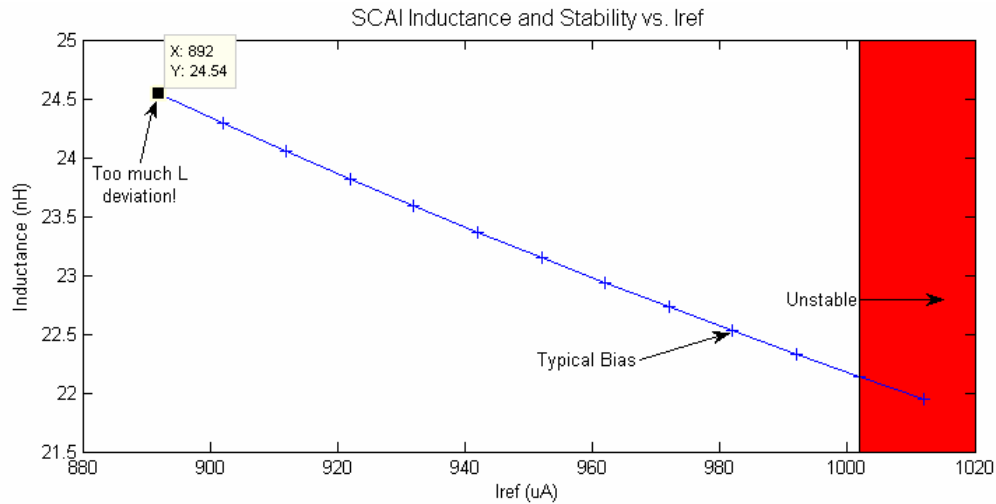


Figure 2.23: Inductance and stability versus I_1 current bias.

Conclusions and the Need for Future Research.

Due to the undesirable variation of the SCAI over the C5 process corners the need for more robust design techniques are required in order to design and fabricate reliable AIs. To determine an acceptable amount of skew in L and Q a simple simulation of a Wilkinson power divider with different inductances and series resistances was run. For a two-way Wilkinson power divider, a Q greater than 20 and an inductance within a few nanohenries (nH) would support high performance. In the context of an oscillator different criteria dictate what is acceptable for the tank's inductance. Because the frequency of oscillation is related to the tank's L and C , values the specific application would dictate the allowable skew in L . As always the largest attainable Q is desired.

CHAPTER THREE

ACTIVE INDUCTOR AUTOMATIC TUNING SCHEME

Introduction to Tuning Scheme

As discussed previously in Chapter two, the AI alone demonstrates far too much variance in inductance and Q and can become unstable over the process corners to be reliable in any given application. Therefore, in order to realize practical AIs that may find use in an IC process, on-chip automatic tuning must be employed to fine tune the AI into a region of operation exhibiting the desired inductance, an acceptable Q and unconditional stability. The above criteria depend on the given function for which the AI will be used. This chapter presents the investigation carried out that focused on the practicality of utilizing an automatic tuning scheme to enhance the basic SCAI. A charge-pump phase-locked loop (CPPLL) topology is the basis of the tuning arrangement [16]. The main objective of this investigation is to determine the capability of tuning the SCAI, to present the simulated performance of the phase-locked loop (PLL) topology and the tuned SCAI over the process corners and to discuss the inherent drawbacks of including additional circuit complexity.

Tuning Theory and Topology Discussion

It was recognized from the investigation carried out in Chapter two that the SCAI is very sensitive to both currents, I_1 and I_2 , generated by the CM transistors (P1 and M4). The SCAI topology is depicted below in Figure 3.1.

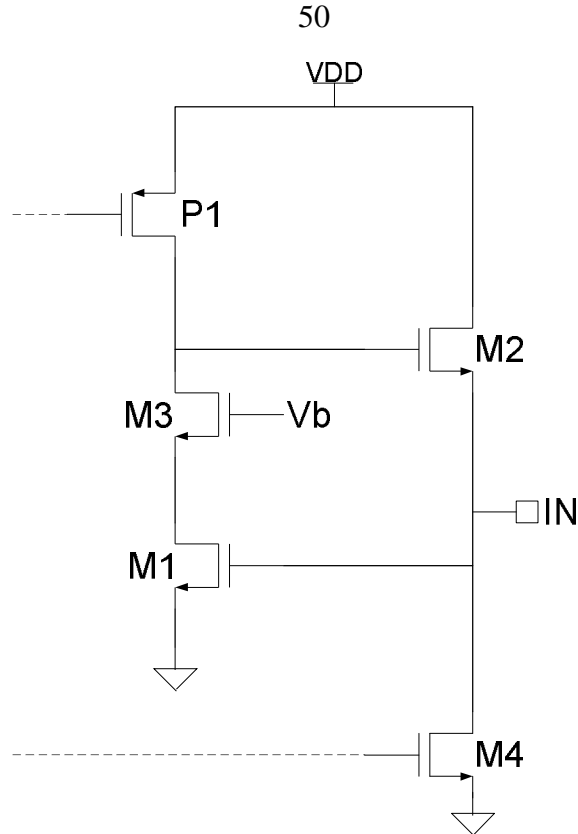


Figure 3.1: SCAI topology.

Therefore, the combination of P1's V_{gs} and M4's V_{gs} can be used to vary the AI's inductance, Q and SRF quite adequately. This is the basis of the idea employed to tune the AI over the transistor process corners. In essence, all additional circuitry is designed and configured in order to tune the V_{gs} of P1. It was demonstrated that a single control loop is sufficient to tune the inductance realized while achieving quality factors greater than fifty-five if small, negative series resistances can be allowed. This specification is application-dependent and is verified in Chapter four to be acceptable for a 50Ω -terminated Wilkinson application. It was found that in order to achieve the desired inductance, Q greater than twenty and only positive series resistance two control loops needed to be employed. Within this work, V_{gsP1} is the voltage tuned to demonstrate the

function of the control circuitry. From here on out the voltage at the gate of P1 is called V_{cont} .

The additional circuitry used in this automatic tuning scheme is a CPPLL. Simply stated, a PLL is a feedback system that compares the phase of its output signal with the phase of an input reference signal and works to minimize the differences in phase. There are six parts to the proposed CPPLL. It is helpful to explain the overall system operation and architecture briefly before developing the specific sub-designs and their functions. Figure 3.2 below shows a top-level diagram of the PLL accepting an input reference clock (REF), generating a corresponding output clock signal (FBK) and tapping the output to feed back to the input for comparison.



Figure 3.2: Top, system-level block diagram of a CPPLL.

The CPPLL designed and used within this thesis contains six essential pieces which are shown in Figure 3.3. Each of these segments are fully developed and discussed in the sub sections following. The first stage consists of a phase frequency detector (PFD) which controls a charge pump based on the phase and frequency differences of the two incoming signals. The charge pump in the second stage charges up or discharges the control voltage on the loop filter. The third stage loop filter is

necessary for stabilization and enhances the PLL's operation. The control voltage (V_{cont}) on the loop filter is the input to the voltage controlled oscillator (VCO) and dictates the output (FBK) frequency. The VCO, which includes the SCAI, makes up the fourth stage. The fifth stage consists of a comparator and an averaging circuit that transforms the sinusoidal output into a square wave signal exhibiting sharp edges. This stage performs the task of signal conditioning before the signal is fed to a digital frequency divider. The frequency divider is the sixth and final stage that reduces the output frequency of the VCO and hence the speed at which the PFD must operate.

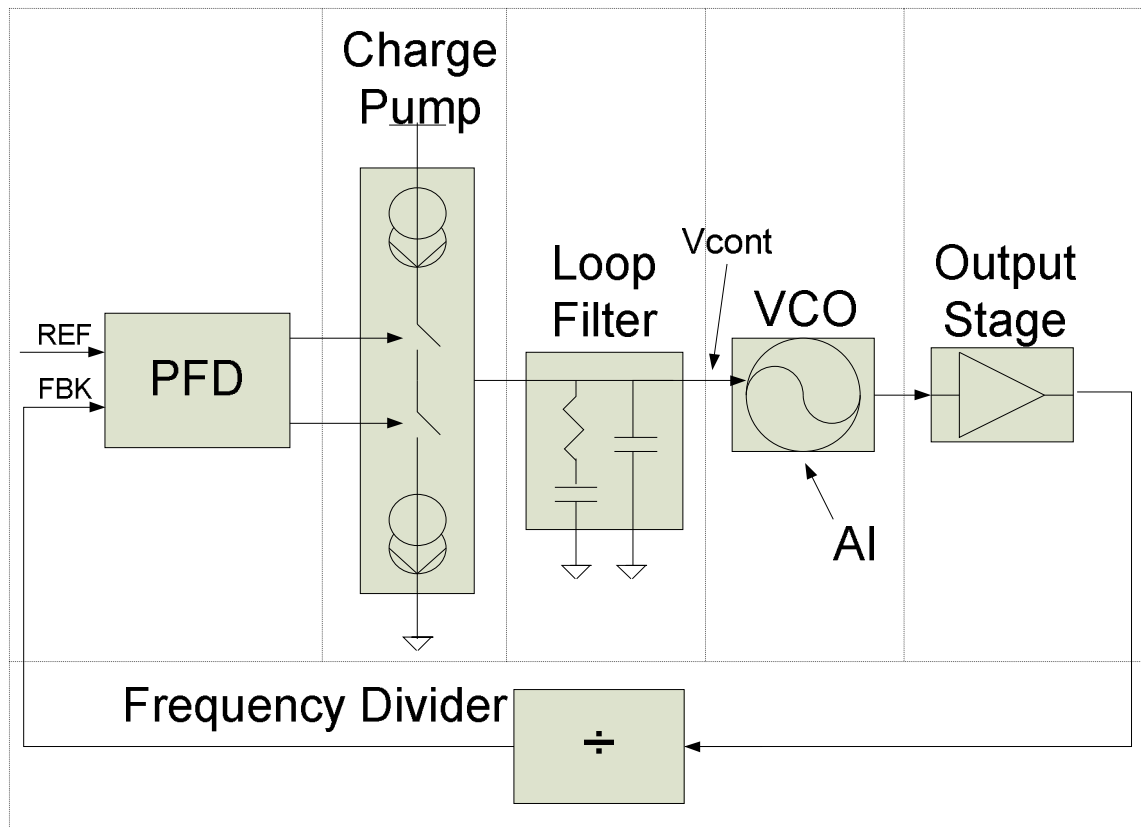


Figure 3.3: CPPLL configuration designed.

At this point it is only necessary to acknowledge that the function of a PLL is to “lock,” or align, the feedback clock signal (FBK) to the input clock signal (REF). In a

basic sense, the locking function is performed by an error signal generated by the PFD controlling the charge pump to vary V_{cont} . Varying V_{cont} correctly tunes the AI and, as a result, the VCO output frequency and phase to match that of the REF signal. Because the frequency of REF determines the steady-state value of V_{cont} , the REF frequency is set to obtain the desired V_{cont} to tune both the AI in the VCO and any other AI on chip.

Applications

The proposed on-chip automatic tuning topology, when successfully implemented opens many possibilities of using AIs in RFIC applications. The concept is that once the V_{cont} voltage is locked and stabilized this voltage is used to tune AIs in different applications around the chip. Therefore, any application involving or requiring an inductance can potentially be realized using this scheme. The application considered within the context of this thesis is the Wilkinson power divider.

Sub-Circuit Design and Operation

PFD Introduction

The input of the PLL is a logic circuit called a PFD. This circuit receives the REF and FBK signals and outputs an error signal with a DC average that is proportional to the difference in phase (Φ) and frequency (ω) of the two signals. It is informative to define the ideal PFD with a block diagram and a transfer function in a graphical format.

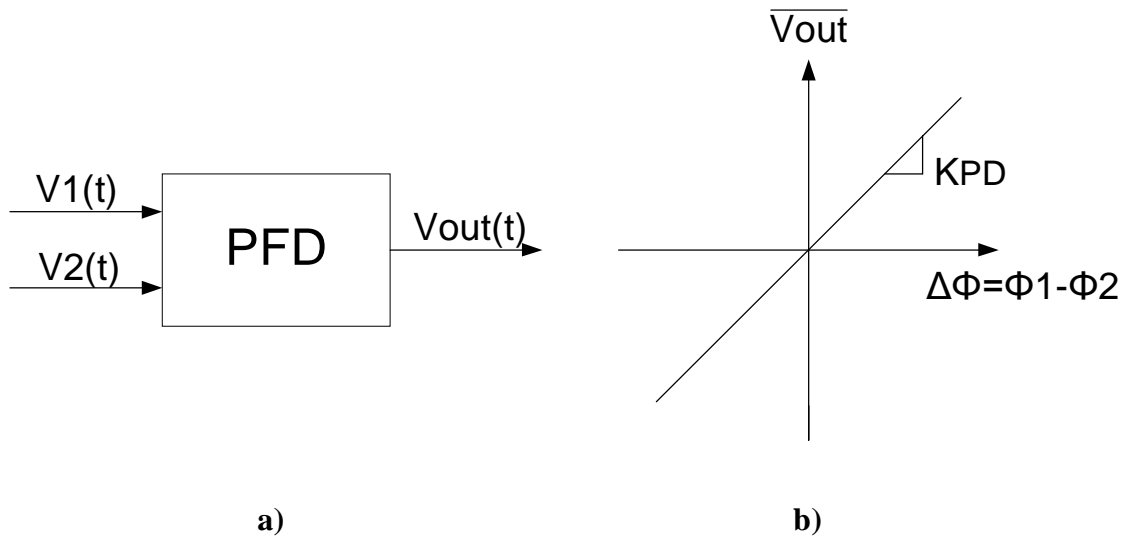


Figure 3.4: (a) PFD block diagram. (b) Transfer function curve of $Vout$ versus $\Delta\Phi$.

The slope of the transfer curve is defined as the gain of the PFD (K_{PD}) and gives an idea of the severity with which the PFD will work to control the charge-pump. K_{PD} has units of V/radians and ideally crosses the origin for $\Delta\Phi=0$.

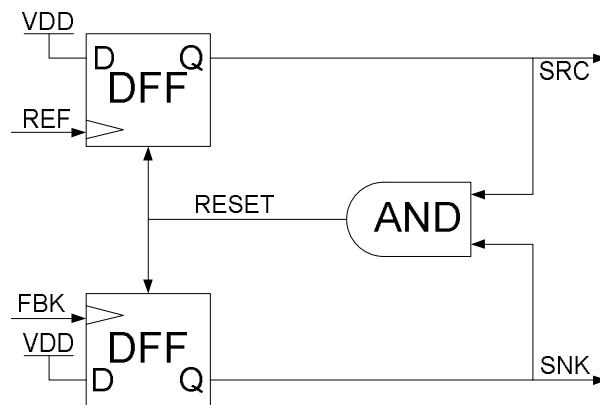


Figure 3.5: Basic PFD topology.

A basic PFD topology discussed in texts such as [9] is shown in Figure 3.5. This circuit exploits sequential logic to create three different states according to the rising

edges and the state of the two input signals. This topology is capable of correcting both frequency and phase differences in the input signals.

With the aid of Figures 3.5 and 3.6, the PFD's transient operation is described below. As noticed in the circuit schematic above, the two D inputs of the rising-edge flip flops (DFFs) are tied high to the VDD supply so that a rising edge in either of the inputs causes the corresponding Q output, SRC or SNK, to respond with a logic high pulse. In Figure 3.6(a), the first situation depicted is one in which the two signals exhibit the same frequency but demonstrate a phase difference between the two input signals. If both outputs SNK and SRC are low initially, a rising edge of the REF signal causes the SRC output to go high until a rising edge on the FBK input is sensed. Once FBK proceeds high, the high signal propagates to the SNK output, both inputs to the AND gate then become logic high causing the RESET signal to go high resetting the two DFFs to logic low levels. The SNK output experiences short pulses that trigger the reset state and are discussed in more detail below. The main concept to grasp is that the SRC output continues to output pulses with widths that are proportional to $\Phi_1 - \Phi_2$ while SNK remains quiet. Conversely, when FBK leads REF the SNK output would be the active error signal.

The other situation of interest is when $\omega_1 \neq \omega_2$, or the frequencies of the two input signals are unequal. This condition is bound to occur at the startup of the tuning circuit because initially Vcont will not equal its desired steady-state voltage. The PFD's operation is exactly the same as before. In Figure 3.6(b), REF has a higher frequency than FBK and generates pulses while SNK remains quiet. The outcomes are reversed

when FBK leads REF. The DC component of each of this circuit's output signals provide information about both $\Phi_1 - \Phi_2$ and $\omega_1 - \omega_2$. This digitized output information in the form of the SRC and SNK output signals, are used to control the charge pump suitably. Naturally, the PFD transforms signal phase and frequency information into voltage form for processing.

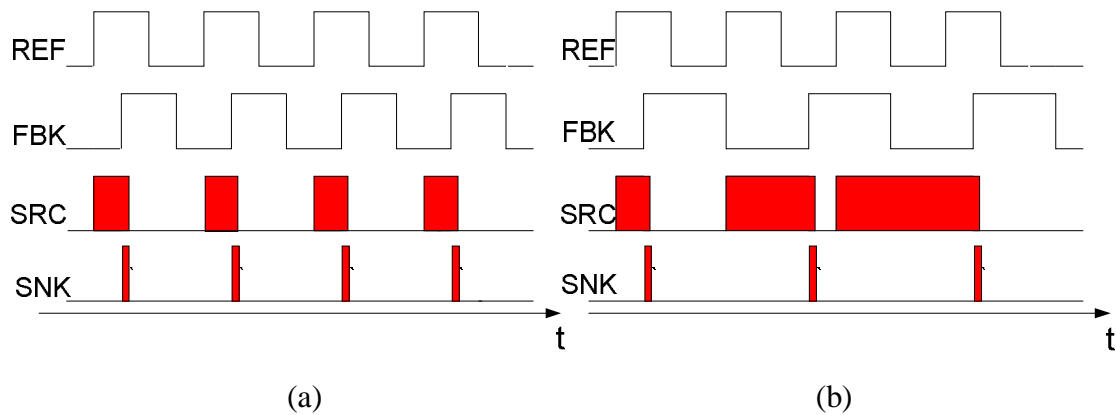


Figure 3.6: Conceptual operation of the PFD in Figure 3.5. (a) Situation where $\Phi_1 \neq \Phi_2$. (b) Situation where $\omega_1 \neq \omega_2$.

As previously mentioned, the actual behavior of the PFD includes pulses on the alternative output (SNK in Figure 3.6) due to the inherent nature of the PFD's resetting function. The reset pulses seen on the SNK signal degrade the charge pump's ability to correctly tune V_{cont} . As will be discussed in the section focused on charge pumps, the undesired pulses open the incorrect switch in the charge pump allowing the opposite effect as desired. Essentially, when the SRC output of the PFD is active high V_{cont} will increase and when SNK is active high V_{cont} decreases. Therefore, when both SRC and SNK are high V_{cont} should remain constant in an ideal scenario. An obvious enhancement to this basic PFD is to limit the duration of the reset pulse by reducing the

gate propagation of the reset function. In fact, the reset propagation delay limits the PFD's upper frequency of operation [19]. Additional enhancements can be made in the charge pump as well to reduce the magnitude of this negative effect and [19] address this issue.

In the linear region of the PFD transfer characteristic its gain can be obtained by the following analysis. As a reminder the gain of a PFD is the average change in the output voltage ($\overline{V_{out}}$) divided by the corresponding difference in the two compared phases ($\Delta\Phi$):

$$K_{PD} = \frac{\overline{V_{out}}}{\Delta\Phi} \quad [3.1].$$

For every period the average output voltage changes by $\frac{V_0 \cdot \Delta\Phi}{2\pi}$ where V_0 is the 5V supply and the PFD gain K_{PD} equals $\frac{V_0}{2\pi}$. Therefore, the implemented PFD exhibits a $K_{PD} = 0.795775 \frac{Volts}{rad}$ which is a necessary quantity in the PLL transfer function and stability analysis presented later.

Charge Pump

In the most basic topology a charge pump consists of two current sources that are switched on or off according to two logical input signals (SRC and SNK) to pump charge onto or off of the loop filter in the third stage of the PLL. As shown in Figure 3.7, the SRC signal controls the sourcing current source (I1) and the SNK signal controls the sinking current source (I2) of this intuitive charge pump. When the SRC signal is logic high, the top switch is closed, the bottom switch is open because SNK is logic low and

current from I_1 is pumped into the loop filter increasing V_{cont} . Oppositely, if SNK is high and SRC is low, I_2 will sink charge off of V_{cont} thereby lowering this voltage.

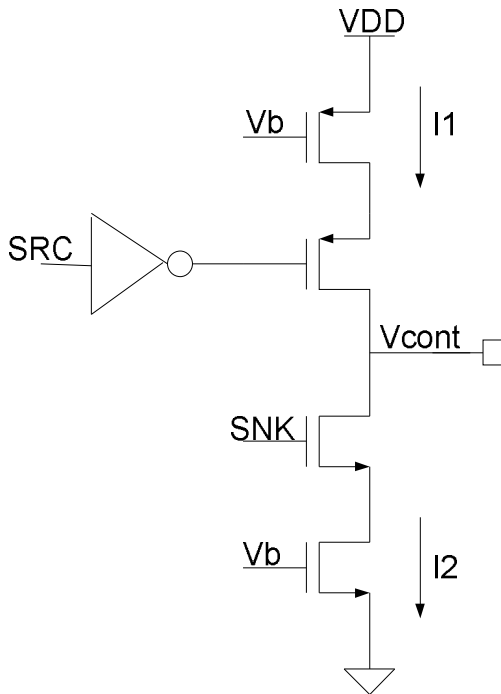


Figure 3.7: Basic charge pump topology.

Enhancements were made on the topology of Figure 3.7 to improve the circuit's performance in several different ways. Due to the switching arrangement, the basic charge pump topology suffers from a well-known phenomenon called channel charge injection. When any transistor is turned from on to off, in the fashion of a switch, the charge carriers that have accumulated under its gate forming the transistor's channel for an "on" operation must exit through both the source and the drain terminals. Consequently, a sufficient amount of charge is dumped onto V_{cont} from this type of switching topology and causes wiggle or "jitter" on V_{cont} . Jitter introduces negative repercussions because it effectively modulates the VCO frequency. A clever switching assembly avoids this issue and is depicted in Figure 3.8. P1-P2 and M1-M2 operate as

tightly matched linear resistors when switched on. Otherwise, P1 and M1 are turned off and no current can flow to or from Vcont.

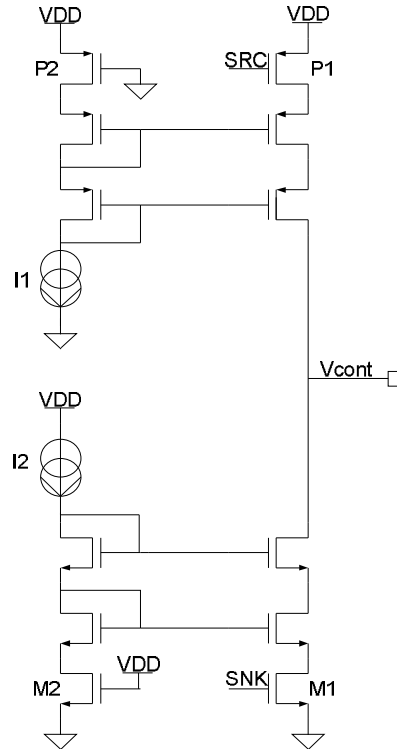


Figure 3.8: Enhanced charge pump circuit schematic.

A further improvement to the switching arrangement was included in the form of using a cascode CM topology in place of a regular current mirror configuration. This topology was used in order to increase the accuracy of the currents mirrored and is easily realizable in a 5V design due to the abundance of headroom. Cascode arrangements increase the resistance seen looking into the current generation devices and regulate the V_{ds} (drain to source voltage) of the mirroring device more closely to that of the diode-connected transistor. As discussed in the PFD section, during the reset state of the PFD both current sources in the charge pump are turned on simultaneously. If $I_1 \neq I_2$ in the charge pump, in accordance with Kirchoff's current law, charge will either be sourced

onto or sunk from V_{cont} leading to an undesirable error on the control voltage. Using a low voltage process with little headroom to spare, techniques other than cascoding may need to be employed.

Loop Filter

Stage three of the CPPLL consists of a simple, passive low pass filter (LPF) which is employed for several different and essential reasons. The LPF is shown in Figure 3.9. As formerly suggested, the implementation of a LPF on the V_{cont} node reduces high amounts of ripple on this susceptible and extremely important voltage. A less obvious reason for the requirement of a LPF at this node in the circuit is the need for a feed-forward zero to stabilize the PLL's transfer function. This realization in the frequency domain is used to add phase to a potentially unstable system and is very similar to a lead compensator system discussed in basic control theory. The added parallel capacitor C_P has a dramatic influence on further depreciating any ripple on V_{cont} . A simple analysis demonstrates that when C_P is less than a fifth of the capacitance of C it has a negligible effect on the introduced zero location [9].

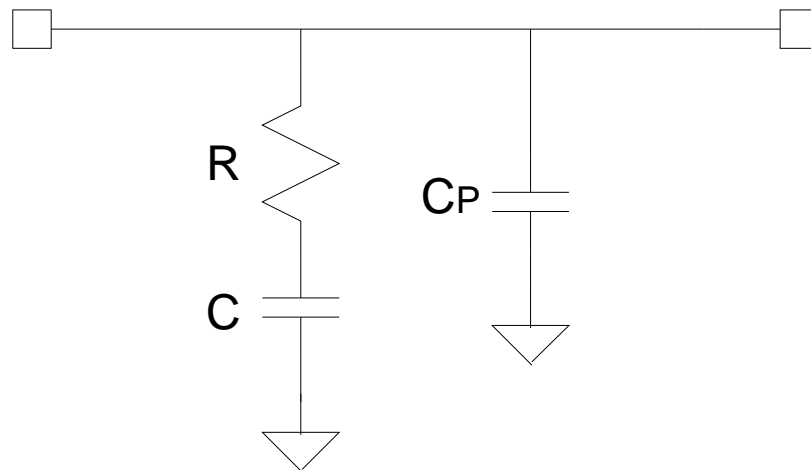


Figure 3.9: LPF circuit.

The LPF is absolutely essential to ensure stability and consequently the circuit's transfer function must be considered and is presented here:

$$H(s) = \frac{(sRC + 1)}{(s(sRCC_p + C + C_p))} \quad [3.2].$$

Because each stage contributes to the operation and stability of the CPPLL as a complete system, the final stability analysis is presented following the discussion of the final three stages.

Colpitt's VCO

Oscillators are commonly referred to as signal generating devices and are a fundamental part of various RFIC circuits. In the context of the automatic tuning application designed within this thesis the VCO is used as a clock generating source to provide the FBK signal to the input of the PFD. The tremendous importance of the VCO, in the tuning configuration presented, is inevitable due to its incorporation of the tunable SCAI.

An oscillator is simply a feedback system realizing right hand plane (RHP) poles. This is the opposite s-plane characteristic of familiar IC circuits such as operational amplifiers, control systems and continuous-time filters. In other words, an oscillator's fundamental operation stems from positive feedback. In the desired circumstance of producing a periodic output waveform the criteria stated above prove extremely useful.

The exact VCO circuit schematic used for the clock-generating source in the PLL is presented in Figure 3.10. This circuit, a Colpitt's oscillator, is titled after its inventor.

This particular oscillator can be realized in three different forms. Due to the grounded inductor constraint of the SCAI, the Colpitt's oscillator topology shown in Figure 3.10 was selected.

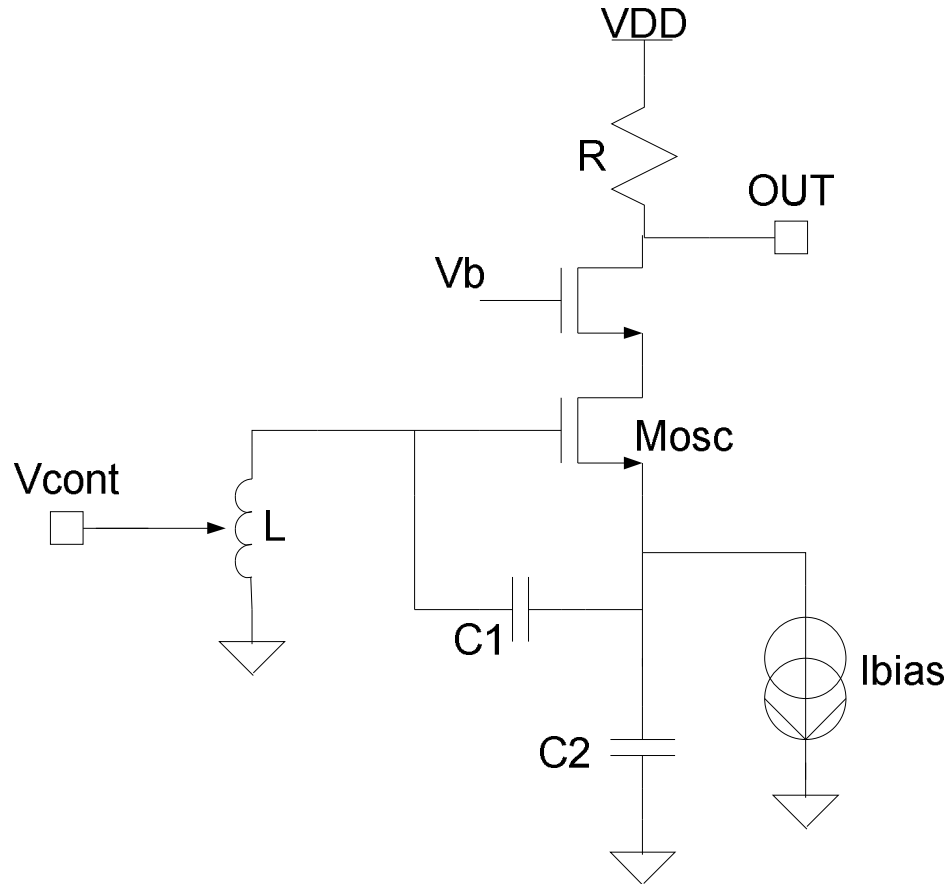


Figure 3.10: VCO schematic employing the SCAI denoted as L.

The Colpitt's VCO design is based on both active and passive components comprising a resonant circuit. The VCO oscillates at the frequency where the magnitude of the feedback impedance is infinite. For an LC Colpitt's oscillator the oscillation frequency is commonly approximated as:

$$f_{osc} = \frac{1}{2\pi \sqrt{L \cdot \frac{C_1 \cdot C_2}{C_1 + C_2}}} \quad [3.3].$$

The gain, K_{VCO} , of the VCO was determined through a simulation that swept V_{cont} and monitored the output frequency. The graphical result of this simulation is included in Figure 3.11.

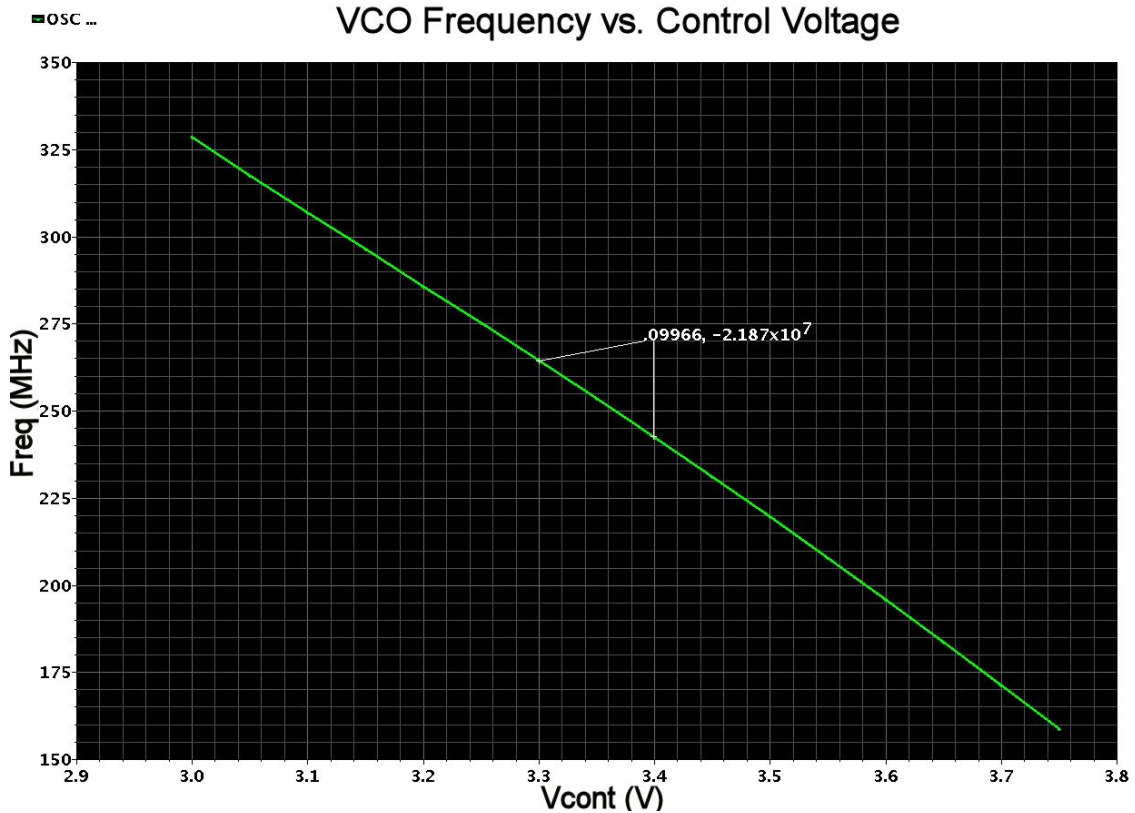


Figure 3.11: VCO frequency versus V_{cont} swept results. The slope of this curve is approximately K_{VCO} .

$$K_{VCO} \approx -219.446 \frac{MHz}{V} \quad [3.4]$$

The reality that the resulting VCO gain is negative makes sense. If V_{cont} is rising, I_1 in the AI is decreasing (p channel CM) and therefore the $g_{m_{M1}}$ is also decreasing. Because the inductance of the AI is inversely proportional to $g_{m_{M1}}$ the inductance consequently increases and the frequency decreases according to equation 3.3.

Employing the inductance L above, in the form of the tunable SCAI studied in Chapter two, enables the “voltage-controlled” functionality of this oscillator topology. By varying V_{cont} the inductance can be varied accordingly thereby changing the output frequency of oscillation consistent with [3.3]. Because the VCO shown in Figure 3.10 outputs a sinusoidal signal, fed back for comparison with the input reference signal, an output stage is required.

Many considerations went into the VCO design. The AI was previously designed for 45nH at 250MHz. Therefore, initially the feedback capacitors were sized to be approximately 18pF so that according to equation 3.3 the output frequency would be 250MHz. Transistor M_{osc} , as shown in Figure 3.10, was sized to generate enough gain for ringing yet was minimized to lower the amount of parasitic capacitance added to the feedback arrangement. In addition, the sizing of this transistor effects the amount of signal swing on its drain, gate and source terminals which was of concern in order to keep all transistors on. Another key phenomenon of concern was biasing M_{osc} in a manner that maintained a positive voltage on its source. Otherwise, with signal swing transposed on top of the DC operating point at this node, a negative voltage forward biases the pn junction from bulk to source which is undesirable. Because $M1$ of the SCAI dictates M_{osc} 's DC gate voltage, the source voltage is determined by the V_{gs} of M_{osc} required for the bias current I_{bias} . Additionally, the low end of the signal swing on M_{osc} 's gate had to be limited to an amount where $M1$ of the AI remained turned on in strong inversion. In the case where the swing on the gate of M_{osc} was too large, and $M1$ was being pushed in between strong inversion and subthreshold conduction or cut off, the g_m of $M1$ would change rapidly thereby varying the inductance according to equation

2.10 where $L = \frac{C_{gs2}}{gm_1 \cdot gm_2}$. The cascode stage was added to increase the gain of the oscillator without adding additional capacitance to M_{osc} and while suppressing the effective Miller capacitance at the gate. R was included in order to set the DC output level.

Comparator

As named, a comparator simply compares an input signal to a reference voltage level and outputs a signal depending on the levels of these two inputs. Ideally, in Figure 3.12, when the input is larger than V_{ref} the output is logic high and when the input is lower than V_{ref} the output is logic low. The voltage reference level can be created in several different ways. In order to generate a fifty percent duty cycle square wave output the V_{ref} voltage is desired to be the DC level of the VCO output. The V_{ref} level is developed by low pass filtering the VCO output signal denoted “IN” through the use of a passive RC configuration as illustrated in Figure 3.12.

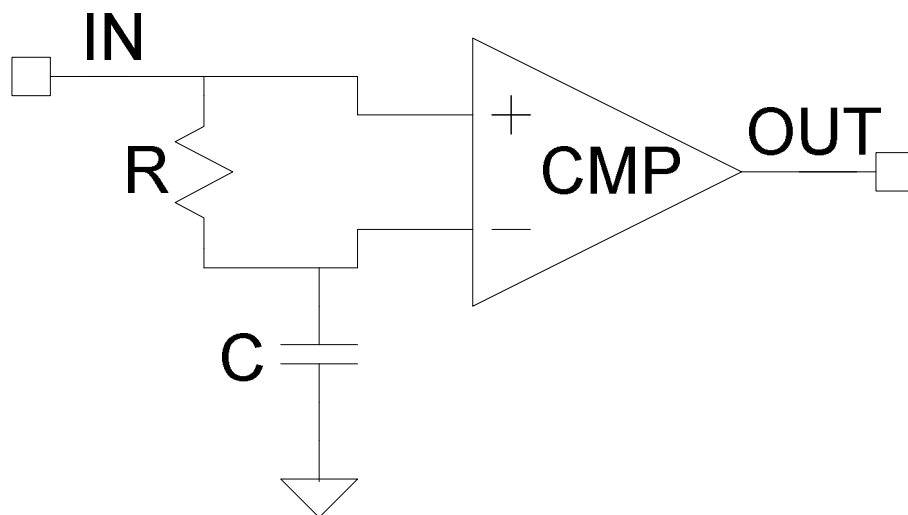


Figure 3.12: Output stage circuit diagram employing both a comparator and an averaging circuit.

The only dictating design criteria of this LPF is that the 3dB BW is desired to be much smaller than the frequency of the VCO's output signal. For this project, the corner frequency was set to:

$$f_{3dB} = \frac{1}{RC} = \frac{1}{(100k\Omega) \cdot (100pF)} = 100kHz \quad [3.5].$$

As discussed in [15], for high-speed operation a specific comparator topology is usually employed. A simple version of the implemented comparator is displayed in Figure 3.13 that employs both positive and negative feedback and is shown to aid the explanation of the comparator's operation. The negative feedback is realized through the CM transistors P1 and P2. A differential current due to the input signal flows through this node changing the V_{o1} and V_{o2} voltages that consequently turn on or off the currents supplied by P1 or P2. The positive feedback is realized in a voltage-shunt path through the gate-drain connections of transistors P3 and P4. Hysteresis will result if the aspect ratio of P3 to P1 and P4 to P2 is greater than one [15].

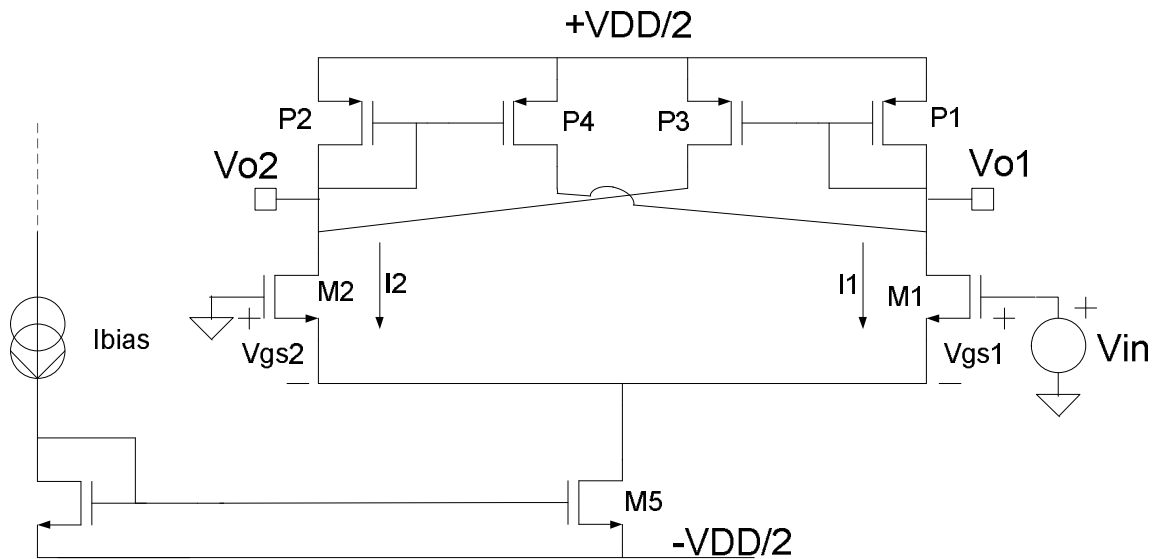


Figure 3.13: Simple comparator configuration.

The circuit's operation can be described in the following manner if plus and minus supplies are assumed, the gate of M2 is tied to zero volts and an input signal is applied to M1's gate. With V_{in} much less than zero volts transistor M1 is completely off and M2 is on. Therefore, current flows through P2 but not through M1, P3 or P1. P4 is trying to source current but due to M1's off condition it cannot. Consequently, V_{o1} is charging up and is high because all the current through the biasing transistor M5 is flowing through P2 and M2. As V_{in} increases some of I_5 begins to flow through M1. Until I_1 , the current in M1, equals the current in P4, V_{o1} remains high and the P1 transistor is off. However, as V_{in} exceeds the threshold voltage the circuit begins to change state and several phenomena occur at once. P1 begins conducting current; I_1 further increases until it equals I_5 , M2 and P2 turn off because V_{o2} becomes high [15]. A similar but opposite phenomena occurs for V_{in} transitioning from a high to low voltage. An analysis provided in [15] demonstrates that both the positive and negative trip points occur at V_{gs1} - V_{gs2} and is included in this work below.

$$I_{M5} = 250\mu A$$

$$\frac{\frac{W_{P4}}{L_{P4}}}{\frac{W_{P2}}{L_{P2}}} = \frac{\frac{W_{P3}}{L_{P3}}}{\frac{W_{P1}}{L_{P1}}} = 2$$

$$I_{P4} = 2I_{P2}$$

$$I_{P2} = \frac{I_{M5}}{1 + \left(\frac{W_{P4}}{L_{P4}}\right) \left(\frac{W_{P2}}{L_{P2}}\right)} = I_{M2} = \frac{250\mu A}{3} = 83.3\mu A$$

$$I_{M1} = I_{M5} - I_{M2} = 166.7 \mu A$$

$$V_{in} = V_{gs1} - V_{gs2} = V_{trp+}$$

Assuming $\mu_0 C_{ox}$ and V_{TH} of M1 and M2 are equal then:

$$V_{trp+} = \sqrt{\frac{2I_{M1}}{\beta}} - \sqrt{\frac{2I_{M2}}{\beta}}$$

A DC operating point simulation was carried out on the comparator and the effective β was found to equal:

$$\beta = 21.1 m \frac{A}{V} \text{ and } V_{th} = 0.9368V .$$

Therefore, the trip points were calculated to be:

$$V_{trp+} = 36.8mV \text{ and } V_{trp-} = -36.8mV .$$

This calculated result matches extremely well with the simulated experiment. The simulated V_{out} versus V_{in} results are presented in Figure 3.15.

The circuit of Figure 3.13 is rarely used as is because of insufficient voltage swings and output resistance. In Figure 3.13 V_{o1} must remain greater than the overdrive voltages of both M5 and M1 and less than $VDD - |V_{thp1}|$. Therefore, a commonly used differential-to-single-ended conversion topology is shown in Figure 3.14. In this circuit it can easily be seen that the output must remain greater than the overdrive voltage of M3 and less than VDD minus the overdrive voltage of P5 thereby increasing and balancing the output swing. It is easily acknowledged that if V_{o2} is high and V_{o1} is low, P6 and M4 are off and P5 is on pulling OUT high. Conversely, if V_{o1} is high and V_{o2} is low P5 is off, P6 is on and current is mirrored to M3 from M4 pulling down OUT.

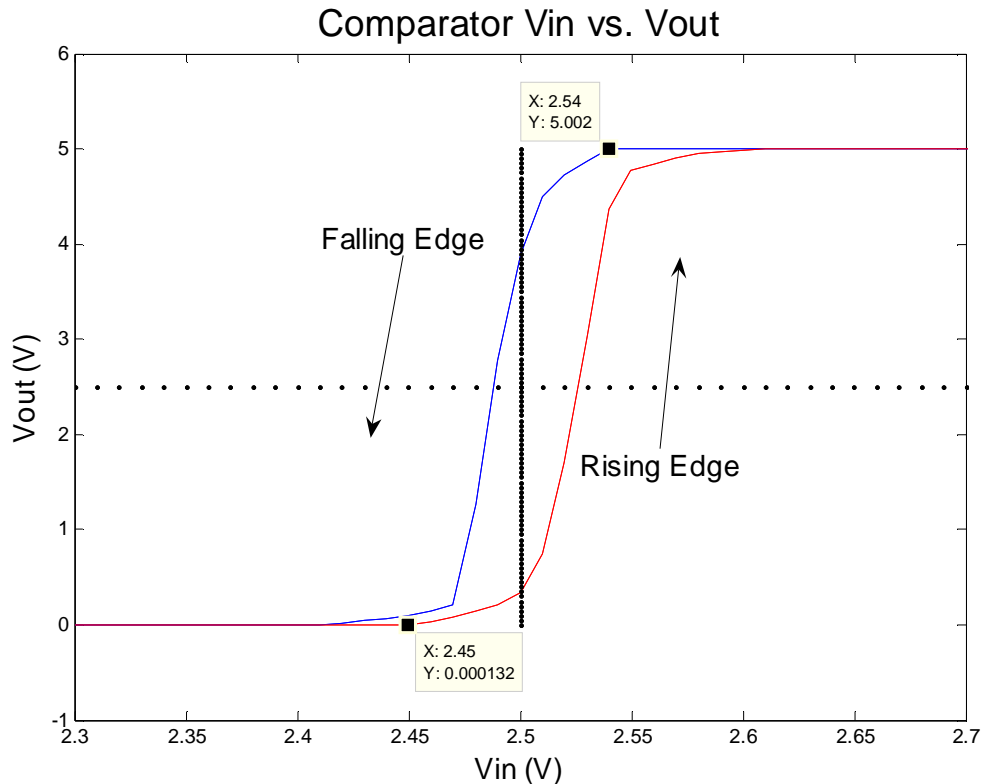


Figure 3.15: Comparator transfer curve with 40-50mV of hysteresis.

Frequency Divider

Finally, a frequency division stage is implemented in the feedback of the PLL loop. This functional block is included to slow down the feed back signal. Because the PFD's reset propagation limits its speed of operation, reducing the frequency of the feed back signal results in a more ideal operation of the PFD. A divide-by-16 circuit was chosen to down convert the feed back frequency from 250MHz to approximately 15.6MHz. The actual divide ratio of 16 was chosen primarily because divide-by- 2^n counter circuits are extremely easy to realize with DFFs. The circuit configuration is provided in Figure 3.16.

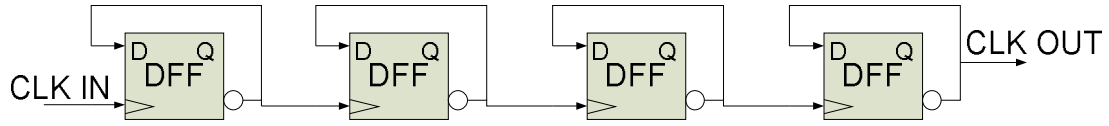


Figure 3.16: Frequency divider topology.

Connecting each flip flop in the manner shown above classifies them as toggle flip flops. With each new rising edge of the clock, the D input becomes the opposite logic value that it was during the previous cycle. Essentially, because Qnot is always fed back to D and Qnot tracks the opposite logic value of D, both these signals toggle between logic high and logic low at half the frequency of the incoming clock signal. Therefore, because the preceding flip flop's outputs are input into the clock of the sequential flip flop a divide-by-two has been realized by each DFF. Cascading four flip flops using this configuration realizes the divide-by-sixteen circuit. The output of the divider, the down-converted clock signal, is then fed back to the PFD as the FBK signal.

Transfer Function Analysis

A CPPLL transfer function is derived and presented in [9]. In order to obtain the transfer function the PLL is approximated as a linear and time invariant system. As derived in [9], the PLL transfer function is:

$$H(s) = \frac{\frac{I_P K_{VCO}}{2\pi C_P} (sR_P C_P + 1)}{s^2 + \frac{I_P K_{VCO}}{2\pi M} R_P s + \frac{I_P K_{VCO}}{2\pi C_P M}} \quad [3.6].$$

In this expression I_P is the charge pump current, K_{VCO} is the VCO gain, K_{PD} is the PFD gain, M is the feed back divide ratio and R_P and C_P are the loop filter parasitic quantities.

One can prove for themselves that without the loop filter zero the system is classified as undamped and is potentially unstable.

From control theory analysis the transfer function can be written in terms of a damping ratio (ζ) and natural frequency (ω_n):

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad [3.7].$$

This representation is convenient because the system time constant is then $\frac{1}{\zeta\omega_n}$ which provides an indication of the amount of settling time required for the system to suppress the ring on Vcont. As derived in [9], the damping ratio is:

$$\zeta = \frac{R_p}{2} \sqrt{\frac{I_p C_p}{2\pi} \frac{K_{VCO}}{M}} \quad [3.8].$$

The natural frequency is:

$$\omega_n = \sqrt{\frac{I_p}{2\pi C_p} \frac{K_{VCO}}{M}} \quad [3.9].$$

Therefore the time constant is calculated to be:

$$\frac{1}{\zeta\omega_n} = \left(\frac{R_p I_p K_{VCO}}{4\pi M} \right)^{-1} = 45.6\mu\text{s}.$$

PLL Stability

It is necessary to design a PLL that guarantees stability. This can be achieved by forcing left hand plane poles. The feed-forward zero realized in the loop filter is absolutely necessary to achieve adequate phase margin. Because the PLL naturally contains two poles at the origin ($s=0$) of the s-plane, a total phase of 180 degrees is

contributed at low frequencies. This can amount to positive feed back in systems that are initially aiming at realizing negative feed back. Therefore, the feed-forward zero is introduced prior to the unity gain crossover of the PLL's transfer function adding phase, eliminating the possibility of oscillation and stabilizing the system. Another way of envisioning how the zero stabilizes the system can be made by recognizing that placing the zero into the left hand plane entices the two complex poles to the left side of the s-plane. Using the simulated and derived values for K_{PD} and K_{VCO} and the optimized values for C_P , R_P and C_{P1} the root locus (pole-zero plot) for the PLL system is plotted below.

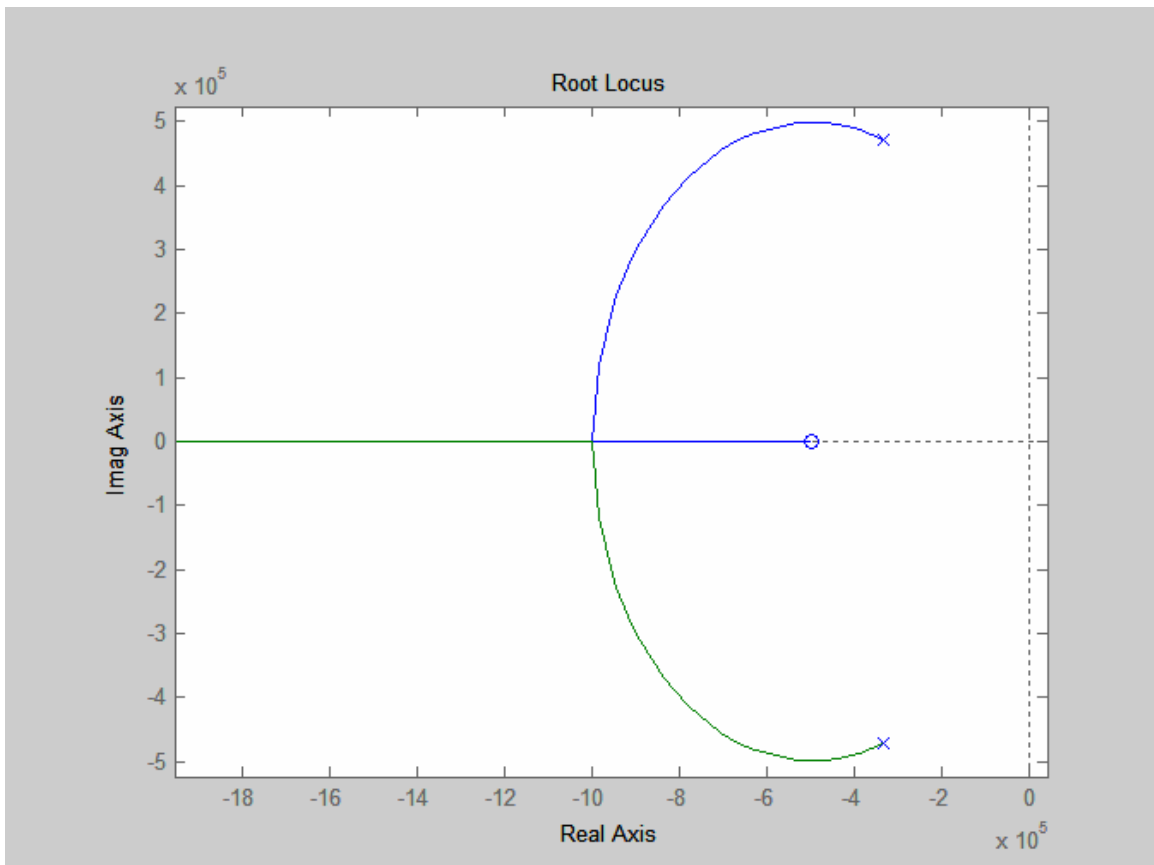


Figure 3.17: Root locus plot of the designed PLL.

As can be seen from the root locus the two poles begin in the left hand plane and approach the real axis in a conjugate symmetric fashion. Once the two poles meet they split along the real axis; one pole approaches the zero to the right and the other moves left toward $-\infty$. Bode analysis techniques can be used as well for determining a PLL's stability and are presented in [9].

Top-Level Tuning System Simulated Results

The main characteristics evaluated when simulating a PLL are the locking of the control voltage waveform and the phase and frequency deviations of the two clocked signals REF and FBK. In order for the PLL to work properly V_{cont} must lock at the correct voltage, the frequency of FBK and REF are required to be equal and the phase deviation between the two signals is desired to be minimal. This section presents the simulated waveform results and the fundamental qualities of the PLL's locked voltage, jitter, settling time and phase error are discussed.

Control Voltage

The control voltage, V_{cont} , is the key voltage that tunes the inductor to its desired inductance and quality. As mentioned previously, while tuning the inductor, this voltage is also tuning the entire VCO so that its output frequency and phase will match FBK with REF. It is therefore desirable that V_{cont} lock to the desired predetermined quantity. The full plot of V_{cont} is shown in Figure 3.18 for nominal conditions. The PLL locks V_{cont} at exactly 3.363V to output approximately 250MHz from the VCO.

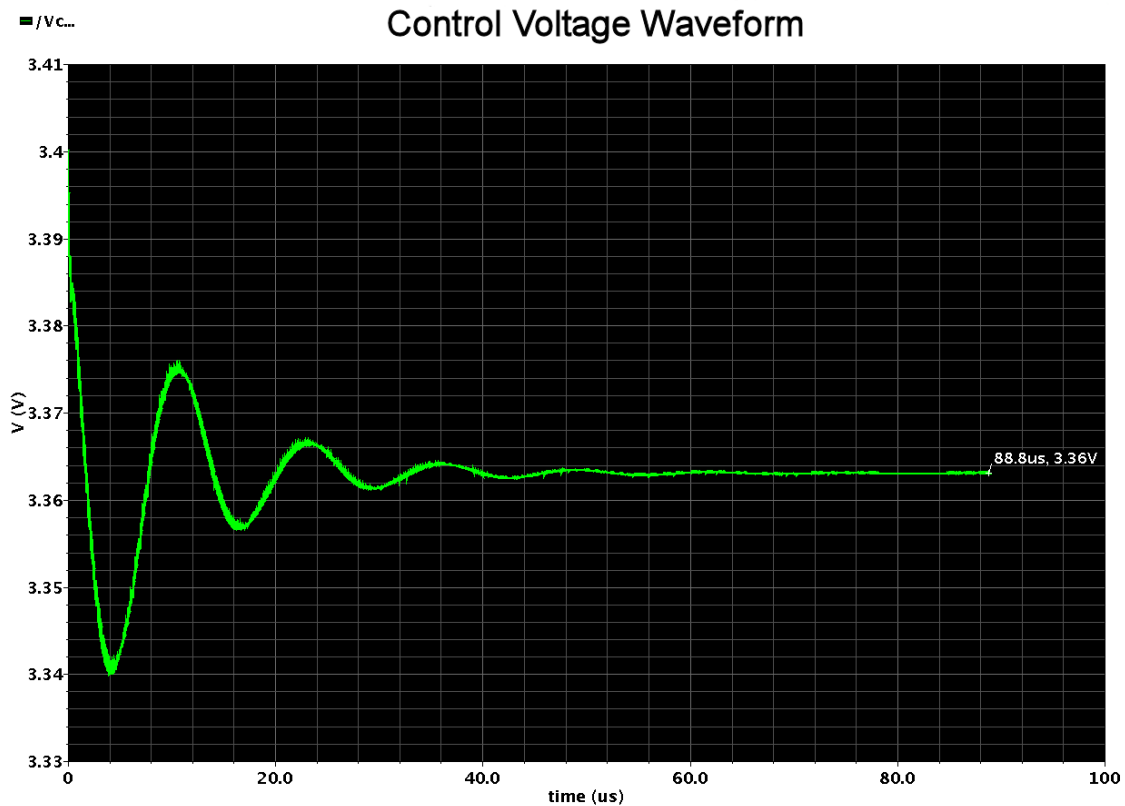


Figure 3.18: Control voltage locked at 3.363 V under typical transistor parameters.

Underdamped Response. The appearance of the waveform shown in Figure 3.18 is immediately identified as an underdamped system response. This is the expected response because the PLL has two complex poles in the left hand plane. When V_{cont} is high, FBK is too slow and the system works to pull V_{cont} back down to speed up the FBK signal and vice versa. It is acknowledged that by altering the resistance in the loop filter this system could easily be forced to respond in a critically damped fashion.

Settling Time. The amount of settling time appears to be roughly 70 to 80 μ s once V_{cont} is in the vicinity of its locking value. This is a fairly close realization in comparison to the calculated quantity of 45.6 μ s. This figure of merit gives an indication

of how long it takes the PLL to pull the two signals into phase and equal frequency. Settling time generally trades off with the magnitude of jitter and PLL stability. For instance, increasing the charge pump current will allow the voltage on the control node to change more substantially each clock cycle reducing the settling time and increasing the circuit's margin of stability while increasing the jitter. It is mentioned in [9] that as the resistance in the loop filter increases to extremely large values the stability begins to degrade although the transfer function predicts the opposite effect. This occurs because of the approximation made in order to obtain the transfer function.

Vcont Jitter Magnitude. Because jitter on Vcont varies the inductance and VCO output frequency this phenomenon is not desired. Jitter modulates the output frequency of the VCO. Consequently, the amount of jitter is a quantity that must be examined for a PLL. Each application dictates the amount of jitter that is acceptable for the design. Figure 3.19 illustrates the jitter produced by the tuning PLL at nominal circuit conditions. The greatest jump in Vcont is marked in the plot above. The largest amount of jitter experienced on the control voltage is approximately $68.43\mu\text{V}$. Notice that Vcont is in its locked state at an average voltage of about 3.363V.

Allowable Jitter. The allowable amount of jitter was determined to be approximately one hundred milli-volts for this application. This jitter specification was obtained by simulating the AI with jitter on its bias node while ensuring acceptable performance. Larger magnitudes of jitter resulted in the AI's inductance and quality skewing far too much to be practical in a high-Q application. This reality traces back to M1 of the AI clipping into the subthreshold conduction region.

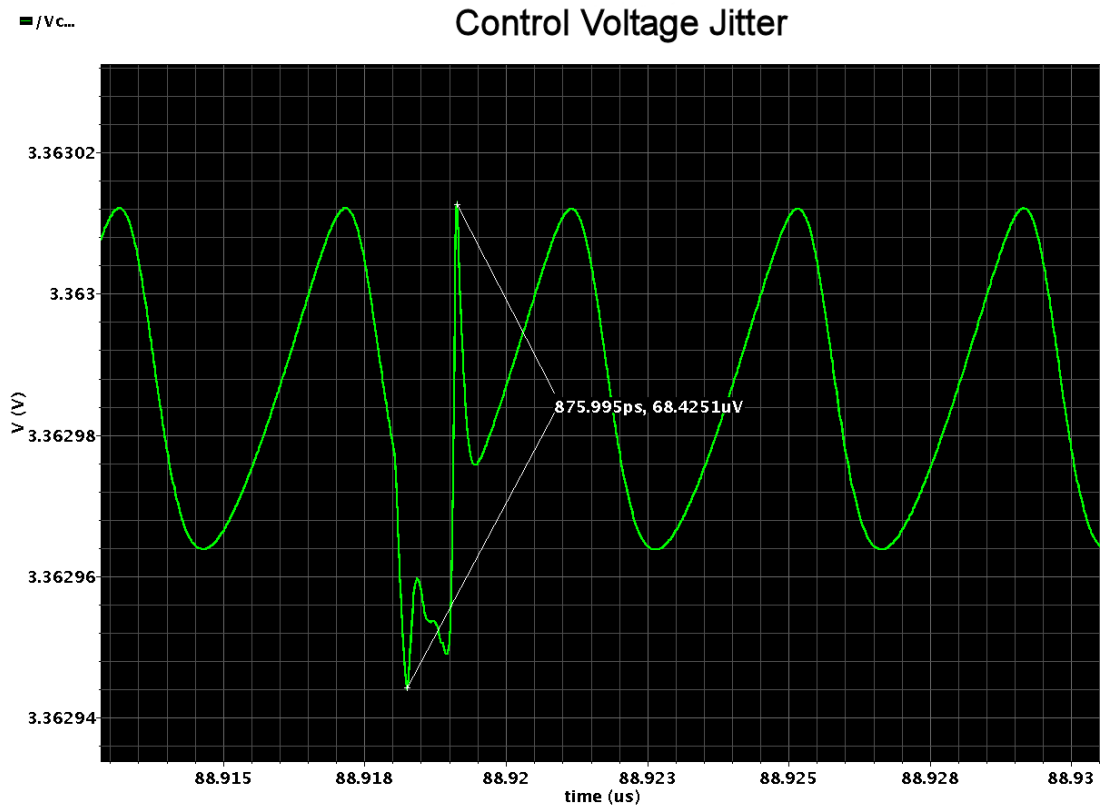


Figure 3.19: Control voltage jitter.

Reference and Feedback Clock Signals

Recall that the main function of a PLL is to align two clock signals in phase and frequency. Below is a plot of both the reference and feedback signal showing seven cycles in a locked state at nominal circuit conditions. This figure was included to provide a visual indication that the clock signals are in phase and display equal frequency.

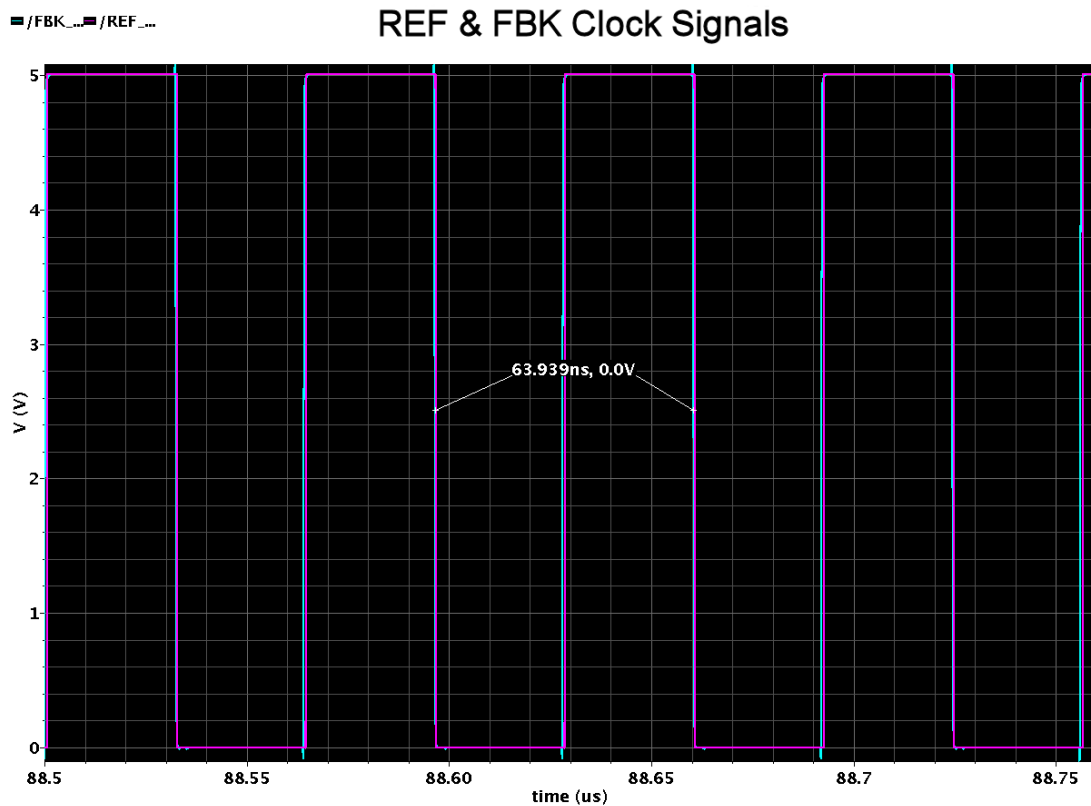


Figure 3.20: REF and FBK clock signals.

From the markers, the frequency of the FBK signal is approximately 15.6399MHz. The input reference signal was set to 15.64MHz for this simulation.

Calculated Phase Error. A zoomed image of the two clock signals is provided below in Figure 3.21 in order to demonstrate and calculate the actual amount of phase error. From the markers it is evident that, at a mid-scale voltage, the two edges differ by approximately 121ps. The relationship between the phase deviation and the time difference is:

$$\Delta\Phi = \frac{2\pi}{T} \Delta T \quad \text{rads} \quad \text{or} \quad \Delta\Phi = 360 \cdot \frac{\Delta T}{T} \quad \text{deg} \quad [3.10].$$

This corresponds to 0.012 radians or .681 degrees of phase deviation in a locked condition. This amounts to 0.19% error in the phase. This result is included for thoroughness; however, the amount of phase deviation is not specifically important in this application.

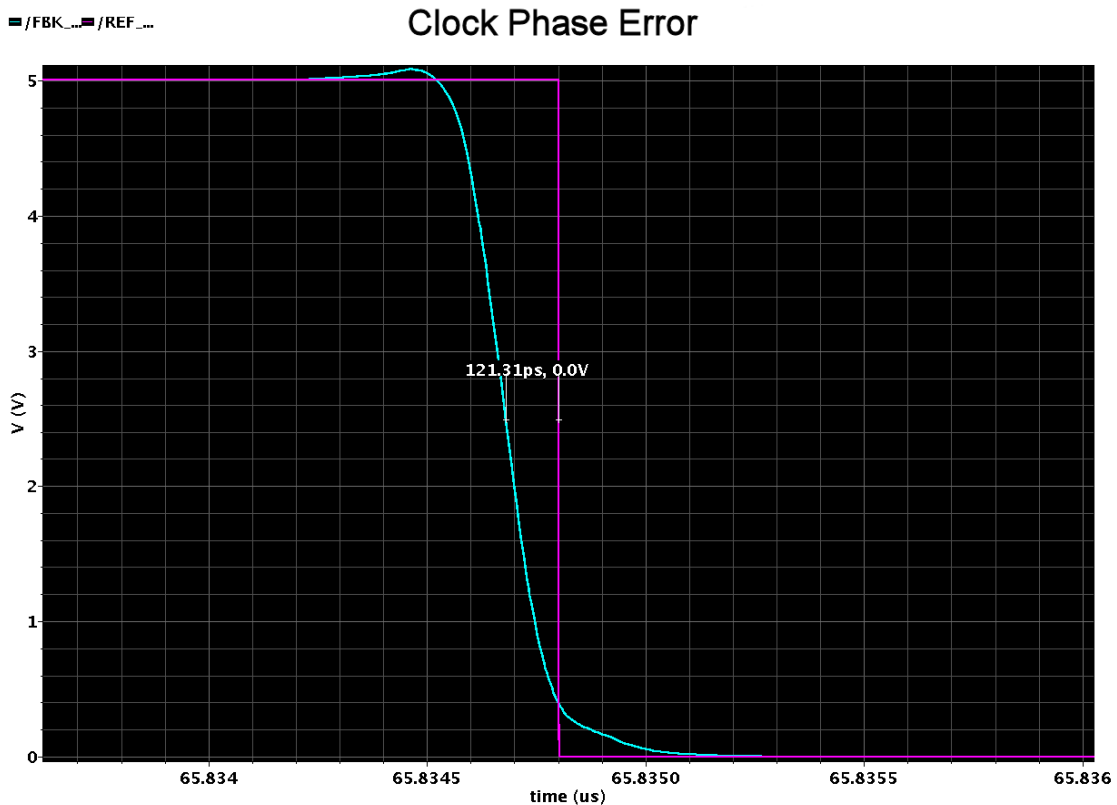


Figure 3.21: REF and CLK signals zoomed in to depict the amount of phase deviation.

Ability to Sufficiently Tune Over Transistor Process Corners.

All transistor process corners were run in order to confirm that the PLL does tune V_{cont} to a bias voltage allowing the AI to remain unconditionally stable, exhibit high quality and assume the desired inductance. The plots for each functional transistor corner are displayed in Figures 3.22-3.24.

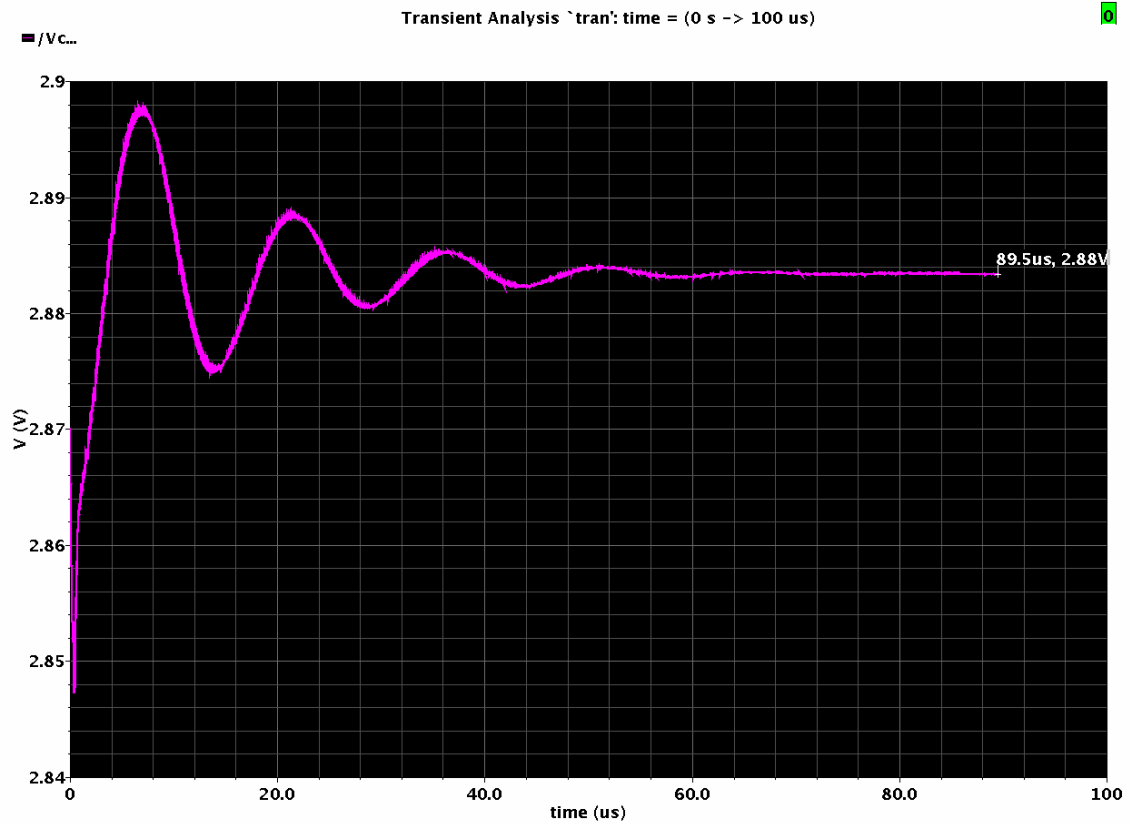


Figure 3.22: Control voltage locked at 2.88V under worst-case speed transistor parameters.

Under worst case speed transistor conditions (slow nmos and slow pmos) the control voltage locks to 2.88V. This corresponds to a 46.3nH inductance and a Q of 334.

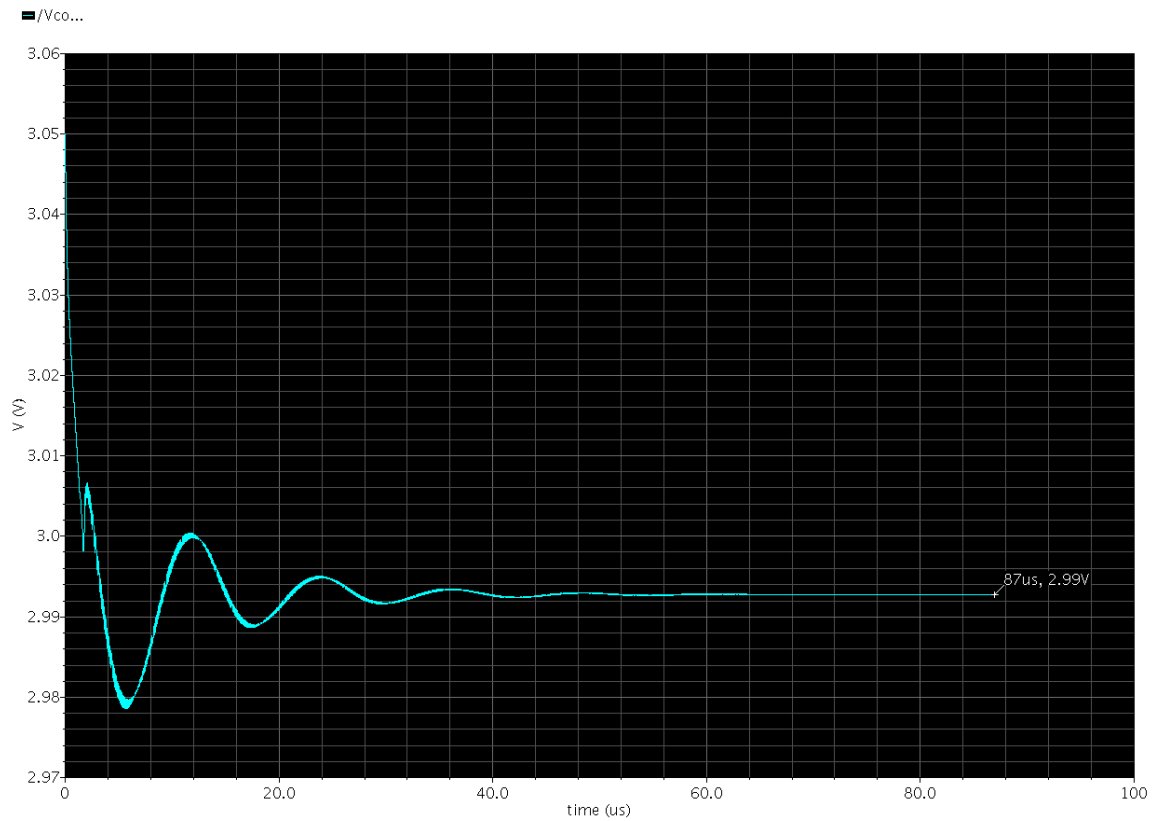


Figure 3.23: Control voltage locked at 2.99 V under worst-case zero transistor parameters.

Under worst case zero transistor conditions (slow nmos and fast pmos) the control voltage locks to 2.99V. This corresponds to a 44.6 inductance and a Q of 84.7.

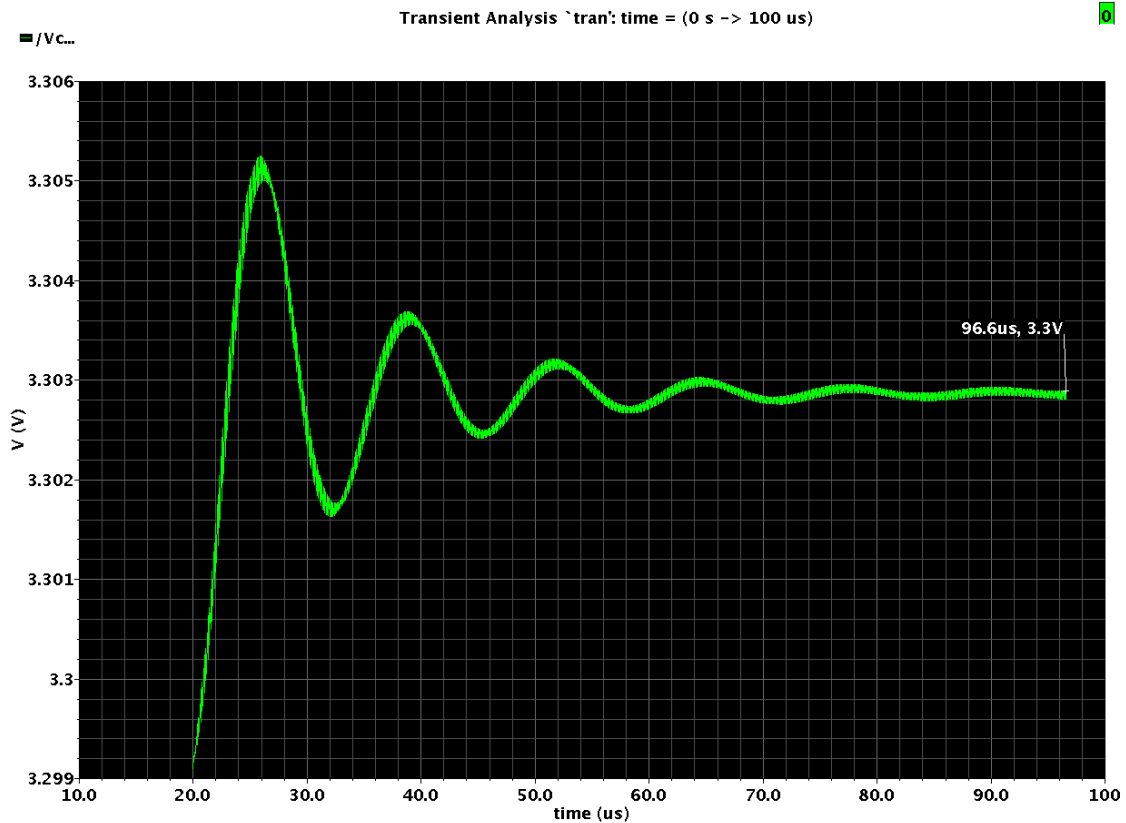


Figure 3.24: Control voltage locked at 3.303 V under worst-case one transistor parameters.

Under worst case one transistor conditions (fast nmos and slow pmos) the control voltage locks to 3.303V. This corresponds to a 43.76 inductance and a Q of 250.

Worst Case Power Explanation. The worst case power corner is not functional with this particular master-slave setup. The locked bias voltage, acquired by the PLL, produces an inductance that varies far too much to be useful in a Wilkinson power divider application. At this transistor corner, while forcing the bias voltage simulated in an AC environment to produce the 45nH inductance, the output frequency of the VCO significantly deviates from the desired output frequency of 250MHz. Consistently, the output frequency of the VCO at this corner overshoots 250MHz by around 10%.

not affect the Colpitt's output frequency. However, a quick sweep of I_{bias} in Figure 3.25 resulted in significant changes in the output frequency. For example, sweeping I_{bias} from $190\mu\text{A}$ to $210\mu\text{A}$ resulted in a reduction of the output frequency from 238.2MHz to 236.8MHz . This result suggests some dependency on the bias or transconductance of this device. However, when the transconductance was swept in a similar fashion in the transfer function representation of the VCO, no variation of output frequency is predicted. The resulting plot is provided below.

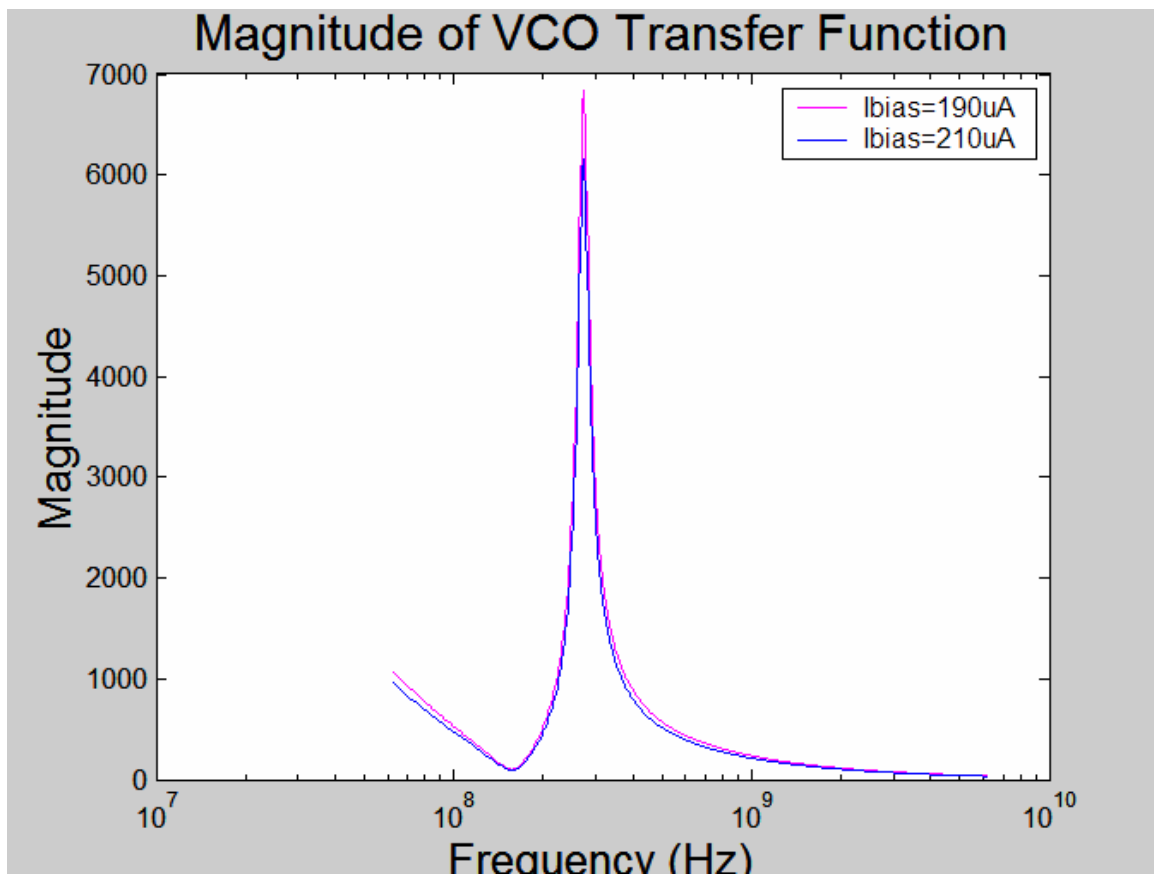


Figure 3.26: Magnitude of the VCO transfer function versus I_{bias} .

Because the circuit oscillates at the frequency where the closed-loop transfer function peaks [9], the resulting plot demonstrates that the predicted output frequency will not vary with biasing.

Another evident suspicion is that the output frequency deviation may be due to the parasitic capacitance which adds to the capacitive feedback ratio and also varies from process corner to process corner. Modeling these parasitic capacitors in the oscillator transfer function the amount of frequency deviation was predicted.

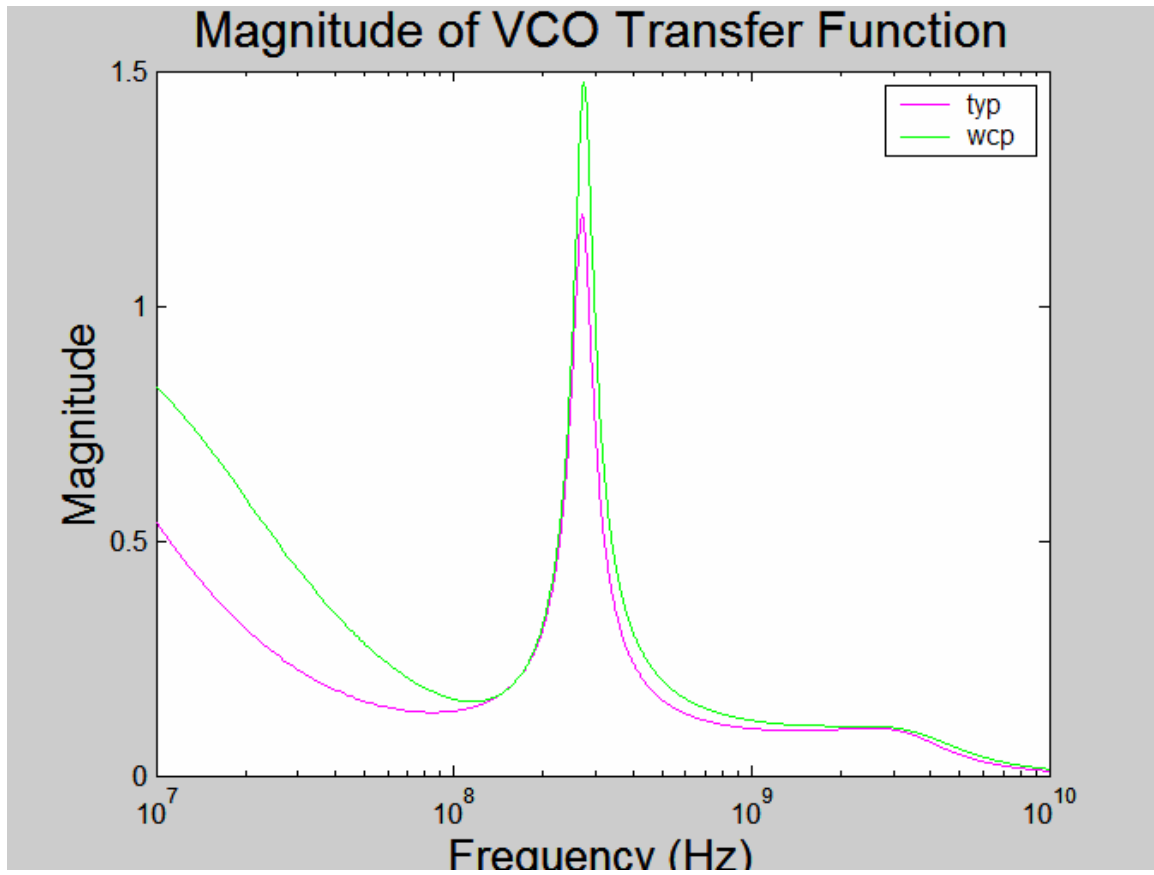


Figure 3.27: Magnitude of the VCO transfer function including the variation of parasitic capacitance experienced over the transistor process corners.

Again, from the location of each peak in the VCO's transfer function it is apparent that including the effect of the major parasitics, and their variation over process, does not predict any significant deviation in output frequency. The parasitic capacitors included in this analysis were the C_{gs} and C_{sb} of M_{osc} , C_{gs} and C_{gb} of $M1$, C_{db} and C_{gd} of $M4$ and C_{sb} of $M2$. These were the parasitics determined to add directly to $C1$, $C2$ or the

series combination of C1 and C2. The quantities used for each of these capacitances were obtained through a DC operating point simulation.

The final suspicion discussed here addresses the realized signal swings and transistor regions of operation within the VCO circuit. Because transistor transconductance and parasitic capacitance vary with the region of operation experienced by the transistor this phenomena potentially could alter the output frequency of the VCO by skewing both the inductance parameters (g_{mM1} , g_{mM2} , g_{mM3} or C_{gsM2}) and the parasitic capacitances by a significant amount. It is understood that when the gate-to-source voltage of a transistor is near the vicinity of the transistor's threshold voltage, or is in between strong inversion and depletion, the transistor's g_m increases and gate capacitance decreases [20]. This can potentially occur with the experienced signal swings realized around the VCO even when the DC bias points are determined acceptable. The combination of these phenomena work in agreement resulting in variation of the VCO output frequency.

Therefore, with this gained insight, taking into account the effect of signal swing at the different nodes of the AI would be considered in the first pass design of the AI. Choosing a suitable bias current I_1 allowing for adequate voltage swing at the gate of M1 would avoid the possibility of operating between strong inversion and depletion at the input of the AI. The same argument is true for transistor M5 of the VCO.

Realized SCAI

The actual AI that was designed and tuned is shown in Figure 3.28. The added circuitry (transistor M5) provides the utility of biasing M3 in saturation over the

loop filter's corner frequency is required to be set to a frequency much less than the unity gain frequency of the PLL in order to add phase. The LPF, on the input to the comparator obligates a corner frequency much less than the VCO output frequency. Also, the maximum resistance corner was run with the typical transistor corner to confirm that the PLL remains stable. Increasing the loop filter's resistance can cause the system to become unstable [9]. If tight control over the resistances was imperative to the specific application, variable resistors could be employed in this design.

It is acknowledged that the capacitor process corners would change the output frequency of the VCO by the relationship of equation 3.3 causing V_{cont} to lock to a different bias voltage. Thus, a simple binary-weighted capacitor network or a varactor diode configuration would be required within the framework of such a project. Reverse bias pn junction diodes are commonly used as tuning varactors in various applications. The defining equation for the capacitance of a reverse biased pn junction is [9]:

$$C_{var} = \frac{C_0}{\left(1 + \frac{V_R}{\phi_B}\right)^m} C_{var} \quad [3.11].$$

Therefore, controlling V_R one can vary the capacitance to the desired capacitance.

Conclusion

The simulated results presented in this chapter suggest that the PLL tuning technique is effective at providing the necessary bias voltage to tune the AI over transistor corners. The AI was verified by simulation to be reliable and high-performing if included on chip with the added tuning circuitry. Chapter four discusses the design of

a lumped Wilkinson power divider circuit employing a tuned AI in an arrangement similar to the master-slave. This discussion is followed up with simulated results verifying the functionality of the Wilkinson device in both power dividing and combining scenarios.

CHAPTER FOUR

SIMULATED LUMPED WILKINSON POWER DIVIDER

Introduction to Topology and Theory of Operation

In the discipline of power dividing and combining, the Wilkinson power divider is a well-known and commonly used topology. A key advantage of the ideal Wilkinson divider topology is that it realizes an impedance match at all ports while simultaneously exhibiting isolation between the two output ports and lossless behavior from the perspective of the input port. The operational details of the Wilkinson were presented in Chapter one. This chapter first presents the transformation from a distributed Wilkinson to a lumped equivalent capacitor-inductor-capacitor (CLC) Wilkinson and then the simulated results of the Wilkinson power divider designed for this thesis work. A discussion focused on the effectiveness of the overall topology and design trade offs that were determined concludes the chapter.

Translating From the Distributed
Wilkinson to the Lumped Wilkinson Equivalent

Usually, to minimize the size, a distributed Wilkinson divider employs $1/4\lambda$ transmission lines. However, because this corresponds to an L-C-L (inductor-capacitor-inductor) T-network in the lumped element equivalent Wilkinson, the divider is transformed to employ a C-L-C T-network to facilitate use of the grounded active inductor. This transformation is visually depicted in the figure below.

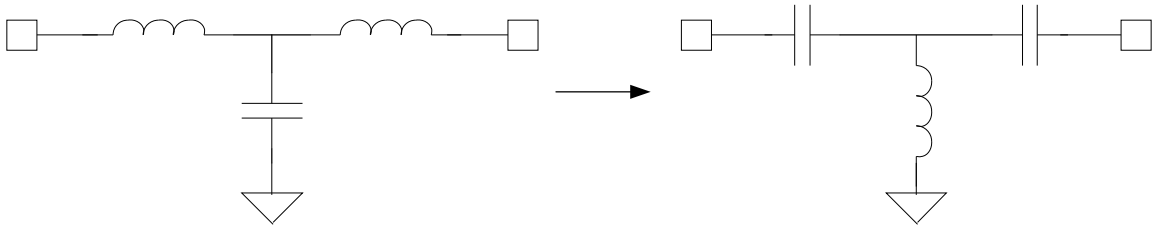


Figure 4.1: Transformation to allow the use of grounded inductors.

First, the transformation, from distributed to lumped equivalent, is derived below. The transmission, or ABCD, matrix is used to transform the distributed Wilkinson into a lumped element Wilkinson equivalent. The ABCD parameters of a length of transmission line characterized by characteristic impedance (Z_0) and the electrical length (βl) are [11]:

$$\begin{aligned} A &= \cos(\beta l) & B &= jZ_0 \sin(\beta l) \\ C &= jY_0 \sin(\beta l) & D &= \cos(\beta l) \end{aligned} \quad [4.1].$$

The characteristic impedance for the $\frac{1}{4}\lambda$ transmission line is $Z_0 = \sqrt{2} \cdot 50 = 70.7\Omega$ and

the electrical length is $\beta l = \frac{2\pi}{\lambda} \cdot \frac{\lambda}{4} = \frac{\pi}{2}$. Therefore, the ABCD parameters can be found

to be:

$$\begin{aligned} A &= 0 & B &= j70.7\Omega \\ C &= j14.14m\Omega & D &= 0 \end{aligned} \quad [4.2].$$

Once the ABCD parameters are known the T-network parameters Z_1 , Z_2 , and Z_3 can easily be calculated. A representation of a three impedance T-network is shown below in Figure 4.2.

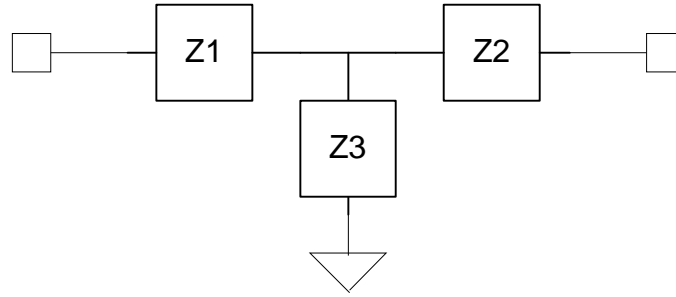


Figure 4.2: Three impedance T-network.

The equations transforming from an impedance matrix to an ABCD matrix are:

$$\begin{aligned} A &= 1 + \frac{Z_1}{Z_3} & B &= Z_1 + Z_2 + \frac{Z_1 Z_2}{Z_3} \\ C &= \frac{1}{Z_3} & D &= 1 + \frac{Z_2}{Z_3} \end{aligned} \quad [4.3].$$

Therefore, solving for Z_1 , Z_2 , and Z_3 one will obtain:

$$\begin{aligned} Z_1 &= \frac{A-1}{C} = \frac{-1}{j(0.01414)} = j70.7\Omega \\ Z_2 &= \frac{D-1}{C} = \frac{-1}{j(0.01414)} = j70.7\Omega \quad [4.4]. \\ Z_3 &= \frac{1}{C} = \frac{1}{j(0.01414)}\Omega = \frac{70.7}{j}\Omega \end{aligned}$$

As can be seen from [4.4], Z_1 and Z_2 are inductive elements and Z_3 is a capacitive element. In fact, the Wilkinson design equations 2.1 can be recognized from this

derivation. Acknowledging that $j70.7\Omega = j\sqrt{2}Z_0 = j\omega L$ and $\frac{70.7}{j}\Omega = \frac{\sqrt{2}Z_0}{j}\Omega = \frac{1}{j\omega C}$,

the L and C values in the T-network can be calculated for any given characteristic impedance and operating frequency. As presented previously, for a 250MHz operation and matching to 50Ω port impedances, it is necessary that $L = 45\text{nH}$ and $C = 9\text{pF}$.

Transforming from a LCL to a CLC T-network

Because the AI is a grounded element, in order to employ this device while maintaining matching ports, isolation and lossless transmission, $\frac{3}{4}\lambda$ transmission lines

may be employed. In this case, $\beta l = \frac{3\pi}{2}$ and the ABCD parameters become:

$$\begin{aligned} A &= 0 & B &= -j70.7\Omega \\ C &= -j14.14m\Omega & D &= 0 \end{aligned} \quad [4.5].$$

Converting to the impedance T-network in the same manner as above one finds that:

$$\begin{aligned} Z_1 &= \frac{A-1}{C} = \frac{1}{j(0.01414)} = \frac{70.7}{j}\Omega \\ Z_2 &= \frac{D-1}{C} = \frac{1}{j(0.01414)} = \frac{70.7}{j}\Omega \quad [4.6]. \\ Z_3 &= \frac{1}{C} = \frac{-1}{j(0.01414)}\Omega = j70.7\Omega \end{aligned}$$

Therefore, the inductance has been effectively moved to the grounded position, Z_3 , in the T-network, allowing the AI to be employed.

Actual Wilkinson Topology Simulated

The Wilkinson divider defining design equations introduced in Chapter one and derived above are repeated below:

$$L = \frac{\sqrt{2}Z_0}{\omega} \quad [4.7]$$

$$C = \frac{1}{\sqrt{2}\omega Z_0} \quad [4.8]$$

$$R = 2Z_0 \quad [4.9].$$

An operation frequency of 250MHz was chosen for the design presented in this thesis because it was considered that the C5 process would be capable of supporting circuit designs operating at this frequency. Therefore, the implemented values were determined to be $L = 45\text{nH}$, $C = 9\text{pF}$ and $R = 100\Omega$. The simulated Wilkinson circuit is displayed in Figure 4.3 below.

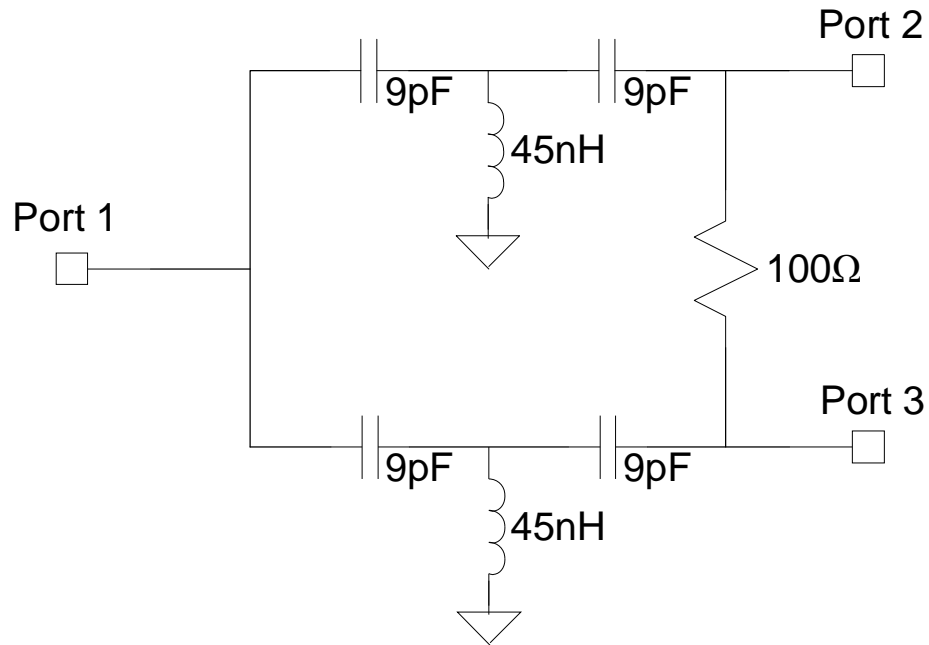


Figure 4.3: Designed and simulated Wilkinson power divider.

Stability Analysis

When employing active gain elements into any circuit stability must be guaranteed. A simple analysis was carried out to determine the transfer function of the lumped Wilkinson divider. The Wilkinson transfer function was found to be:

$$H(s) = \frac{sR}{sR + \frac{1}{C_1}} \cdot \frac{s^2RL + s\left(\frac{L}{C_1} - R_L R\right) - \frac{R_L}{C_1}}{s^2L + s(R - R_L) + \frac{2}{C_1}} \quad [4.10].$$

With the Wilkinson transfer function derived it is trivial to solve for the system's three poles:

$$poles : s = -\frac{1}{RC_1}; \quad s = \frac{-(R_L + R) \pm \sqrt{(R + R_L)^2 - 4\left(\frac{2}{C_1}\right)(L)}}{2L} \quad [4.11].$$

The condition where a right hand plane pole, or instability, occurs is when a positive real part of the complex conjugate pole pair location results, or when:

$$R_L > -R \quad [4.12].$$

This stability analysis has specifically assumed that the output impedance of the Wilkinson is matched to a 50Ω load. For microwave applications involving loads other than 50 ohms a source and load stability circle analysis would be required. Below is a plot demonstrating the S parameters of an unstable Wilkinson divider. An R_L of -75Ω was used to generate the results in Figure 4.4.

Notice, from the figure, that the reflection coefficients at all ports (S11 and S33 shown) significantly degrades. Additionally, the transmission from port one to either port two or three is less than -6dB in comparison to its ideal power split of -3dB. This was the driving force to generate active inductors with small positive or negative series resistance.

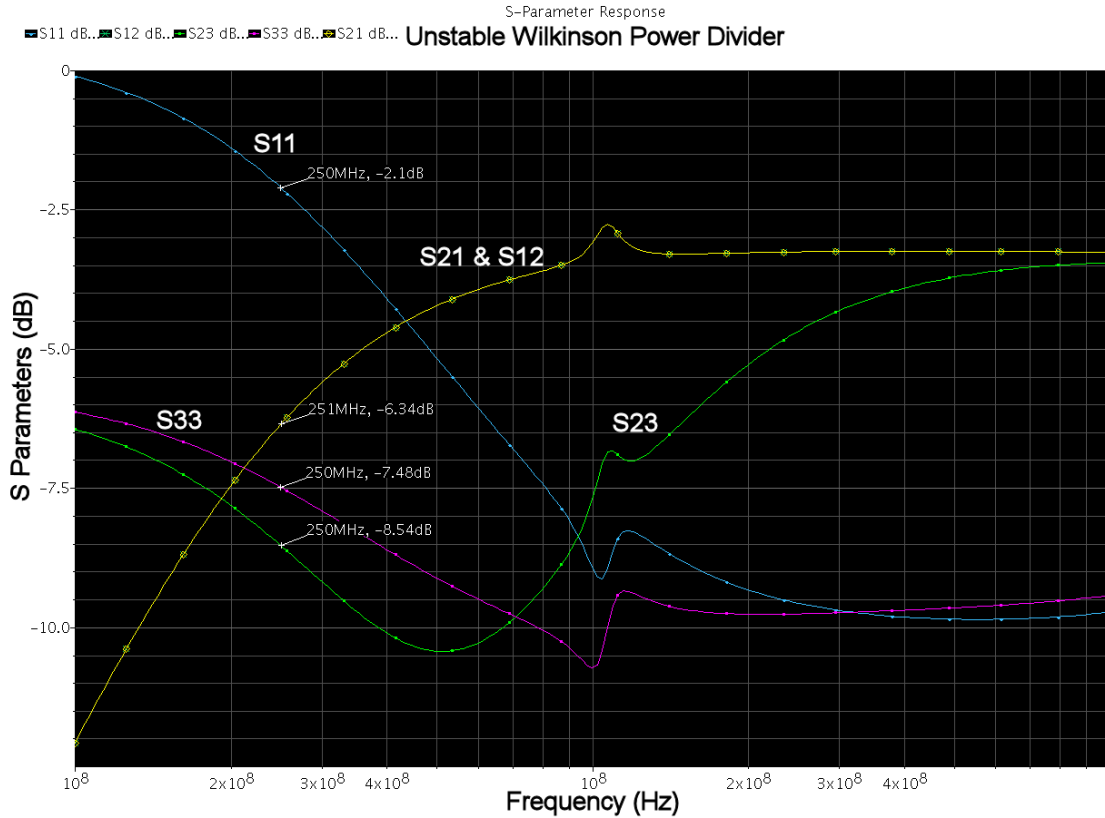


Figure 4.4: S parameter plot of an unstable Wilkinson power divider including all important quantities.

An interesting implication of employing active elements, which generate a negative resistance, as the inductor in the lumped Wilkinson is the possibility of introducing gain along the signal's propagation while maintaining matched ports and isolation between the two output ports.

Simulated Results

Due to the length of turnover time required for running large transient simulations the control voltage output of the tuning PLL is modeled as the locked DC value plus the jitter found on this node. Below, in Figure 4.5, a depiction of the entire topology is presented.

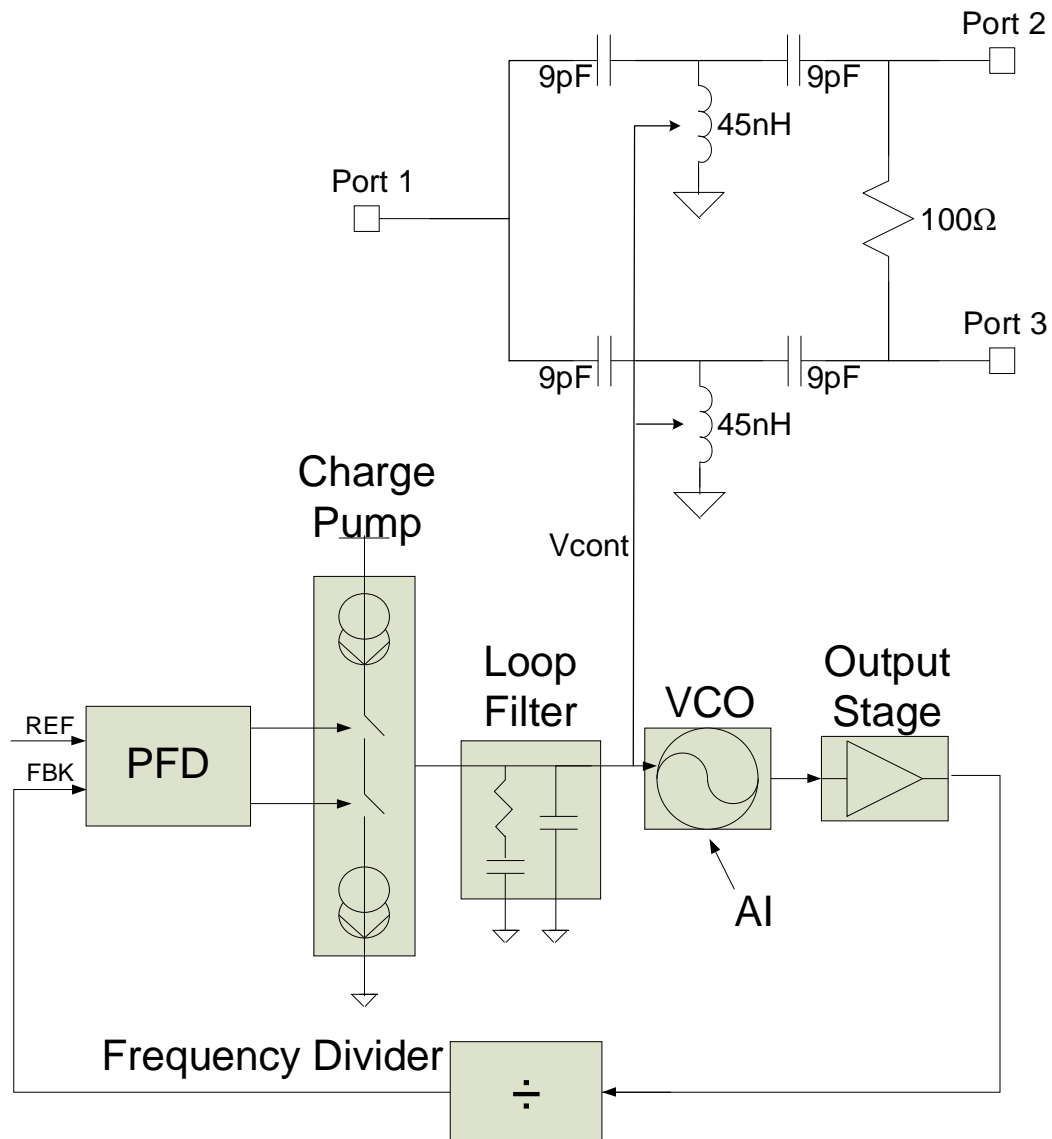


Figure 4.5: Realized Wilkinson power divider with AI tuning PLL.

Simulated S11, S21, S23, S33 Results

The results of running S parameter simulations with 50Ω matched ports and using the typical transistor corner are reported in this section pertaining to the typical process condition. Realistic hi-poly2 resistors and poly1-poly2 capacitor passives were employed for these simulations. The main figures of merit, as discussed in Chapter one, are the reflection coefficients at each port, the transmission from port one to two or from port

one to three and vice versa, and the isolation of port two and port three. Due to the Wilkinson's symmetry, in terms of port two and port three, assumptions can realistically be made about its S parameters. First, the transmission from port one to port two (S_{21}) will equal the transmission from port one to port three (S_{31}). It can be assumed that $S_{23} = S_{32}$ (the isolation from port three to two equals the isolation from port two to three). Because of symmetry, the reflection at ports two and three should be equal as well. Thus, in such cases, only one of the S parameter plots is presented.

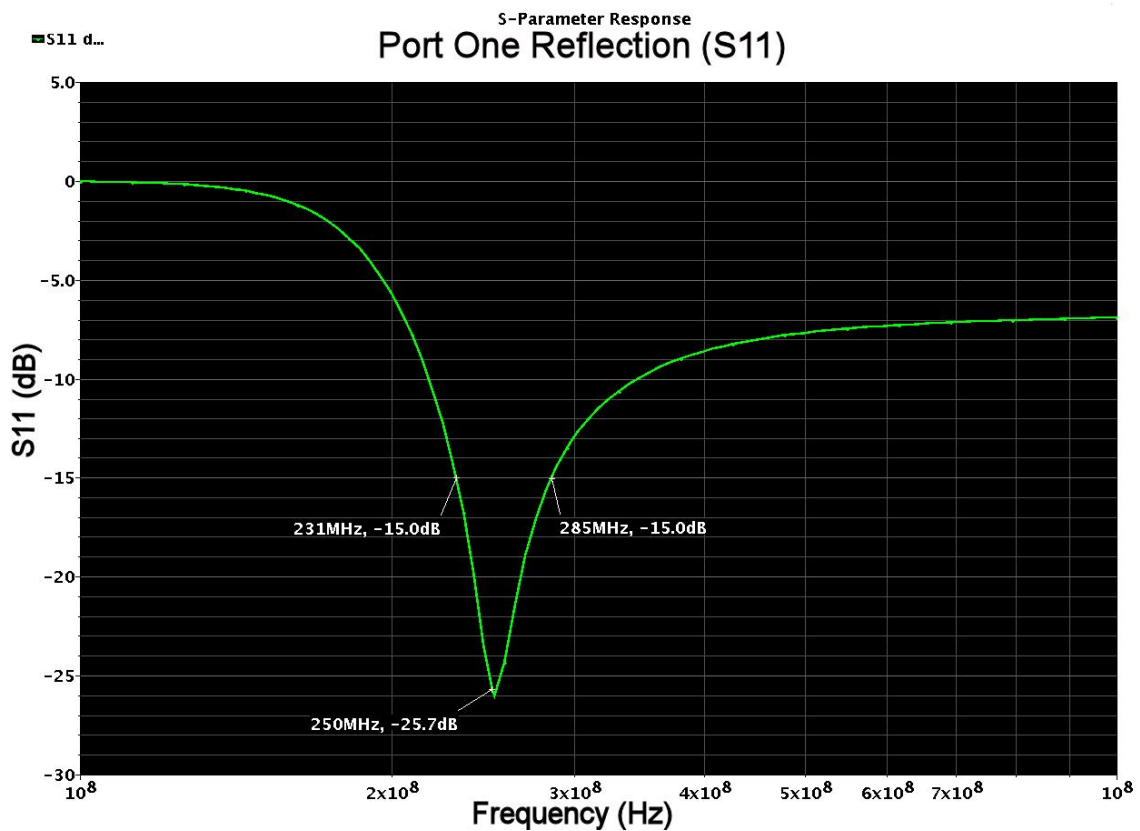


Figure 4.6: Reflection S parameter (S_{11}) for the simulated Wilkinson power divider.

The reflection coefficient (S_{11}) of port one was simulated to be -25.8dB at 250MHz. This implies that reflections are extremely suppressed at the input port of the simulated Wilkinson divider. From the markers it was calculated that the 15dB Return

loss BW is approximately 21.6%. This result is not fully consistent for $Q = 65$ as found in Figure 1.3. The inconsistencies likely stem from non idealities of the poly1-poly2 capacitors and the RLC tank-like impedance of the actual AI. However, if the deciding criteria were defined as port one reflection less than -15dB then the usable BW of the power divider is from 231MHz to 285MHz.

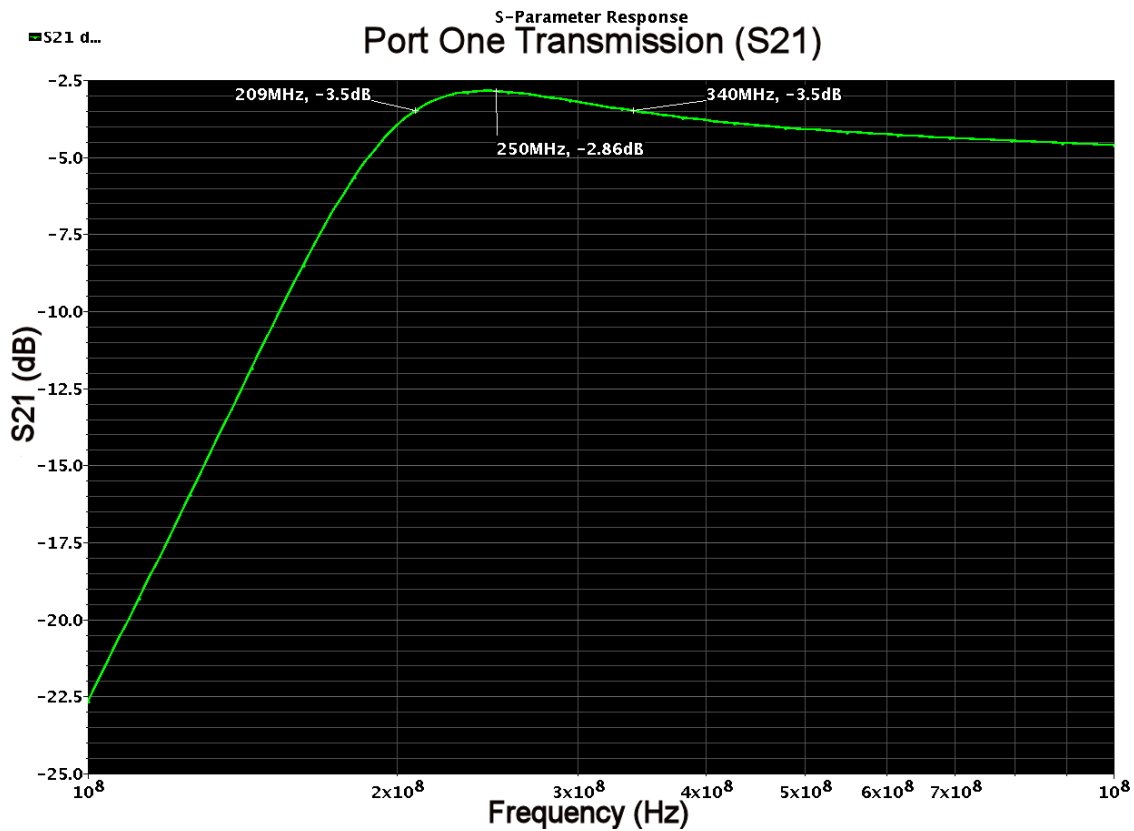


Figure 4.7: S21 parameters for the simulated Wilkinson power divider.

S21, or the transmission from port one to port two, is -2.86dB at the operating frequency of 250MHz. For an ideal lumped Wilkinson S21 is -3dB, or half power, with reference to the input signal. Again, it was assumed and verified that S31 equals S21. From the markers it is easily observed that S21 is greater than -3.5dB from 209MHz to 340MHz.

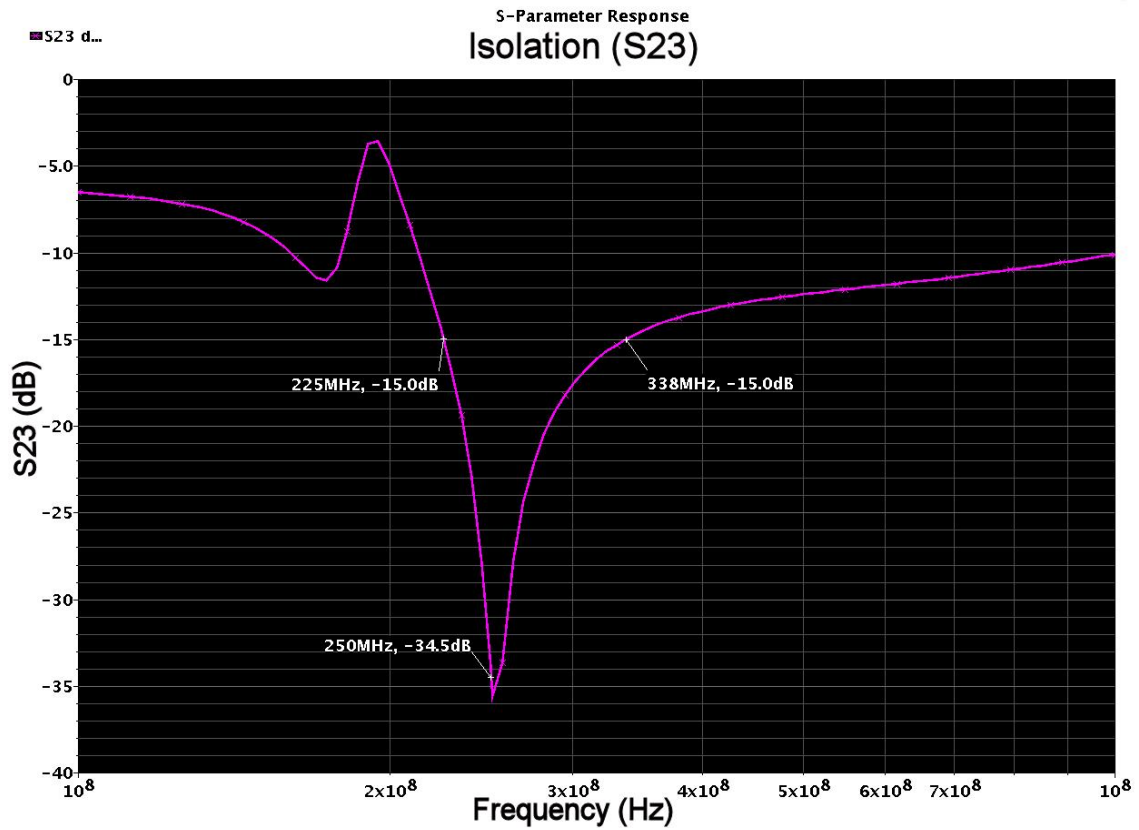


Figure 4.8: Isolation S parameter (S23) for the simulated Wilkinson power divider.

Figure 4.8 plots the isolation of port two from port three. At the design frequency, there is isolation of -34.5dB implying that the two ports are sufficiently isolated. From 225MHz to 338MHz the Wilkinson power divider simulated exhibits an isolation between ports two and three of less than -15dB.

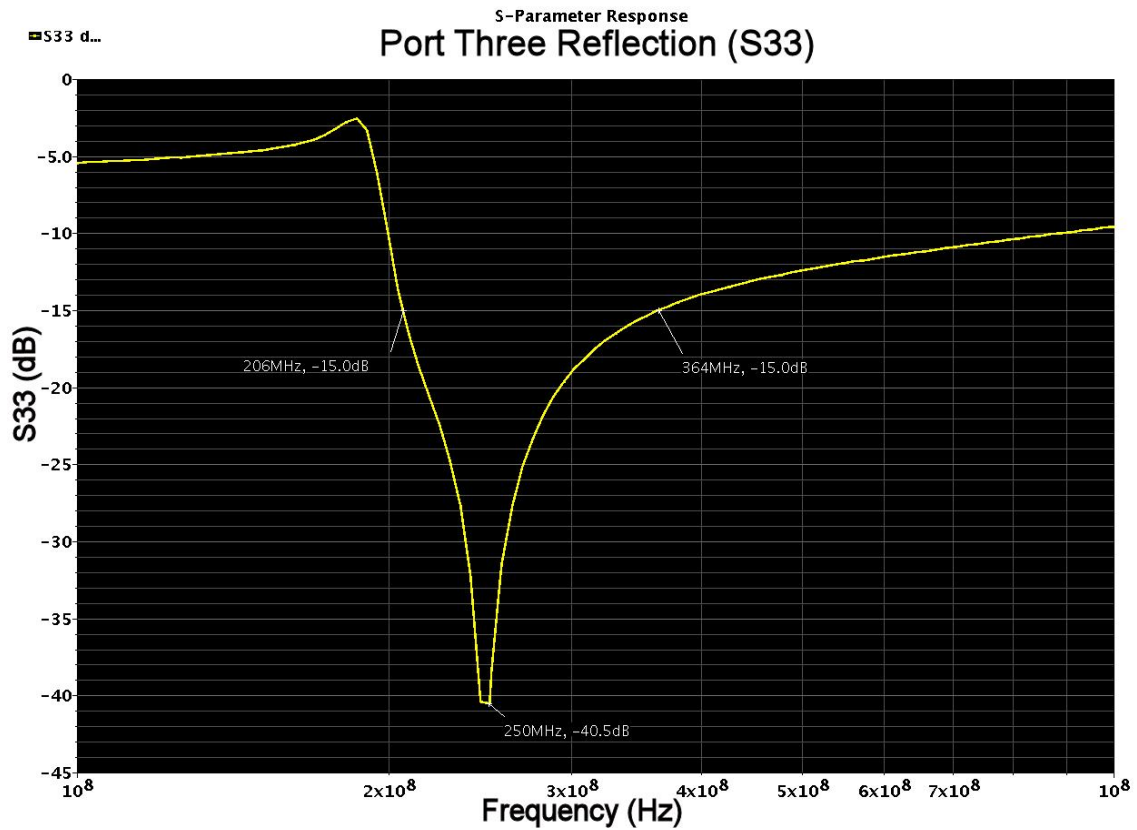


Figure 4.9: Port Three Reflection (S33) S parameter for the simulated Wilkinson power divider.

The reflection coefficient at port three is -40.5dB at the operating frequency. Therefore, reflections of signals at this port are extremely suppressed as desired. The same results were found for S22. The output port reflection is maintained less than -15dB from 206MHz to 364MHz.

Transient Simulation Results

Transient simulations were conducted to ensure that the AIs were not clipping and that the desired waveforms were being generated by the Wilkinson. The different setups tried were inputting power into port one and measuring the output at ports two and three,

inputting power signals, in phase, at port two and port three to combine at port one and inputting power, out of phase, at ports two and three for low power at port one.

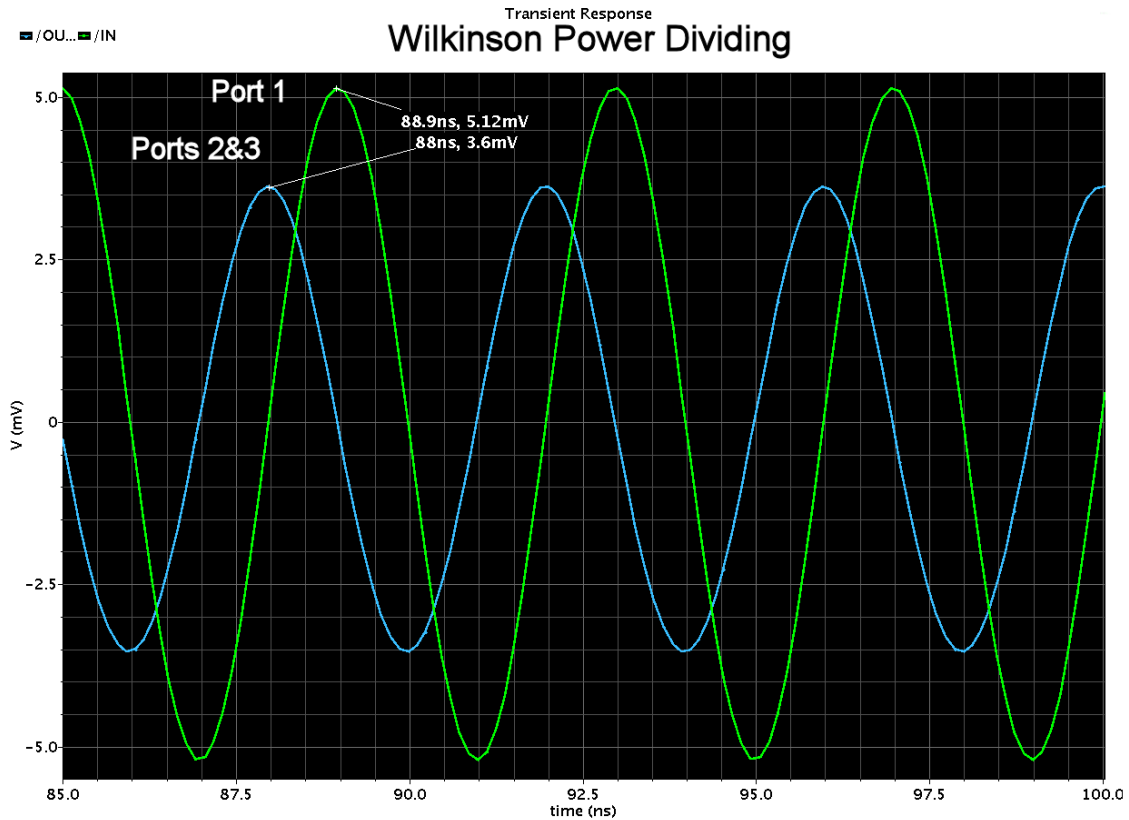


Figure 4.10: Wilkinson power dividing results in the transient domain.

Figure 4.10 depicts the situation of input power at port one splitting to port two and three equally. From the marked peaks the amount of power that translated to ports two and three relative to the input power in Watts or decibels can be determined:

$$P = 10 \log \frac{(3.6mV)^2}{(5.12mV)^2} = 10 \log(0.494) \frac{W}{W} = -3.06dB \text{ relative to the input [4.13].}$$

This transient simulation and calculation matches very closely to what was found in the S parameter simulation result plotted in Figure 4.7. The Wilkinson is approximately 98.8% efficient at dividing power under nominal conditions.

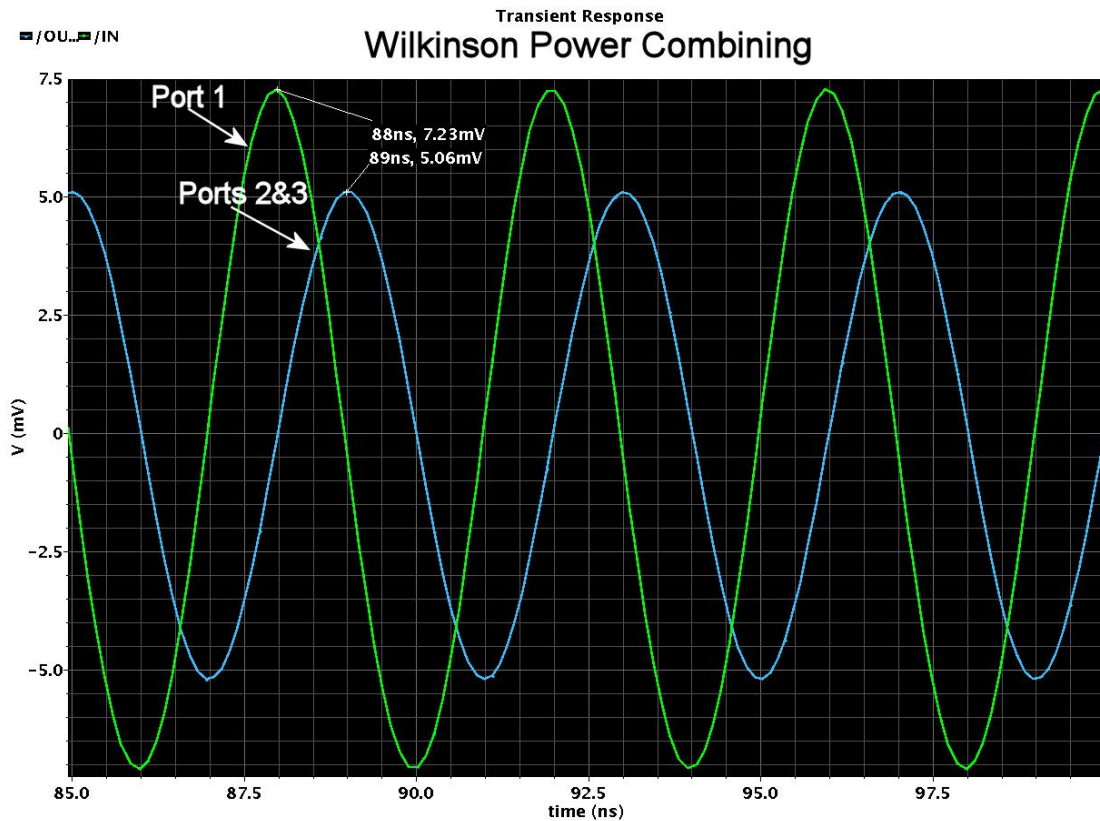


Figure 4.11: Wilkinson Power combining simulation result.

For the results depicted in Figure 4.11, ports two and three were driven by impedance matched sinusoidal sources and port one was terminated with an impedance matched 50Ω load. In the case of an ideal Wilkinson port one will demonstrate twice the power as either of the input signals. From the marked values a simple calculation can be made to determine how close to ideal the designed Wilkinson is:

$$P = 10 \log \frac{(7.23 \text{ mV})^2}{(5.06 \text{ mV})^2} = 3.1 \text{ dB} \quad [4.14].$$

The power at port one is approximately 3.1dB above both port two and three or $10^{\frac{3.1}{10}} = 2.04$ times the power of either port. With the amount of power realized at port 1 the Wilkinson is 102% efficient at combining power.

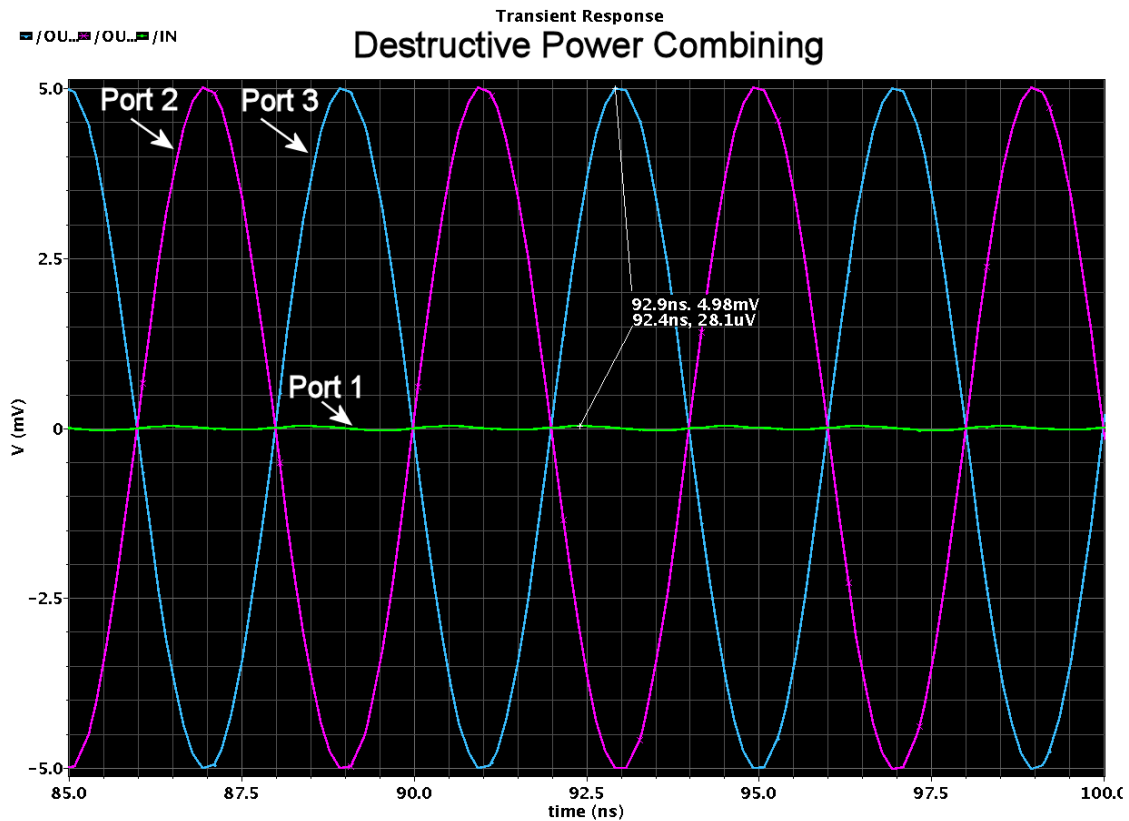


Figure 4.12 displays the results of inputting a differential signal to ports two and three and observing the output at port one. Due to the symmetric nature of the Wilkinson the two signals add destructively resulting in low output power.

Wilkinson Process Corner Analyses

Although the inductor has been tuned to approximately 45nH over the transistor process corners the capacitors will vary over the capacitor minimum and maximum corners. This causes a change in the input impedance of the Wilkinson devices. The capacitor process corners were run to demonstrate the alteration key S parameters and are compared to the typical capacitor setting.

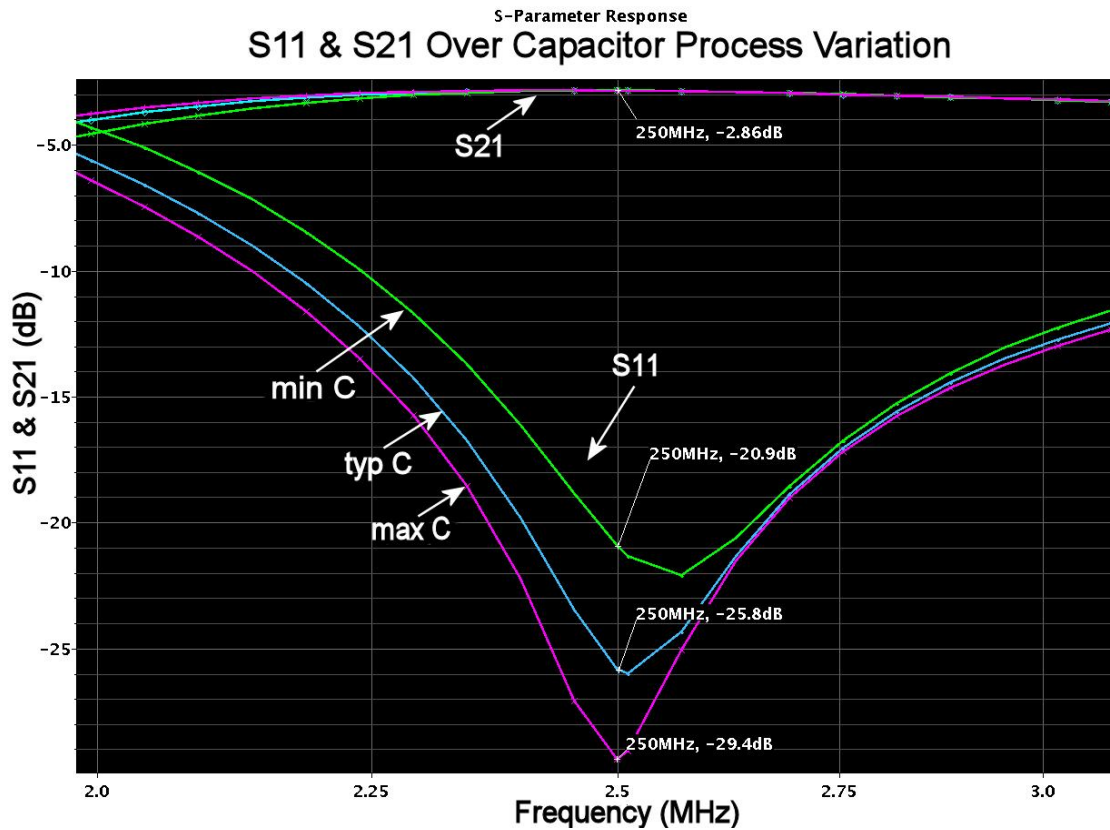


Figure 4.13: S11 and S21 over capacitor fabrication error.

It is noticeable from Figure 4.13 that the transmission of the Wilkinson is not significantly effected at the design frequency by variation in circuit capacitance. However, the reflection coefficients do vary over the process. The minimum capacitance corner results in an S11 of -20.9 dB whereas the maximum capacitance corner results in an S11 of -29.4 dB. The changes in the input impedance of the Wilkinson are expected to result in variation of performance in terms of reflection.

Below in Figure 4.14 it is again found that the minimum capacitance fabricated will produce the worst performance in terms of isolation (-24.5 dB). However, the reflection performance at port two is fairly similar over the capacitive corners. It is interesting that the typical corner does not exhibit the best performance in terms of

reflection or isolation. This suggests that, in future work, taking into account the true full impedance of the realized AI, including parasitic capacitances and series resistance, may determine the Wilkinson typical capacitor values more suitably.

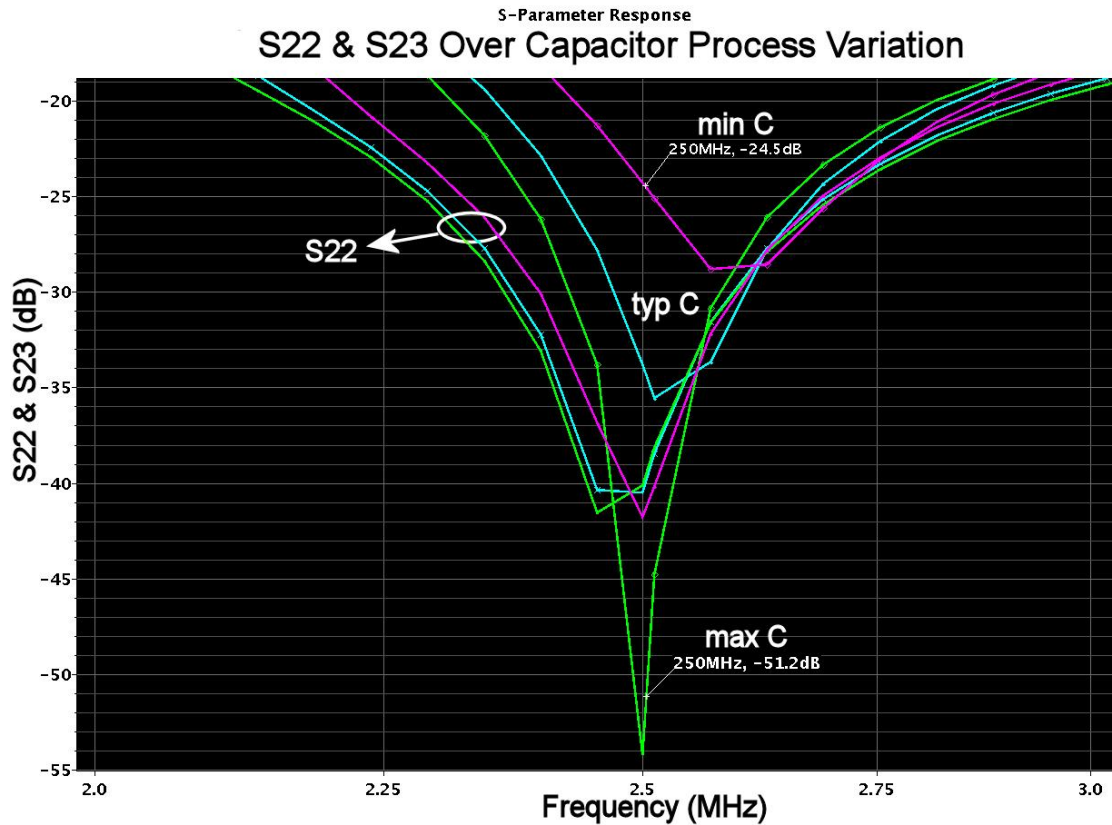


Figure 4.14: S22 and S23 over capacitor fabrication error. The three curves not indicated by the circle are the isolation curves (S23).

As mentioned in Chapter three for the VCO, a capacitor tuning arrangement would be an appealing feature to enhance the performance of the Wilkinson. Techniques that would be explored include varactor capacitors or switched capacitor arrays.

Effectiveness of the Tuning Technique

The tuning technique employed works based on the fact that actions and changes made to the active inductor in the VCO are mirrored to all active inductors used

elsewhere on chip. This type of setup is not quite “master-slave” because the reference inductor in the VCO is not used in the same manner as the inductor in the Wilkinson [16-17]. Because the VCO in the PLL and the Wilkinson power divider are not closely matched circuit tuning errors will be inevitable. For instance, over the transistor and passive process corners, fluctuation in transistor gm, parasitic and passive capacitance, transistor conductance and so on, will change the VCO operation resulting in a slightly skewed control voltage. This occurs because the PLL always works to lock the VCO at 250MHz. It is acknowledged that this effect, in combination with the skew expected in the Wilkinson capacitors, will degrade the circuit’s overall performance. Therefore, for precision control of the AI and the circuit to be employed, the reference and actual circuits need to be the same. Therefore, this tuning setup would work well for employing sinusoidal sources (VCOs) around the chip because process variation in the PLL VCO would be mirrored to the other VCOs operating on chip.

Transistor Mismatch

It is acknowledged that no two semiconductor circuits, which are intended to be identical, are ever fabricated exactly the same. Hence, it’s inevitable that both the AI tuned in the VCO will differ slightly from both of the AIs in the Wilkinson and that the two AIs employed in the power divider will also vary from one to another. The unavoidable differences, due to fabrication of the devices, are realized in the form of dimension inconsistency and threshold voltage variation. Therefore, the importance of analyzing mismatch, in the context of the AI, is the inescapable differences in transistor

transconductance. The AI topology is shown again for reference in Figure 4.15. Recall, that a transistor's transconductance is defined as:

$$gm = \sqrt{2\mu_0 C_{ox} \frac{W}{L} I_D} \quad [4.15].$$

For instance, a dimensional mismatch (i.e. ΔW) between transistor M1 of the AI employed in the VCO versus M1 of either AI employed for the Wilkinson implies that gm_{M1} will be different in all employed AIs. Because of the relationship of equation 2.10, the inductance realized in the Wilkinson will deviate slightly from the desired inductance which is tuned in the VCO. Additionally, parasitic capacitances realized in the transistors generating the AI will differ causing slight variations in inductance. Another consequence of both transistor and passive mismatches is seen in the Wilkinson power divider. Due to mismatch of the Wilkinson capacitors and between the two employed AIs, the divider will not be realized in a perfectly symmetric nature. As a result, deviation of S parameter performance is anticipated over fabrication mismatch.

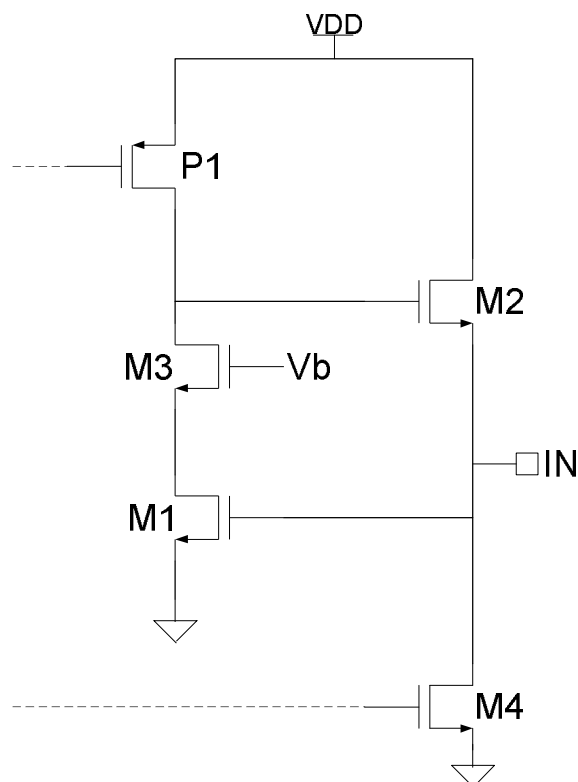


Figure 4.15: SCAI schematic.

The master-slave tuning technique cannot tune, or track, the AIs in the Wilkinson to the AI in the VCO exactly over transistor mismatch. Therefore, to ensure the reliability of employing AIs, in a master-slave fashion, monte carlo statistical mismatch analyses are required to determine the significance of all perceivable mismatch and its implications on the system's performance. Furthermore, specific layout techniques, such as employing transistors as parallel combinations of narrower devices, can be utilized to minimize these adverse effects.

Tuning Over Temperature

The master-slave topology investigated in this work theoretically does enable AI tracking over temperature variability as well. To this point, this work has assumed a

“golden” temperature of 27 degrees Celsius (C), or room temperature. Because the threshold voltage is inversely related to temperature it is understood that device transconductance will vary over temperature and will once again require some form of tuning in order to achieve a desired inductance. Previous to any implementation in industry the system would need to demonstrate functionality over the application-dependent temperature range. Typically, a temperature range of -40 to 125 degrees Celsius is used for industry applications.

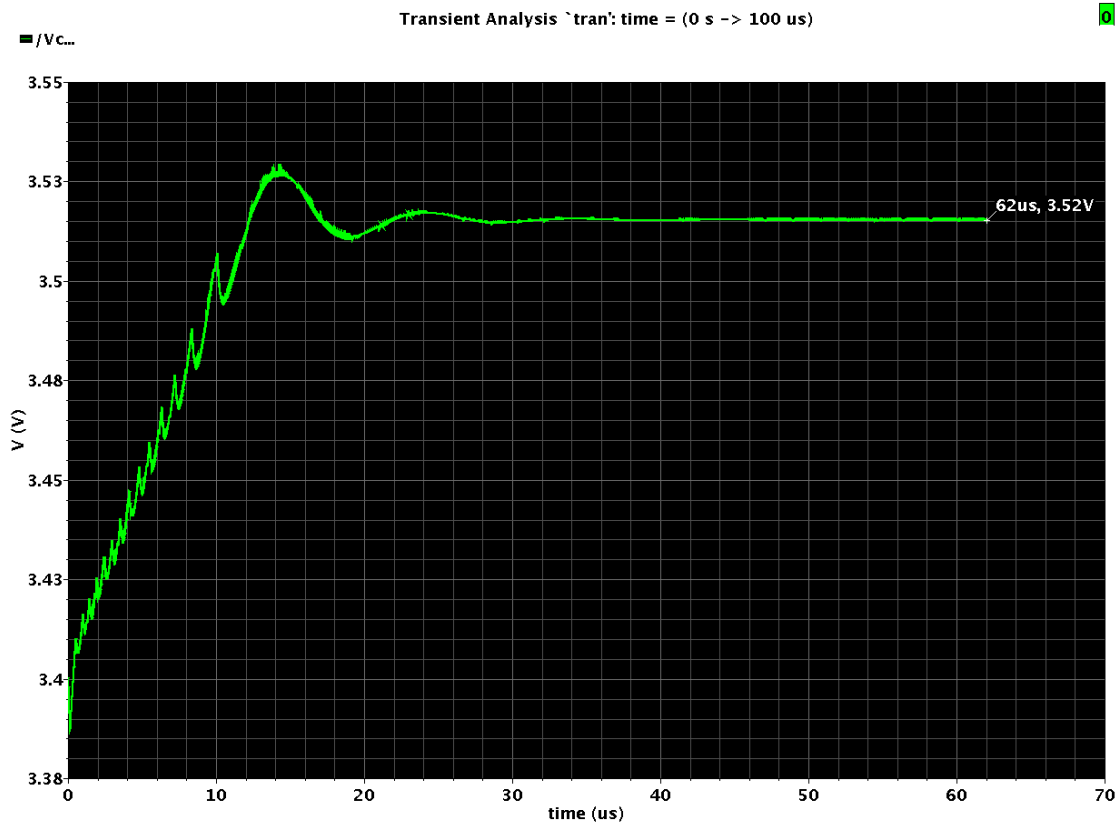


Figure 4.16: Vcont waveform locking to 3.518 volts at T=-40C.

The result of running the PLL at the -40C temperature setting is displayed above. The 45nH AI, realized under the typical transistor setting, exhibited an inductance of 85.96nH at T=125C whereas an inductance of 26.7nH at T=-40C. The control voltage

locks at 3.518V, a voltage which corresponds to an inductance of 40.4nH at $T=-40\text{C}$. The aim of this section is to demonstrate that the master-slave tuning technique will tune the AIs over temperature. The above result demonstrates that the system does in fact work to tune the inductor back to 45nH. The key element in acknowledging this functionality is that the AI tuned in the VCO is realized on chip within close proximity the AIs of the Wilkinson. Therefore, the master and slave AIs experience approximately the same temperature. Further demonstration or validation of the master-slave tuning technique employed here versus temperature variability is left for future work.

Tuning Over Voltage Variation

Industry normally requires that circuits function over a +/-10% variation in the provided voltage supplies. For this work, this constraint implies that the devices should be ensured to operate from a 4.5V to 5.5V power supply voltage. Although not included in this work it is recognized that the master-slave tuning topology employed is conducive in spite of such variation because the AI in both the master and the slave circuitry each experience the variation. Because the AI and PLL are both biased through current references it is estimated that a +/-10% voltage supply variation will not have a significant adverse affect on the overall system's performance. However, voltage variation tests would need to be run before industry implementation in order to guarantee performance.

Wilkinson With and Without Tuning

To demonstrate the actual utility of the tuning system designed a comparison of the Wilkinson at the worst case speed corner with and without tuning circuitry is

presented in this section. The key S parameter results are illustrated in Figure 4.17 and 4.18.

The simulation results are consistent with what one would expect for the worst case speed process corner. The wcs corner essentially models all transistors with a larger threshold voltage. This means that, for a given gate voltage and bias current, the transconductance of the transistor will be less than the same transistor under the same conditions and typical processing. Therefore, according to equation 2.10, the inductance is predicted larger at this corner which was the demonstrated result in Figure 2.22. Then according to equation 4.7 the operation frequency decreases. Notice in both Figure 4.17 and 4.18 that the Wilkinson without AI tuning appears to operate best in between 100MHz and 200MHz.

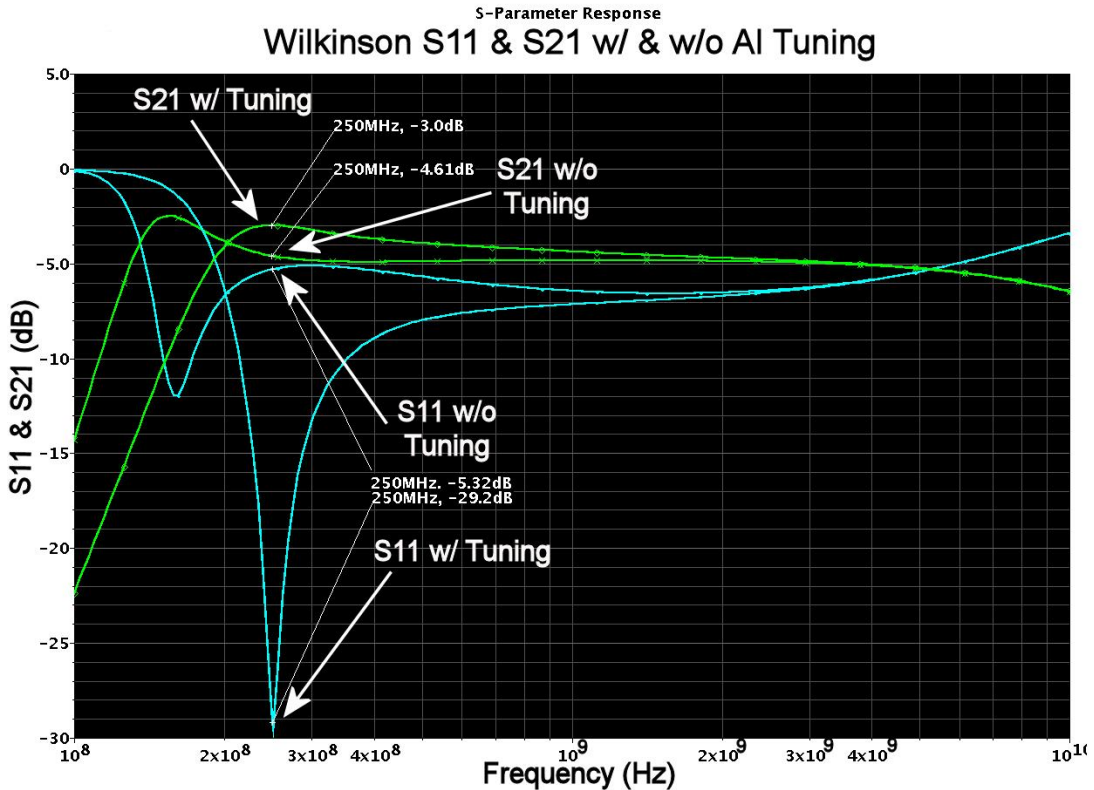


Figure 4.17: Wilkinson S11 and S21 with and without AI tuning.

From Figure 4.17 the vast improvement in terms of S11 and S21 at the operating frequency is obvious. S11, the reflection, improves from -5.32dB to -29.2dB and the transmission improves from -4.61dB to -3dB. In Figure 4.18, the reflection at port two improves from -11dB to -45.6dB. The isolation of the two output ports improves from -11.3dB to -30.8dB.

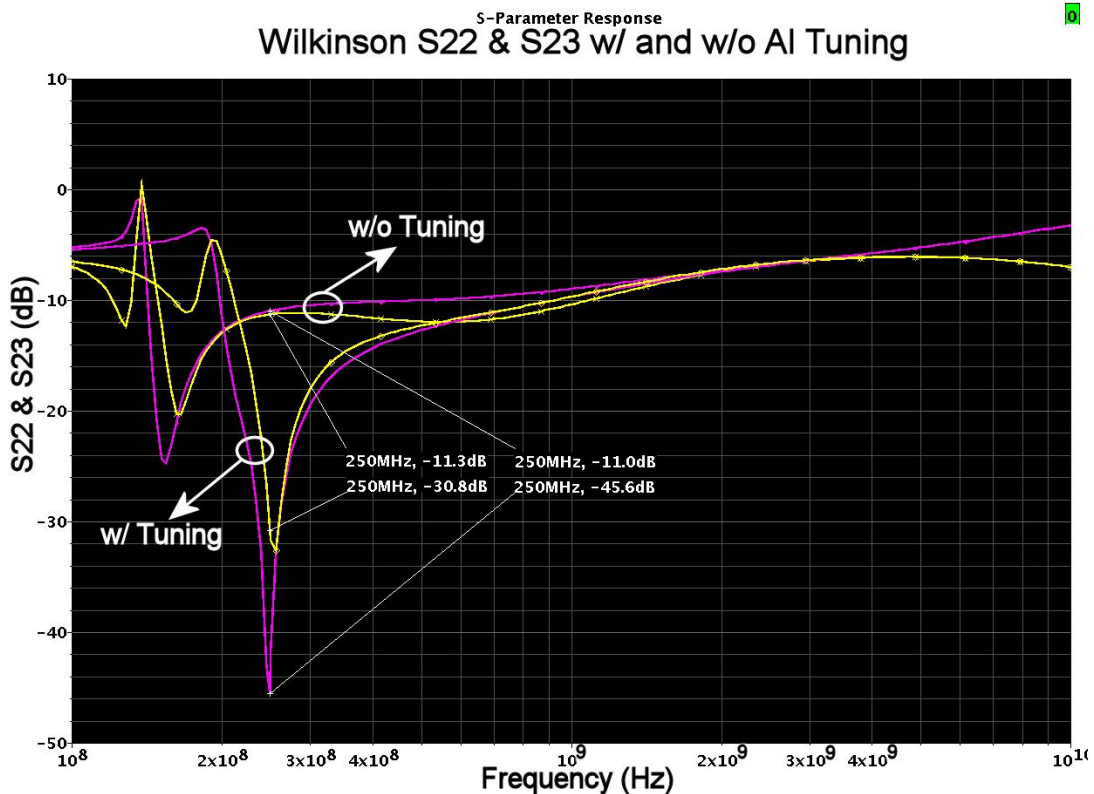


Figure 4.18: Wilkinson S22 and S23 with and without AI tuning.

Alternative Tuning Approach

An alternative topology, that would be a true master-slave, was suggested by [17]. The suggested idea is to use a sensing circuit to tune an AI used in a Wilkinson. The idea behind the proposed setup would be to drive the sensor amplifier with the input signal

and one of the output signals fed back. The sensing circuit would resolve the situation when half power was achieved at the output and therefore provide the desired bias to the AI. This type of setup would tune more precisely over process variation due to the close match between the tuning circuitry and the used Wilkinson [16-17]. Figure 4.19 depicts the setup.

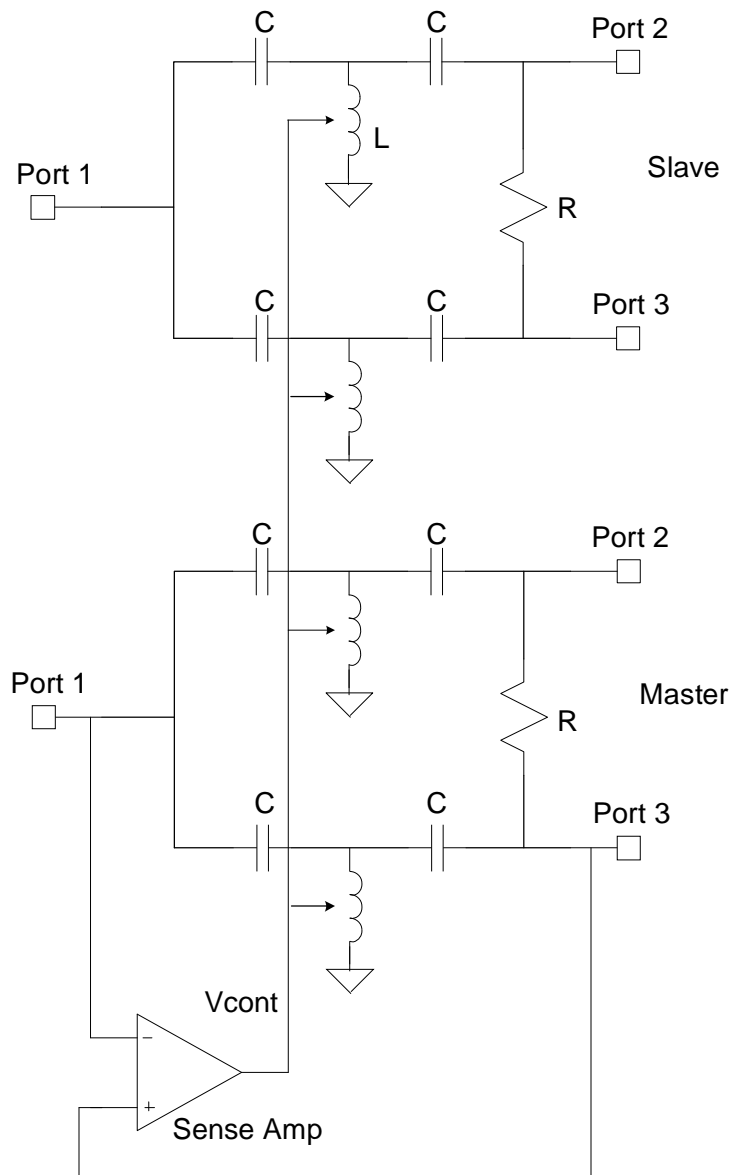


Figure 4.19: Sensor tuning circuit.

Design Tradeoffs

Although the simulation results do appear favorable for accomplishing power dividing and combining, the added complexity to tune over the transistor corners presents significant additional design effort and inherent tradeoffs.

Power Consumption

There is a sufficient amount of additional power required for biasing a single Wilkinson device with the added tuning circuitry. The tunable Wilkinson design simulated requires approximately 43.75mW of power in comparison to 18.75mW of power required for the Wilkinson not employing tuning circuitry and zero bias power consumed by that of a true lumped Wilkinson. For adding a second tuning loop roughly 68.75mW of power would be required. In other words, the amount of power required more than doubles when including the tuning circuitry. This statement of required supplementary power does not even include necessary additional tuning circuitry for passive elements.

Capacitor Tuning Technique

As described previously, the capacitors specifically employed in the Wilkinson vary over the capacitor minimum and maximum process corners. This effect was portrayed in Figures 4.13 and 4.14. Consequently, a tuning arrangement would have to be realized and implemented for the Wilkinson to be better matched. For instance, at the minimum capacitor corner, because the design frequency is constant the input impedance looking into any of the Wilkinson capacitors will increase above the desired quantity in

accordance with equation 4.8. This is very undesirable and the degraded performance of the Wilkinson in terms of its reflection and isolation was demonstrated by simulation. Again, additional augmentation is required to realize high performance and the circuit's complexity increases further.

Approximate Layout Area

The Wilkinson design with tuning circuitry was automatically generated by Cadence Layout XL to get a rough prediction of the amount of active area it would occupy. The estimated area of a chip containing a Wilkinson power divider with the tuning PLL is 93,000 square microns. In other words, a die would be approximately 300 μm by 300 μm . In addition, pads and any metal interconnects would need to be included along with any ESD protective circuitry. The amount of area consumed by a solitary 10nH spiral inductor using the same process, investigated in an earlier project [19], was 202,500 square microns, or 450 μm by 450 μm . Therefore, the added area of the tuning circuitry may not be an influential issue since the performance has been significantly enhanced.

Conclusions

Under nominal conditions the Wilkinson divider operates as expected. All relevant design parameters of the Wilkinson have been investigated and presented within this chapter. For this device to be fully automated more effort would need to be focused on designing tuning circuits for the passive elements and ensuring the devices operation

over all process corners. Suggestions for further work and project conclusions are discussed in Chapter five.

CHAPTER FIVE

CONCLUSION AND SUGGESTED FUTURE RESEARCH

Summary

An in-depth investigation of the active inductor, implemented in the AMIS C5 process, has been the primary motivator driving this research work. Comparisons to other published works, focused on AIs, have been made within this thesis. Different design topologies and strategies to realize AIs have been offered. The shortcoming of the AI, over statistical process skew, has been uncovered and the obligation to tune as an essential strategy to avoid instability, inductance variation and low quality has been stressed.

An automatic on-chip tuning system for AIs used in a 250MHz Wilkinson power divider has been designed, simulated and presented within the context of this thesis. Four of the five transistor process possibilities were confirmed and the high resistance corner, the most likely to cause instability, was verified. A design that is robust over the passive corners in an automatic fashion is not the focus of this thesis and therefore was not realized; however, the methods of including this functionality to the proposed topology were recommended and discussed within this thesis. The simulated results in both an S parameter and transient environment suggest that, with incorporated passive tuning and a successful resolution of inductor tuning at the worst case power corner, the overall Wilkinson power divider employing AIs and the PLL tuning circuit would be reliable to fabricate as a final product over predicted fabrication variation.

Scaling Down AIs

Achieving higher operating frequencies in the Wilkinson divider or other components utilizing AIs, would require a move from the 0.6 μm C5 process to a smaller channel length process. Employing AIs in scaled processes would present further challenges however. The challenges that would need to be overcome are lost headroom and signal swing and increased process variation which are inherent in small geometry processes.

Recommendations for Future Work

There are several directions that future research work following this project could be directed. First and foremost, the design of a more robust VCO, as a chief enhancement of the entire system's functionality over all transistor settings, is the most obvious possibility for future work. Incorporation of automatic passive tuning to this design would further fulfill the "hands off" classification of this design tuning strategy. However, simple manual tuning circuits of the passives would enable lab measurements to be made without demeaning the general theory behind the tuning approach developed. By no means is the exact master-slave circuit investigated in this work the optimal solution to tuning AIs, and thus other means of automatically tuning could be explored. Finally, the possibility of employing gain in a Wilkinson power divider was another interesting result of this thesis work which has not been previously discussed to the author's knowledge and offers an interesting avenue of research.

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APPENDIX A:

SCAI AND VCO TRANSFER FUNCTION DERIVATIONS

This appendix provides the derived transfer function of the SCAI and VCO circuits. The transfer characteristic was developed by writing the Kirchoff Current Law (KCL) equations of the small signal model of both circuits and using MathCAD to derive the V_{out}/I_{in} relationship. Once the transfer function was obtained it was input into Matlab in order to plot the transfer functions. In each place that the inductance was part of the VCO characteristic its actual impedance for every particular frequency was input into the overall transfer function. Due to the length of the derived VCO transfer function it is displayed on three consecutive pages. Please note that the equation of interest is the top of each set of equations.

SCAI Transfer Function

Given

$$(0 - V_{in}) \cdot g_{ds2} + (0 - V_{in}) \cdot s \cdot C_{gs1} + g_{m2} \cdot (V_x - V_{in}) + I_{in} + (V_x - V_{in}) \cdot s \cdot C_{gs2} = 0$$

$$g_{m1} \cdot V_{in} + V_x g_{ds1} + (V_x - V_{in}) \cdot s \cdot C_{gs2} + V_x s \cdot C_{db} = 0$$

$$\text{Find}(V_{in}, V_x) \rightarrow \left[\begin{array}{l} \frac{I_{in} \cdot (s \cdot C_{db} + g_{ds1} + s \cdot C_{gs2})}{s \cdot C_{db} \cdot g_{ds2} + s^2 \cdot C_{db} \cdot C_{gs1} + s \cdot C_{db} \cdot g_{m2} + s^2 \cdot C_{db} \cdot C_{gs2} + g_{ds1} \cdot g_{ds2} + g_{ds1} \cdot s \cdot C_{gs1} + g_{ds1} \cdot g_{m2}} \\ \frac{I_{in}}{[-((-s) \cdot C_{gs2} + g_{m1})] \cdot (s \cdot C_{db} \cdot g_{ds2} + s^2 \cdot C_{db} \cdot C_{gs1} + s \cdot C_{db} \cdot g_{m2} + s^2 \cdot C_{db} \cdot C_{gs2} + g_{ds1} \cdot g_{ds2} + g_{ds1} \cdot s \cdot C_{gs1} + g_{ds1} \cdot g_{m2})} \\ \frac{g_{ds1} \cdot g_{m2} + g_{ds1} \cdot s \cdot C_{gs2} + s \cdot C_{gs2} \cdot g_{ds2} + s^2 \cdot C_{gs2} \cdot C_{gs1} + g_{m1} \cdot s \cdot C_{gs2} + g_{m1} \cdot g_{m2}}{g_{ds1} \cdot g_{m2} + g_{ds1} \cdot s \cdot C_{gs2} + s \cdot C_{gs2} \cdot g_{ds2} + s^2 \cdot C_{gs2} \cdot C_{gs1} + g_{m1} \cdot s \cdot C_{gs2} + g_{m1} \cdot g_{m2}} \end{array} \right]$$

[A.1].

VCO Transfer Function

Given

$$\frac{V_g - V_l}{R_l} + V_g \cdot s \cdot C_p + (V_g - V_s) \cdot s \cdot C_1 = 0$$

$$(V_g - V_s) \cdot s \cdot C_1 - V_s \cdot s \cdot C_2 + g_m \cdot (V_g - V_s) + \left(\frac{V_{out}}{r_o} - \frac{V_s}{r_o} \right) + I_{in} = 0$$

$$\frac{V_{out}}{R} + g_m \cdot (V_g - V_s) + \frac{V_{out} - V_s}{r_o} = 0$$

$$\frac{V_g - V_l}{R_l} - \frac{V_l}{s \cdot L} = 0$$

$$\begin{aligned}
 \text{Fmd}(V_{\text{our}}, V_s, V_g, V_l) \rightarrow & \left[\begin{aligned} & \frac{\text{Im } R}{s^2 L \cdot C_p + s^2 L \cdot C_1 + g_m \cdot r_o + s \cdot C_1 \cdot r_o + s \cdot C_p \cdot R_1 + s \cdot C_1 \cdot R_1 + R \cdot s \cdot C_1 +} \\ & \left(s^2 L \cdot C_p + s^2 L \cdot C_1 + 1 + s \cdot C_p \cdot R_1 + s \cdot C_1 \cdot R_1 \right) \cdot (r_o + R) \cdot \frac{1}{s^2 L \cdot C_p + s^2 L \cdot C_1 + g_m \cdot r_o + s \cdot C_1 \cdot r_o + s \cdot C_p} \\ & \frac{\text{Im } s \cdot C_1}{s^2 L \cdot C_p + s^2 L \cdot C_1 + g_m \cdot r_o + s \cdot C_1 \cdot r_o + s \cdot C_p \cdot R_1 + s \cdot C_1 \cdot R_1 + R \cdot s \cdot C_1} \\ & \frac{\text{Im } s^2 \cdot C_1 \cdot L}{s^2 L \cdot C_p + s^2 L \cdot C_1 + g_m \cdot r_o + s \cdot C_1 \cdot r_o + s \cdot C_p \cdot R_1 + s \cdot C_1 \cdot R_1 + R \cdot s \cdot C_1} \end{aligned} \right. \\
 & \frac{g_m \cdot r_o + 1 + s^2 L \cdot C_1 + s \cdot C_1 \cdot R_1 + s^2 L \cdot C_p + s \cdot C_p \cdot R_1 + g_m \cdot r_o \cdot s^2 L \cdot C_p + g_m \cdot r_o \cdot s \cdot C_p \cdot R_1}{+ R \cdot s \cdot C_1 + 1 + s \cdot C_2 \cdot r_o + R \cdot s \cdot C_2 + s^3 C_1 \cdot r_o \cdot L \cdot C_p + s^2 C_1 \cdot r_o \cdot C_p \cdot R_1 + g_m \cdot r_o \cdot s^2 L \cdot C_p + g_m \cdot r_o \cdot s \cdot C_p \cdot R_1 + R \cdot s^3 C_1 \cdot L \cdot C_p + R \cdot s^2 C_1 \cdot C_p \cdot R_1 + R \cdot s^3 C_2 \cdot L \cdot C_p +} \\
 & \frac{\text{Im}}{r_o \cdot s \cdot L + r_o \cdot R_1 + R \cdot s \cdot L + R \cdot R_1} \\
 & \frac{r_o + s \cdot C_p \cdot R_1 + s \cdot C_1 \cdot R_1 + R \cdot s \cdot C_1 + 1 + s \cdot C_2 \cdot r_o + R \cdot s \cdot C_2 + s^3 C_1 \cdot r_o \cdot L \cdot C_p + s^2 C_1 \cdot r_o \cdot C_p \cdot R_1 + g_m \cdot r_o \cdot s^2 L \cdot C_p + g_m \cdot r_o \cdot s \cdot C_p \cdot R_1 + R \cdot s^3 C_1 \cdot L \cdot C_p + R \cdot s^2 C_1 \cdot C_p \cdot R_1 +} \\
 & \frac{+ R \cdot s \cdot C_1 + 1 + s \cdot C_2 \cdot r_o + R \cdot s \cdot C_2 + s^3 C_1 \cdot r_o \cdot L \cdot C_p + s^2 C_1 \cdot r_o \cdot C_p \cdot R_1 + g_m \cdot r_o \cdot s^2 L \cdot C_p + g_m \cdot r_o \cdot s \cdot C_p \cdot R_1 + R \cdot s^3 C_1 \cdot L \cdot C_p + R \cdot s^2 C_1 \cdot C_p \cdot R_1 + R \cdot s^3 C_2 \cdot L \cdot C_p}{r_o + R} \\
 & \frac{R_1 + R \cdot s \cdot C_1 + 1 + s \cdot C_2 \cdot r_o + R \cdot s \cdot C_2 + s^3 C_1 \cdot r_o \cdot L \cdot C_p + s^2 C_1 \cdot r_o \cdot C_p \cdot R_1 + g_m \cdot r_o \cdot s^2 L \cdot C_p + g_m \cdot r_o \cdot s \cdot C_p \cdot R_1 + R \cdot s^3 C_1 \cdot L \cdot C_p + R \cdot s^2 C_1 \cdot C_p \cdot R_1 + R \cdot s^3 C_2 \cdot L \cdot C_p}{+ R \cdot s^3 C_2 \cdot L \cdot C_1 + R \cdot s^2 C_2 \cdot C_p \cdot R_1 + R \cdot s^2 C_2 \cdot C_1 \cdot R_1 + s^3 C_2 \cdot r_o \cdot L \cdot C_p + s^3 C_2 \cdot r_o \cdot L \cdot C_1 + s^2 C_2 \cdot r_o \cdot C_p \cdot R_1 + s^2 C_2 \cdot r_o \cdot C_1 \cdot R_1} \\
 & \frac{C_1 \cdot C_p \cdot R_1 + R \cdot s^3 C_2 \cdot L \cdot C_p + R \cdot s^3 C_2 \cdot L \cdot C_1 + R \cdot s^2 C_2 \cdot C_p \cdot R_1 + R \cdot s^2 C_2 \cdot C_1 \cdot R_1 + s^3 C_2 \cdot r_o \cdot L \cdot C_p + s^3 C_2 \cdot r_o \cdot L \cdot C_1 + s^2 C_2 \cdot r_o \cdot C_p \cdot R_1 + s^2 C_2 \cdot r_o \cdot C_1 \cdot R_1}{C_p + R \cdot s^3 C_2 \cdot L \cdot C_1 + R \cdot s^2 C_2 \cdot C_p \cdot R_1 + R \cdot s^2 C_2 \cdot C_1 \cdot R_1 + s^3 C_2 \cdot r_o \cdot L \cdot C_p + s^3 C_2 \cdot r_o \cdot L \cdot C_1 + s^2 C_2 \cdot r_o \cdot C_p \cdot R_1 + s^2 C_2 \cdot r_o \cdot C_1 \cdot R_1} \\
 & \frac{C_p + R \cdot s^3 C_2 \cdot L \cdot C_1 + R \cdot s^2 C_2 \cdot C_p \cdot R_1 + R \cdot s^2 C_2 \cdot C_1 \cdot R_1 + s^3 C_2 \cdot r_o \cdot L \cdot C_p + s^3 C_2 \cdot r_o \cdot L \cdot C_1 + s^2 C_2 \cdot r_o \cdot C_p \cdot R_1 + s^2 C_2 \cdot r_o \cdot C_1 \cdot R_1}{+ R \cdot s^3 C_2 \cdot L \cdot C_1 + R \cdot s^2 C_2 \cdot C_p \cdot R_1 + R \cdot s^2 C_2 \cdot C_1 \cdot R_1 + s^3 C_2 \cdot r_o \cdot L \cdot C_p + s^3 C_2 \cdot r_o \cdot L \cdot C_1 + s^2 C_2 \cdot r_o \cdot C_p \cdot R_1 + s^2 C_2 \cdot r_o \cdot C_1 \cdot R_1} \end{aligned}
 \end{aligned}$$

[A.2].