Development of l6-channel communication multiplexor for Hewlett Packard 2100 series computers
by Richard David Weaver

A thesis submitted to the Graduate Faculty in partial fulfillment of the requirements for the degree of
MASTER OF SCIENCE in Electrical Engineering
Montana State University

Abstract:
The subject of this thesis is the design, development and construction of a low-cost 16-channel communication multiplexor (MUX) used for interfacing from 1 to 16 teletypes, modems or other bit-serial devices to a single I/O channel on a Hewlett Packard 2100 series computer.

This thesis discusses the following items: First, reasons for the project and the problems to be solved are presented and discussed. Second, specifications of the hardware to be interfaced are presented, along with a detailed description of the specifications for the MUX. Third, the logic design used to realize the MUX is described. This section ends with a short summary of testing procedures used to verify correct operation of the logic. In the fourth section the physical and mechanical design and construction is presented. The thesis ends with an analysis and discussion of the overall performance and success of the project.

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Signature Richard D. Weaver

Date May 23, 1974

DEVELOPMENT OF A 16-CHANNEL COMMUNICATION MULTIPLEXOR FOR HEWLETT PACKARD 2100 SERIES COMPUTERS

by

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R.D.W.

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ABSTRACT

The subject of this thesis is the design, development and construction of a low-cost 16-channel communication multiplexor (MUX) used for interfacing from 1 to 16 teletypes, modems or other bit-serial devices to a single I/O channel on a Hewlett Packard 2100 series computer.

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CHAPTER I

INTRODUCTION

1.1 INTRODUCTION

This thesis describes the specifications, design and construction of a 16-Channel Communication Multiplexor. The multiplexor (MUX) provides a way of interfacing from 1 to 16 bit serial (teletype) data channels to a Hewlett Packard (HP) 2100 series computer.

This thesis is organized in chapter form as described below. Chapter one provides the introduction and reasons for the project. Chapter two explains the computer interface, multiplexor and I/O device specifications. Chapter three describes the design and testing procedures used in developing the MUX. Chapter four describes the construction techniques and problems encountered in actually building a working model. Chapter five discusses the overall effectiveness of the project upon its completion. Relative cost, performance and reliability are also discussed.

1.2 BACKGROUND AND PROJECT INTRODUCTION

This project was started when it became necessary to connect 16 teletypes to an HP 2116B computer for use with Time-Share Basic. Also, a large number of serial data input channels were needed in data

acquisition systems that were being developed. There were two possible ways to do this interfacing before the MUX was constructed and both were expensive and not very satisfactory.

The first consisted of buying one teletype interface card for each channel to be interfaced. The cost per channel was high and each channel implemented required one input-output (I/O) slot in the computer. There are only 19 I/O slots total in the 2116B computer and two are used to interface a disc drive, one is required for a clock and three more for a high speed papertape reader, high speed papertape punch and console teletype. Therefore, only 13 slots were available for user teletype channels. Also the 2116B computer cannot supply enough current to that much I/O equipment so a power supply extender (also expensive) must be installed. Therefore, to interface only 13 user channels of Basic, required having 13 interface boards, a power supply extender and using every available I/O slot.

The other alternative was to buy another entire HP 2114 computer and the HP software multiplexor. This uses only one 16 parallel-bit board which brought in the 16 teletype channels, one on each of its 16 input bits. Then by sampling at a high frequency, the waveforms coming in on each line could be reconstructed by the computer. The whole I/O process completely tied up one computer making the cost for this solution very expensive. Also four 16 bits I/O cards were required for data transfer between the 2114 I/O computer and the 2116B

processor computer.

During the development of this project, HP replaced the older 2116, 2114 and 2115 series computers with the HP2100A computer. This computer, which they are still presently selling, has only 13 I/O slots total, leaving only 7 for time-share Basic users. With this computer the need for a multiplexor for time-share users was greater than ever.

The need for a multiplexing device can now be clearly seen. What is needed is some "black box" that will connect to 16 serial data channels (teletypes) and interface to the computer through only one I/O channel. This one interface to the computer, however, must not keep the computer so completely tied up in I/O that it cannot do other operations as was one of the problems with the HP software MUX.

CHAPTER II

THE SPECIFICATIONS OF THE MULTIPLEXOR

2.1 INTERFACE SPECIFICATIONS

The first step in designing the multiplexor is defining or stating in detail the specifications of the computer interface and the I/O equipment (teletype, modem or other bit-serial device). Figure 2.1 contains a block diagram of the overall system showing computer, MUX, and I/O device interconnections.

2.2 I/O COMPUTER INTERFACE SPECIFICATIONS

The computer interface selected is a standard HP 16 bit, parallel full-duplex I/O card. This gives two independent storage registers, one for 16 data output bits (from the computer) and one for 16 data input bits (to the computer). Also a "Device Command" signal is available that can be used to tell an external device to take some action. Another line, "Device Flag" can be used by the external device to signal to the computer.

The operation of the I/O interface board can then be summarized as follows: The computer can store 16 bits of information in the data output register with an OTA or OTB instruction. The contents don't change until the computer stores another 16 bits in the register. The "Device Flag" line is pulsed (for approximately 1 μsec),

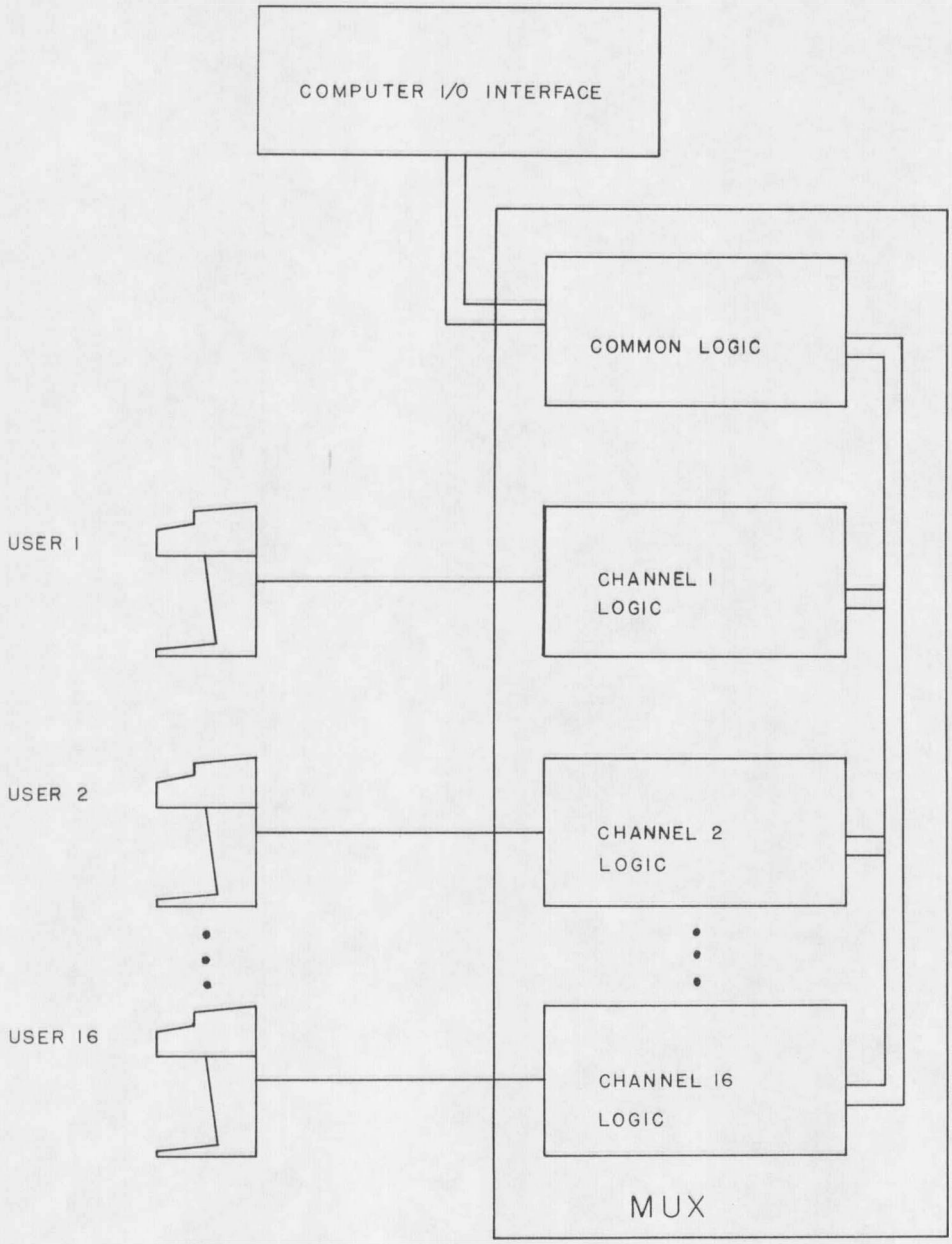


FIGURE 2.1 MUX SYSTEM BLOCK DIAGRAM

once every time a Set Control instruction is executed. Whatever data is present on the 16 data input lines coming from the external device will be loaded into the data input register when the "Device Flag" line is pulsed. This pulse also sets the I/O channel flag indicating to the computer that new data is available. The Computer can then bring in the data stored in the input register (with an LIA or LIB) and take whatever action it may desire, depending on the results of the input data word.

All signals described above are generated by standard (7400 series) TTL logic gates. This means a logic 0 = 0 to .8 volts, a logic 1 = 2 to 5 volts and voltage outside this range after transitions are undefined. The current that must be drawn from an input in the logic 0 state is 1.6 mA maximum and for a logic 1 state 10 μA must be supplied. The transition time from one logic state to the other is typically 5-50 ns. Each logic output is capable of driving at least 10 logic inputs for a fan-out of ten. The line drivers (SN7416 and SN7417) are capable of driving 20 gate inputs. The MUX was constructed using TTL logic for compatability with this computer interface.

2.3 SERIAL I/O DEVICE INTERFACE SPECIFICATIONS

At the user end of the MUX, 16 channels of serial data are to be interfaced. For each channel there is one line coming from a terminal and one going to the terminal over which the data is trans-

ferred. Figure 2.2 contains the timing diagram showing the structure of the serial data signal.

All data signals wait in the logic 1 or marking condition. When a character is to be sent, a start pulse of one bit duration is output in the logic 0 or space condition followed by the 8 information bits. The character is terminated by one or two (depending on the device) stop bits. Characters are transmitted asynchronously with the start and stop bits defining each character.

The MUX can also be interfaced directly to a modem for data transmission over telephone lines to remote users. In this case three control lines; ringing indicator, carrier detect and data terminal ready are necessary on each channel for control operations.

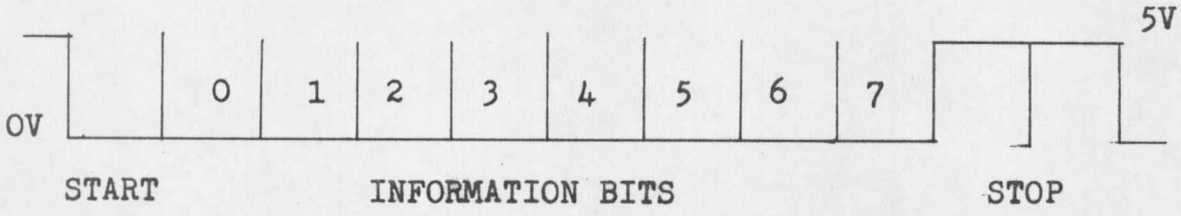
The ring indicator line is used to tell the computer when a channel is being called. The data terminal ready line is used to allow the modem to answer or once answered can terminate a call. The carrier detect tells the computer whether or not the customer has properly connected his modem for data transmission.

Therefore, for each channel two serial data lines, a ring indicator line, carrier detect line and data terminal ready are required.

Modems and many bit-serial I/O devices operate using EIA RS232 signal levels. These logic levels require a logic 1 to be in the range of +3V to +25V and a logic 0 to be in the range of -3V to -25V although 0V to -25V is often used for a logic 0. The TTL levels are

SERIAL DATA FORMAT

(GROUND TRUE TTL SIGNAL)



STANDARD BIT TIMES

110 BAUD-9.09 ms/BIT

300 BAUD-3.33 ms/BIT

FIGURE 2.2

also widely used so both signal types (EIA and TTL) are made available.

2.4 MULTIPLEXOR SPECIFICATIONS

The specification of the MUX can now proceed and must mesh effectively with the operation of the computer interface board and the data terminals and modems. The first step will define the meanings and operations associated with the 16 bit computer output word. Then the 16 bit computer data input word supplied by the MUX must be defined.

It is in these specifications that the overall efficiency of the MUX will be determined. If they are awkward the MUX will be hard to program and the computer will spend large amounts of time processing I/O. Remember the design is to be used with only one computer and 16 users all running time-share Basic and the time devoted to executing programs must be maximized. Also inefficient specifications can lead to more complex logic realizations for a given job and hence the overall product will cost more than necessary.

2.5 THE DATA OUTPUT WORD

The first step in the MUX specification is defining the computer output word. By outputting a series of these words the computer controls the entire operation of the MUX.

In Figure 2.3 it can be seen that all necessary data and information can be supplied to one MUX channel in one computer step of loading the output register of the I/O card. The "Device Command" signal is then pulsed to tell the MUX that the data is correct and can be accepted. Now from a programming point of view, the operation of outputting information to the MUX is a three-step process. First, the 16 bit data word is assembled in the computer. Second, it is stored on the I/O register card where the signals are actually transferred to the MUX. Then the Set Control instruction is executed which pulses "Device Command" causing the MUX to accept the new data.

2.6 "MODE" CONTROL

There are two types of output to a channel as illustrated in Figure 2.3. The first type sets up the "Mode" of the channel and is determined by bit 15 = 1 and bit 0 = 0.

Bits 8 through 11 determine the channel address in the following manner. If all four bits = 0 then channel 1 is accessed. Then by counting up in binary, each channel is selected in turn, according to its binary representation. With four bits, $2^4 = 16$ combinations are possible, which is the required number. As an example, an output of 0110 for bits 11 through 8 would select channel 7.

When setting the "mode", bits 1-7 are ignored by the channel. Bits 12 through 14 determine the "mode" or state of a channel and