New techniques in the analysis of homologous binal networks
by George Hampton Grenier

A thesis submitted to the Graduate Faculty in partial fulfillment of the requirements for the degree of DOCTOR OF PHILOSOPHY in Electrical Engineering
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Abstract:
Noting the general use of ever-higher frequencies in more compact equipment and at lower signal levels, as typified in missile-borne systems or resulting from the use of microelectronics, the author has considered it desirable to develop new techniques for use in the analysis of networks which are subject to interference. A singularly important subset of these is characterized by a symmetry about some reference in the physical and/or electrical sense.

Towards this end, performance criteria have been defined relating to the symmetry of these so called balanced networks and these embody a new set of balance factors involving the network's susceptibility to common-mode interference, A new list of definitions is offered in an effort to remove some of the ambiguities caused by the specialized usage of generic terms as well as applications inconsistent with presently existing professional standards. The networks under study are actually double ones and made up of two similar parts here called binary parts or biparts: the two biparts comprise the binal network or binet.

The concept of common-mode interference is enlarged to include paths of influx into all homologous node-pairs of a binet, to be driven through equivalent source impedances chosen to represent either the actual selfimpedances of an interfering wave, or variously, from worst to best case combinations of these.

An indefinite admittance matrix is used to simplify analyses of the resulting test-circuit configurations. A new method of simplifying pertinent cofactors has reduced calculations in a (2n)-node binet by a factor up to (2n-l)!/(n-1)! The simplification procedure is essentially dependent on the homology of the binet rather than its reciprocity, so is equally applicable to active networks. A new fault polynomial is proposed as an efficient mechanism to allow the choice of any order of simplifying approximation to be based on expected values of unbalance and the network parameters,, A new fault-minor expansion is offered as an alternative expression of the fault properties of the binet.

The proposed methods of analysis are particularly useful for calculating exact expressions representing the common-mode susceptibilities of large binets with relatively few unbalanced components involved at one time but with no limit to the magnitude of unbalance to be considered.

Those aspects of synthesis implicit in this approach to binets, are surveyed and objectives for future related studies are delineated.

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Electrical Engineering

Approved:

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MONTANA STATE UNIVERSITY
Bozeman, Montana

June, 1967

ACKNOWLEDGMENTS

The author wishes to thank Professor J. L. Hogin for his encouragement and helpful counsel. He is also grateful for the support provided by a National Science Foundation Fellowship.

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LIST OF SYMBOLS

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V_i	Voltage parameter	7
Z_{ij}	Impedance interconnecting terminals i and j	7
N	Number of independent nodal equations	6
J	Number of nodes	8
S	Number of separate parts in the network	8
s	The generalized frequency variable	10
E_o	Ideal voltage source parameter	11
$Z_5(s)$	Effective impedance of source, a function of the generalized frequency variables	11 a
$\mathcal{E}(s)$	Electric field intensity, a function of s	12
$\mathcal{H}(s)$	Magnetic field intensity, a function of s	12
CMRF	Common mode rejection factor (See page 94)	13
K	Voltage amplification, a ratio of voltages	13
DF	Discrimination factor	14
L	Common mode to differential mode loss; a ratio of powers	16
G	Power gain of a network; a ratio of powers	16
RC	Abbreviation for the term "resistance-capacitance"	16
DM	Abbreviation for differential mode	16
CM	Abbreviation for common mode	17
RF	Abbreviation for radio frequency	19

y_{ij}	Element of admittance matrix in $i^{\underline{th}}$ row and $j^{\underline{th}}$ column position	25
Z_{jk}^{mn}	The open circuit transfer impedance between the $jk^{\underline{th}}$ and $mn^{\underline{th}}$ port	26
V_{mn}	Voltage drop from $m^{\underline{th}}$ to $n^{\underline{th}}$ node	26
I_{jk}	Current entering node j and leaving node k	26
$Y_{kl\ldots}^{ij\ldots}$	The signed minor of the indefinite admittance matrix Y with columns i, j (etc.) and rows k, l (etc.) removed	26
N_R	The total number of resistive elements in a network	28
N_S	The total number of resistive elements in equivalent network of the source	29
A	Voltage attenuation; a ratio of voltages	31
det	Abbreviation for determinant	32
A_1, A_2, A_3, A_4	Submatrices	33
Δ_{ij}	Unbalance admittance connected across nodes i and j	35
Y '	Y matrix including unbalanced values	36
$(Y_{CR}^{CR})'$	The signed minor of Y ' with rows and columns C and R deleted	37
Y_Δ	The *leading* cofactor of the fault minor expansion, the totality of which includes *all* unbalance admittances and some of the binet's admittances	39
VCT	Abbreviation for voltage current transactor	43
y(jk/mn)	The ideal active element admittance in which current	

ABSTRACT

Noting the general use of ever-higher frequencies in more compact equipment and at lower signal levels, as typified in missile-borne systems or resulting from the use of microelectronics, the author has considered it desirable to develop new techniques for use in the analysis of networks which are subject to interference. A singularly important subset of these is characterized by a symmetry about some reference in the physical and/or electrical sense.

Towards this end, performance criteria have been defined relating to the symmetry of these so called *balanced networks* and these embody a new set of *balance factors* involving the network's susceptibility to *common-mode interference*. A *new* list of definitions is offered in an effort to remove some of the ambiguities caused by the specialized usage of generic terms as well as applications inconsistent with presently existing professional standards. The networks under study are actually double ones and made up of two similar parts here called *binary parts* or *biparts*: the two biparts comprise the *binal network* or *binet*.

The concept of common-mode interference is enlarged to include paths of influx into *all* homologous node-pairs of a binet, to be driven through equivalent source impedances chosen to represent either the actual self-impedances of an interfering wave, or variously, from worst to best case combinations of these.

An indefinite admittance matrix is used to simplify analyses of the resulting test-circuit configurations. A *new* method of simplifying pertinent cofactors has reduced calculations in a (2n)-node binet by a factor up to $(2n-1)!/(n-1)!$ The simplification procedure is essentially dependent on the homology of the binet rather than its reciprocity, so is equally applicable to active networks. A *new* fault polynomial is proposed as an efficient mechanism to allow the choice of any order of simplifying approximation to be based on expected values of unbalance and the network parameters. A *new* fault-minor expansion is offered as an alternative expression of the fault properties of the binet.

The proposed methods of analysis are particularly useful for calculating *exact* expressions representing the common-mode susceptibilities of *large* binets with relatively *few* unbalanced components involved at one time but with no limit to the *magnitude* of unbalance to be considered.

Those aspects of synthesis implicit in this approach to binets, are surveyed and objectives for future related studies are delineated.

I. A STATEMENT OF THE PROBLEM

1.0 Introduction. During the design and initial use of new electronic equipment, interference and noise in the signal or data portions of the electric circuits often cause some degradation of performance. Various government agencies, equipment manufacturers, and utility companies have published techniques for the measurement of interference in equipment and to a lesser extent the measurement of an equipment's susceptibility to the presence of such interference. Some of these are included in the literature cited in this chapter and listed at the end of the paper. It is to be expected that many of the susceptibility tests are peculiar to the specific kind of equipment under test. The first five on the list relate to a particular equipment's susceptibility to common mode (CM) interference. It is this latter kind which is of special interest here.

Interference waves entering electronic equipment may be induced by one or more of several mechanisms: Direct radiation from electric or magnetic fields, metallic conduction across common parasitic impedances such as in signal-ground networks, electromagnetic effects on control, input or output leads connected to the equipment or inadvertently, through an input transducer. The parasitic parameters involved are sometimes part of an intrasystem anamoly.

If the length of connecting wire leads is over a few feet and in an environment or at a signal level thought to require shielding in the first place, it is really not clear whether direct radiation, common coupling impedances or wire-conducted influx is more important. This particular problem is compounded by the fact that the addition of any kind of shields usually changes the ground-current configuration: so that interference in all three types of influx is simultaneously so modified. Still another complicating factor lies in the physical evidence that a degree of common-mode interference can exist across an asymmetrical (single-ended) input and indeed, may be present on more than just two conductors.

A significant part of this important problem lies in the fact that usually none of these paths of influx are readily measurable in an absolute sense. It appears to follow that for most practical configurations, conducted influx would be subject to easier measurement and that an attempt should be made to make these particular measurements more meaningful.

Suprisingly little work has been done in developing special analytical techniques for efficiently handling such problems. It is to be hoped that the concepts developed here would not only simplify the calculation of interference susceptibility, but would also lead to a new insight into the reduction of the susceptibility of networks to such kinds of interference.

1.1 THE "BALANCED" CIRCUIT

From the literature one might suspect that there are relatively few types of electrical circuits for which common mode interference has been known to be a serious problem. A singularly important catagory comes under the general heading of the "balanced" circuit.

Electronic circuits are often specially designed to be symmetrical with respect to a ground or reference terminal. In other words, one half the circuit is made to be the mirror image of the other. The literature has referred to these as balanced circuits and they are used to gain special advantages: such as those ordinarily realized in a push-pull arrangement - or to prevent interference as on low-level transducer leads or on telephone circuits. They are also used in broadcast transmission for the added reliability afforded.

Usually such configurations are easily recognizable - the term "balance" referring to like physical components symmetrically located about a center line typifying ground, or a reference terminal. Some consideration will show, however, that this particular concept of "balance" is rather limited and perhaps unrealistic in more ways than one. Clearly, each of the identical halves can be described by the same transfer function, say F(s), which can be realized by an infinitude of circuit configurations. Furthermore, due to inevitable, small, differences in the parasitic or distributed parameters involved in inter-connecting actual circuit components, as well as in-tolerance differences in the actual values of homologous components, good balance at all frequencies is often very difficult to attain. As a matter of fact, imbalance can be very large at (usually) higher frequencies so that the normal mode signal on just one side of the "balanced" circuit may be so attenuated as to approach that of the reference terminal.

On the other hand, at a particular port, an actual circuit designed to be asymmetrical or single-ended may appear to be "balanced" at one or more frequencies, because the port terminals can sustain identical voltages when driven by equivalent (effectively, low-) impedance sources. From a practical standpoint, therefore, the "balance" of a port or terminal-pair may refer to that port's ability to sustain the same voltage at discrete frequencies and with respect to two identical in-phase specified sources returned to a third reference terminal. Specifically involved of course is the common impedance of these sources compared with the values of the driving point impedances from each terminal to the reference terminal. The transfer characteristic is also subject to a similar but more involved definition of balance to be discussed later.

It is apparent that new terms are needed to distinguish between circuits so related. Longitudinal sections of network more naturally fall into the category of those portions formed by cutting off cascaded sections. On the other hand, transverse partitioning is not usually considered to be a cutting-off, but merely the result of identifying *two* parts symmetrically related to some physical line of reference. These parts will be called *binary parts* or *biparts* and the whole of such a network will be a *binal network* or a *binet*. If the network is designed to have equivalent elements symmetrically located about the reference, it will be called a *homologous binet*. If the network behaves electrically as a homologous network, this behavior will be referred to as *balance* and the network will be a *balanced binet* whether homologous or not.

Now an extremely important property of homologous binets is related to their ability to suppress or attenuate the effect of equivalent in-phase voltages applied between each terminal of any port and the chosen references:

This refers to the so-called "common mode rejection" of a circuit (See Definitions in Appendix) and is usually defined as a characteristic of a differential amplifier. When balance is considered in its broad sense, there is little reason even to limit the definition to homologous networks. (See Definitions.)

Telephone and utility people have long been aware of the problem of common mode interference on their relatively long lines (ex: Reference 1.1 a). Medical researchers making bioelectric measurements (exs: References 1.1 b, c, d) have introduced means of reducing the effects of common mode noise on the balanced input lines from their transducer instruments.

More recently, with the general use of ever higher frequencies in more compact equipment, it has been suggested that all wire-connected equipment be considered subject to possible common mode interference when installed in an unknown or otherwise questionable environment. (Reference 1.1 e)

It follows that an important insight into all such interference can be gained by the study of meaningful performance criteria related to the common-mode susceptibility of balanced circuits. An efficient means of analyzing such networks will contribute to optimum noise characteristics.

1.2 DISCUSSION AND DELINEATION

There have been substantial efforts to standardize test methods and to reduce ambiguity in the language used in describing interference problems.

(References 1.2 a - 1.2 i) Reference 1.2 a lists 102 references on the theory of grounding alone. In spite of this, it has been considered expedient to provide a list of definitions for possibly ambiguous terms used in this dissertation.

This immediately leads into a study of the various descriptors used in the analysis of homologous binets. Although R. D. Middlebrook's "Differential Amplifiers" (Reference 1.2 j) is applied largely to transistor d.c. amplifiers, the descriptors used therein and his Sequential Analysis method derived from LePage's bisection theorem (See References 1.2 k and 1.2 l) can readily be applied to most homologous binets. According to the above, practical circuits of interest in the interference problem can be subject to substantial values of imbalance. Unfortunately the Sequential Analysis method is difficult to apply when the imbalance is large.

In analyzing homologous binets, it appears that the toilsome duplication which prompted Middlebrook's initial efforts might also be obviated in the use of matrix descriptors, especially if computer time is to be saved. Then an immittance matrix can describe the balanced network configuration and the imbalance mechanisms can be represented by a *fault polynomial*. For example, assume the lumped, linear, finite passive bilateral network (LLFPB) of Figure 1.2 a illustrating any 5-terminal network, in which terminals 1 and 3 represent the input port and terminals 2 and 4 the output port with a fifth reference or ground node. It is at once clear that the (tested) network can be described by a 4th order node to datum admittance matrix since there will be a N=J-S=5-1=4 independant nodal equations. An *n* terminal network