IMPROVED CONTROL SYSTEM FOR PROCESS, VOLTAGE, AND

TEMPERATURE COMPENSATION OF CMOS ACTIVE INDUCTORS

by

Reinhold Frederick William Hollender, III

A professional paper submitted in partial fulfillment
of the requirements for the degree

of

Master of Science

in

Electrical Engineering

MONTANA STATE UNIVERSITY
Bozeman, Montana

April, 2011

APPROVAL

of a professional paper submitted by

Reinhold Frederick William Hollender, III

This professional paper has been read by each member of the professional paper committee and has been found to be satisfactory regarding content, English usage, format, citations, bibliographic style, and consistency, and is ready for submission to The Graduate School.

Dr. Jim Becker

Approved for the Department of Electrical and Computer Engineering

Dr. Robert C. Maher

Approved for The Graduate School

Dr. Carl A. Fox

STATEMENT OF PERMISSION TO USE

In presenting this professional paper in partial fulfullment of the requirements for a master's degree at Montana State University, I agree that the Library shall make it available to borrowers under rules of the Library.

If I have indicated my intention to copyright this professional paper by including a copyright notice page, copying is allowable only for scholarly purposes, consistent with "fair use" as prescribed in the U.S. Copyright Law. Requests for permission for extended quotation from or reproduction of this thesis in whole or in parts may be granted only by the copyright holder.

Reinhold Frederick William Hollender, III

April, 2011

ACKNOWLEDGEMENTS

TABLE OF CONTENTS

TABLE OF CONTENTS – CONTINUED

LIST OF TABLES

Table   Page

LIST OF FIGURES

LIST OF FIGURES – CONTINUED

ABSTRACT

Wireless communications play an increasingly large role in today's society. Today, many wireless functions are necessarily integrated into chips and other small packages to support miniaturized wireless devices such as cell phones, laptops, netbooks, etc. These Radio Frequency Integrated Circuits (RFICs) often require inductances to perform their function. Most RFICs utilize spiral inductors. Spiral inductors have their properties defined by their physical dimensions, often taking up large areas of IC real estate. There has been research into replacing these spiral inductors with active elements to reduce their size. However, these active inductors are based on parasitic elements that can vary significantly over temperature, supply voltage, and processing variations of the wafers themselves. This professional paper documents an improved control scheme to maintain correct active inductor behavior over process, voltage, and temperature variations in applications where the active inductor is used in a Wilkinson power divider.

INTRODUCTION AND PREVIOUS WORK

Introduction

Radio Frequency Integrated Circuits (RFICs) using standard CMOS processes is a very interesting area of research. CMOS processes are ubiquitous due to their use for digital and mixed-signal components. These processes are preferred over other process types, such as gallium arsenide (GaAs), due to their low cost and the possibility of integration with other mixed-signal and digital components on a single die, even though other process types, such as GaAs, may have much better RF and microwave performance. RFICs using CMOS processes must therefore be cleverly designed to overcome the lack of inherent high frequency performance as compared to other process types.

Inductors are very important in radio frequency and microwave design. They are needed for a wide range of applications from filters to biasing networks. They are necessary in RFICs as well, but, because an inductor's characteristics are determined by their physical dimensions, they often take up large amounts of die area. Because these inductors typically take the shape of a spiral to obtain the required electromagnetic characteristics, they are sometimes known as 'spiral' inductors. On-chip spiral inductors typically suffer from high parasitic resistance due to the available thin metal layers and highly doped, low resistivity substrates that are typical in CMOS processes. The high loss due to this parasitic resistance can reduce an on-chip inductor's quality factor, a measure of how much loss an inductor or capacitor has, to the point where it is no longer useful.

Integrated circuits, however, lend themselves to the design of complex active circuits, and high quality capacitors are widely available on integrated circuits.

Through the use of active devices and capacitors, artificial, or active, inductors can be created that have the characteristics of an inductor without the physical shape and size that would normally be necessary. The use of active circuits and capacitors to simulate inductance is not new, and there is considerable research into these active inductors to replace the large, low quality spiral inductors. [1] introduces a few simple CMOS circuits that can create an artificial inductance both with designable characteristics and an inductance that can be tuned. One example is shown in figure 1.1.

These simple CMOS inductor replacement circuits, known as active inductors, have been widely studied for the use in CMOS RFICs [2] [3]. They can achieve very high quality factors that are many times higher than possible with spiral inductors. And, because the circuit is only a few MOSFETs, these active inductors are much smaller than the spiral inductors that they replace.

Many on-chip circuits are possible only with the small size and high quality of these active inductors. [3] introduces a miniaturized Wilkinson power divider using passive capacitors and active inductors instead of transmission lines as one likely application for the simple active inductor circuits introduced in [1]. This application is also the focus for this work. [3] also notes that the active inductors can be tuned, and that this can be used to compensate for process variations.

One of the active inductor circuits introduced in [1] is of particular interest due to its capability for high quality factors and simplicity. The circuit of this active inductor, known as a Simple Cascoded Active Inductor (SCAI), is shown in figure 1.1. [2] finds an equivalent circuit model and analytical equations for determining the model parameters. The equivalent circuit model is shown in figure 1.2. The equations for determining the model parameters follow:

$$L = \frac{C_{gs2}}{g_{m1}g_{m2}}$$
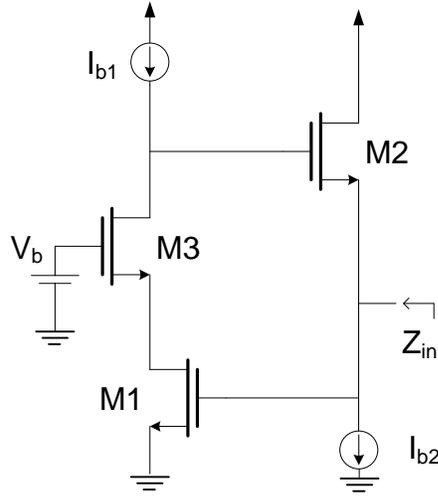
Figure 1.1: Schematic of simple active inductor introduced by [1].
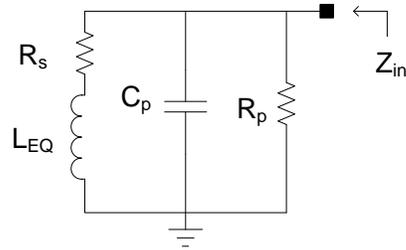
Figure 1.2: Equivalent circuit model for SCAI developed in [3].

$$R_s = \frac{-\omega^2 C_{gs2} C_{gs3}}{g_{m1} g_{m2} g_{m3}}$$

$$C_p = C_{gs1}$$

$$R_p = \frac{1}{g_{m1}}$$

Notice that these model parameters depend on parasitic gate to source capacitances and the small signal transconductance parameters, g_m, for the transistors in the circuit. Both the parasitic capacitances and g_m, which depends on the physical doping

levels, etc of the transistor, are heavily dependent on the parameters of the fabrication process used to create the integrated circuit. The fabrication process tolerances can have a very large effect on the equivalent circuit parameters, including inductance, of the active inductor. A commercial device needs to meet its design specifications over the full range of process variations specified by the process foundry, but, as Lyson [4] and Bucossi [5, 6] note, an active inductor design will have unacceptable variation in its characteristics over this range of process variations.

The equivalent circuit model parameters, especially the transconductance, g_m, will also vary due to changes in temperature, and the bias conditions I_1 and I_2 will vary with the applied supply voltage. Together with process variations, these effects are known as Process, Voltage, and Temperature (PVT) variations. The active inductor circuit is very sensitive to these variations and needs to be compensated in some way to achieve stable parameters over a useful range of PVT variations. This is especially important for commercial applications where devices need to meet specifications over the full range of process variations, and wide temperature and voltage ranges.

Previous Work

Considerable reseach has explored these active inductors and their possible applications [1–3], but very little research has been performed on compensation of these active inductors for PVT variations, though [2] notes that the tunability of these active inductors could be used to compensate for process variations. The only prior research in this area that the author is aware of is the work of Lyson [4] and Bucossi [5, 6] at Montana State University.

Lyson

Lyson [4] identified the lumped element Wilkinson divider as a likely application for the AI inductor and determined the necessary AI parameter tolerances for this application. Lyson then designed a phase-locked-loop control scheme to compensate the active inductor to remain within the required tolerances over a wide range of process, voltage, and temperature variations.

The active inductor was used as the tunable component in a voltage controlled oscillator (VCO). The VCO was then phase locked to a reference signal with a known frequency, effectively driving the AI to a known inductance. The AI control signal can then be used to control the active inductors in a Wilkinson divider, or other application, to that same inductance. A block diagram for this compensation scheme is shown in figure 1.3.
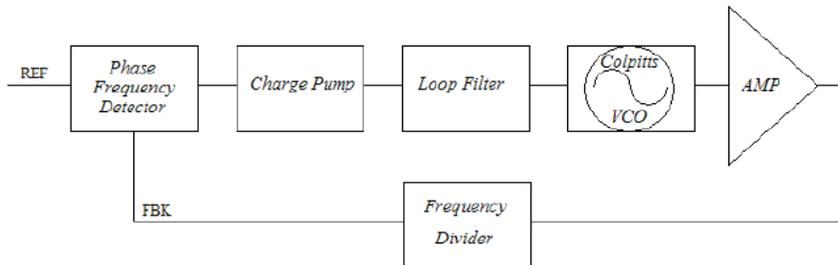
Figure 1.3: AI Compensation scheme designed by Lyson [4].

Lyson's active inductor compensation scheme met with limited success over the full range of simulated process variations. At certain process corners, the current mirror used to generate I_2 (see figure 1.1) was driven out of saturation and into the triode mode of operation, significantly changing its small signal characteristics, and making the active inductor lose its inductive characteristics [4]. Lyson's design also suffered from issues with the dynamic range of the active inductor. The simple

cascoded active inductor configuration begins to distort significantly above inputs of approximately 75mVpp. The VCO must be carefully designed so that the signal applied to the active inductor does not induce significant distortion, which is a very difficult condition to maintain over a wide range of PVT in a circuit that relies upon large-signal operation.

Bucossi

Bucossi [5,6] identified a different compensation scheme for the Wilkinson active inductor application that uses the Wilkinson itself as a central part of the control loop. The phase output of the lumped element Wilkinson has a heavy dependence on the inductance of the AI. The nominal phase shift of the output of the Wilkinson is 90 degrees, so the control loop adjusts the AI inductance until this value is reached. A block diagram of this compensation scheme is shown in figure 1.4.

There are a number of benefits to this control scheme:

- The behavior of the Wilkinson itself is corrected by the control loop so the master and slave active inductors will see the same circuit conditions.

- The control loop itself is simplified, because both signals into the phase detector are necessarily the same frequency so the PLL does not need to correct for frequency as well as phase.

- The magnitude of the signal seen by the active inductor can easily be controlled through the reference signal so that the active inductor does not introduce distortion.

There are a number of problems with this control scheme as well:

- A delay line is necessary to match the phases between the Wilkinson input and output signals.
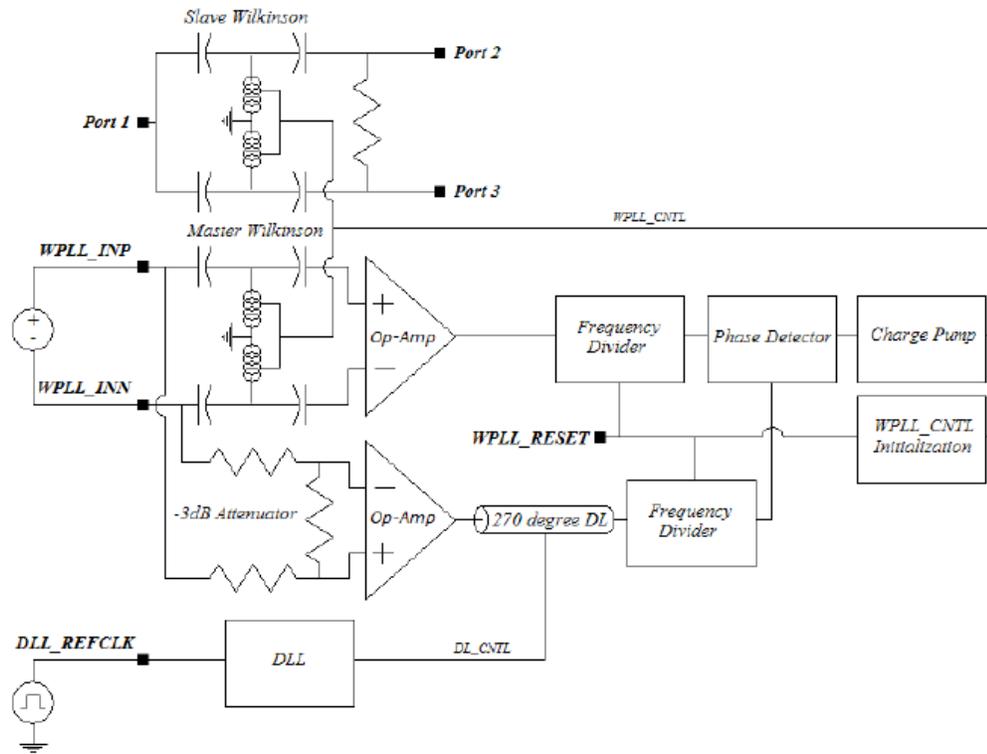
Figure 1.4: AI Compensation scheme designed by Bucossi [5].

- A second control loop is required to make sure that the delay line maintains its value over a full range of PVT.

- The use of digital delay lines and digital phase detection requires that the Wilkinson input and output signals be amplified from signals small enough to prevent AI distortion to signals with full digital swings. This will limit the application of this control scheme to frequencies low enough that this can be achieved.

- The large amount of digital circuitry needs separate supply voltage lines to avoid switching noise on the analog supply.

- The need for two full control loops and high gain requirements at the Wilkinson design frequency results in very high power consumption.

Bucossi's control scheme was, however, able to successfully compensate the active inductor over a very wide range of process, voltage, and temperature variations. This work investigates an active inductor compensation scheme that uses the same concept as that of Bucossi, but that eliminates many of the problems associated with the implementation.

IMPROVED CONTROL SYSTEM
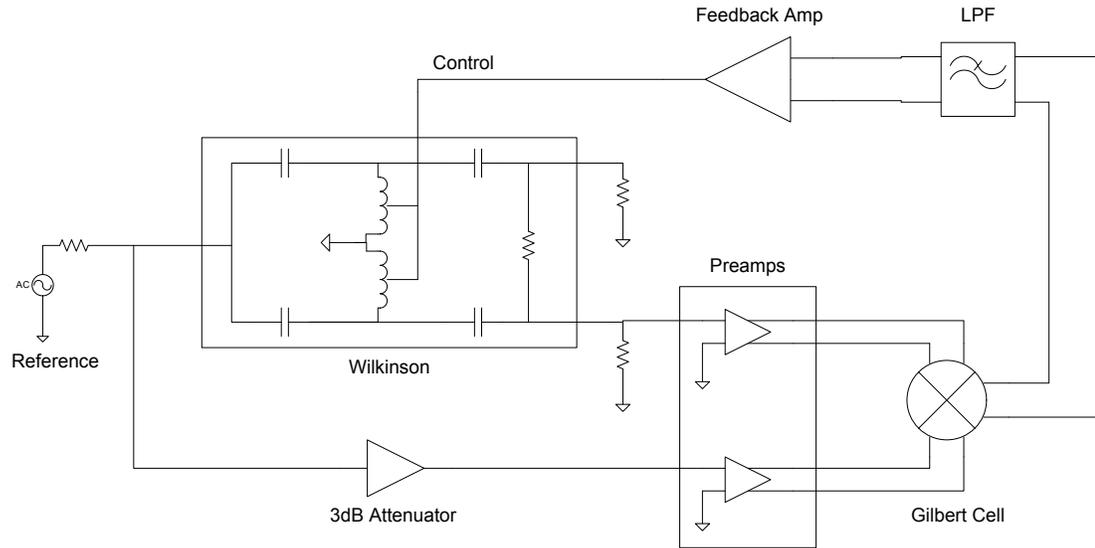
Figure 2.1: Block Diagram for improved control system.

Introduction to New Control System and Differences with Previous Work

The new control system shown in figure 2.1 is based on the same basic concept as Bucossi's control scheme: the error term is determined from the output phase of the Wilkinson divider. The main difference between the control scheme introduced by Bucossi and the improved control scheme stems from the use of a Gilbert cell [7] mixer as a phase detector instead of a digital phase frequency detector.

The use of a Gilbert cell phase detector allows the system to be simplified considerably. A multiplier based phase detector has an output of zero with the input signals shifted 90 or 270 degrees from one another. The control system should have an error signal of zero at 90 (or 270) degrees because this is the nominal Wilkinson

divider phase shift. This allows the elimination of the accurate 90 degree delay line and associated delay locked loop which drastically simplifies the system.

The use of an analog phase detector also simplifies the system, as the inputs to the phase detector do not need to be amplified to a full digital signal swing before being used. There is no further need for digital circuitry which can introduce large amounts of switching noise into the supply and ground lines. Because full digital swings are not required, higher reference frequencies are possible, allowing a reduction of the Wilkinson capacitor size required.

A Gilbert cell was chosen as the phase detector due to its differential configuration. Differential signaling reduces the sensitivity of the circuit to process, supply voltage, and temperature variations because these variations tend to result in common mode and gain fluctuations. Differential offsets will manifest themselves as DC phase offsets which need to be minimized for proper circuit operation. These differential offsets can be minimized through the use of component matching, which is the use of IC layout techniques to minimize the systematic differences between components from small scale process variations.

The use of an multiplier type phase detector will also introduce high frequency components in the output as well as the phase term at DC. An ideal multiplier will only introduce a component at twice the input frequency, any offsets present at the inputs will multiply to components at the input frequency itself, and, because of the use of real components, many higher order harmonics will also be present. The signal of interest is the phase signal around DC; the unwanted higher frequency components need to be removed using a low pass filter so that they do not corrupt the phase signal.

The attenuator is included for source matching and isolation of the Wilkinson input node.

System Analysis

A thorough analysis of the new control scheme needs to be performed so that it is clear how each component affects the operation of the system as a whole. Because the system is based on analog blocks, it is extremely important to understand the source of possible errors in the system, and to know where analog design effort needs to be concentrated.

Because of their importance to the control loop, the active inductor, Wilkinson, and Gilbert cell will be analyzed at the component level, while the effects of the amplifiers and low pass filter will only analyzed with respect to their block level characteristics.

In many cases, full equations are omitted due to length. Most symbolic computations were performed using MATLAB's symbolic math tool, MuPAD. The code used is attached in the appendices. Many of the analyses are confirmed in simulation.

Active Inductor

The active inductor topology chosen for this design is the same as in Bucossi [5] and Lyson [4], and originally presented in [1] (figure 2.2). This topology was chosen to maximize design reuse and to limit the amount of additional analysis that needs to be performed on the active inductor itself. [2] presents a simple equivalent circuit for this topology, figure 2.3, along with approximations for the components values L, R_s, C_p, and R_p (equations 2.1-2.4):

$$L = \frac{C_{gs2}}{g_{m1}g_{m2}} \tag{2.1}$$
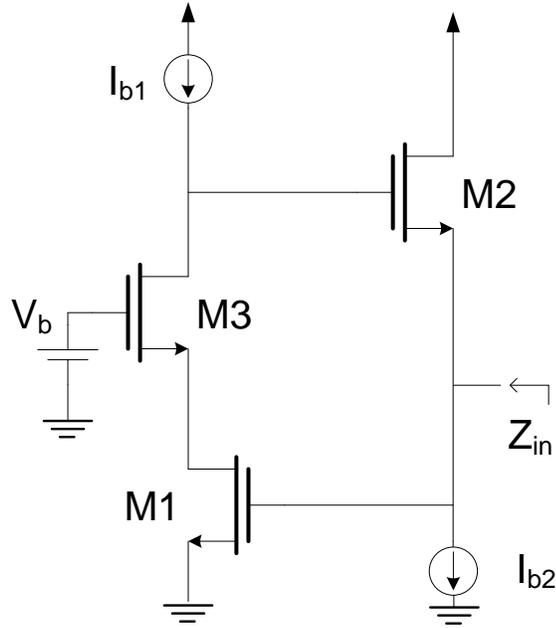
Figure 2.2: Simple active inductor topology introduced by [1].

$$R_s = \frac{-\omega^2 C_{gs2} C_{gs3}}{g_{m1} g_{m2} g_{m3}} \tag{2.2}$$

$$C_p = C_{gs1} \tag{2.3}$$

$$R_p = \frac{1}{g_{m1}} \tag{2.4}$$

Both Lyson [4] and Bucossi [5] present more accurate transfer function based active inductor models. The complexity, however, of these models precludes their use for active inductor design and full system analysis. The design of this topology active inductor is covered very adequately in [2–5] and so will not be covered here.

There are a few important things to note about the active inductor model described above. First, the shunt capacitance, C_p, effectively reduces the total equivalent inductance of the model. Assuming a large shunt resistance, R_p, and a small
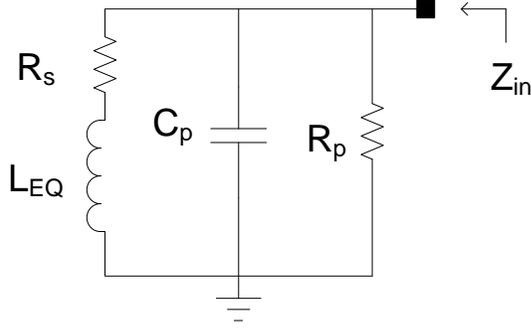
Figure 2.3: Active inductor equivalent circuit model introduced by [2].

series resistance, R_s, the equivalent inductance of the model can be found as shown in equation 2.5.

$$L_{tot} = \frac{\Im(Z)}{\omega} \approx \left(1 - \left(\frac{f_{op}}{SRF}\right)^2\right) L_{eq} \tag{2.5}$$

Where $\frac{f_{op}}{SRF}$ is the ratio of the frequency of operation to the self-resonant frequency of the inductor, $\frac{1}{2\pi\sqrt{L_{eq}C_p}}$. The lower the frequency of operation, the lower the impact of the shunt capacitance. Below 10% of the self-resonant frequency, the shunt capacitance reduces the total inductance by less than $0.1^2 = 1\%$.

Second, the negative resistance introduced by R_s (equation 2.2) can be used to cancel the resistive loss associated with the shunt resistance, R_p, as described in [2]. This effectively maximizes the quality factor by minimizing the real part of the total impedance. Unfortunately, these parameters can only be made to cancel at a single frequency, limiting the broadband applications of the active inductor.

The active inductor is controlled by varying one of the bias currents. I2 was chosen to control the inductance to simplify the generation of the cascode transistor gate bias voltage, V_b. This also simplifies the analysis as the characteristics of only one transistor will change. By changing only the characteristics of M2, only L and R_s change, and C_p and R_p will stay constant.

Additional circuitry must be added to the active inductor circuit to transform the control signal into the bias current, I2. Typically, the control signal is a voltage which must then be converted into the bias current to control the active inductor. There are any number of ways to convert a voltage signal to a current, but the simplest is to use a single transistor, as shown in figure 2.4. Source degeneration can be added to increase linearity and allow for finer control of the bias current. Figure 2.4 also shows the current mirrored to any slave active inductors to be controlled. More complex conversion circuits are generally unnecessary as the conversion is performed within the overall control loop.
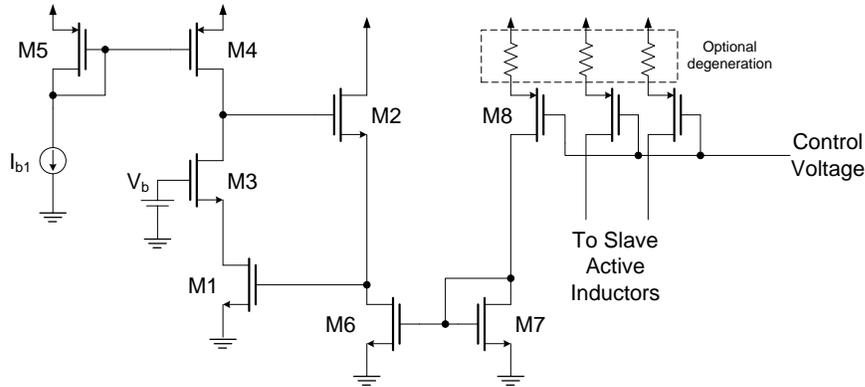
Figure 2.4: Active inductor with control voltage to bias current conversion.

This circuit can then be analyzed to determine the transfer function between the control voltage and change in the inductance, L. Any source degeneration is ignored here for the sake of simplicity.

First, the current generated by the control voltage must be determined. The PMOS transistor used to convert the control voltage is assumed to be in saturation so the equation for the drain current is (neglecting channel length modulation) [8]:

$$I_D = \frac{1}{2} K'_p \left(\frac{W}{L} \right)_8 (V_{SG} - |V_{tp}|)^2$$

Substituting in the control voltage:

$$I_D = \frac{1}{2} K'_p \left(\frac{W}{L}\right)_8 (V_{DD} - V_{control} - |V_{tp}|)^2$$

The transconductance can be expressed as [8]:

$$g_m = \sqrt{2 K'_p \left(\frac{W}{L}\right) I_D}$$

Substituting it all into the equation for the equivalent inductance (equation 2.1):

$$L_{eq} = \frac{C_{GS2}}{K'_n (V_{control} - V_{DD} + V_{tp}) \sqrt{2 \left(\frac{W}{L}\right)_1 \left(\frac{W}{L}\right)_2 \left(\frac{W}{L}\right)_8 I_{b1} K'_p}} \tag{2.6}$$
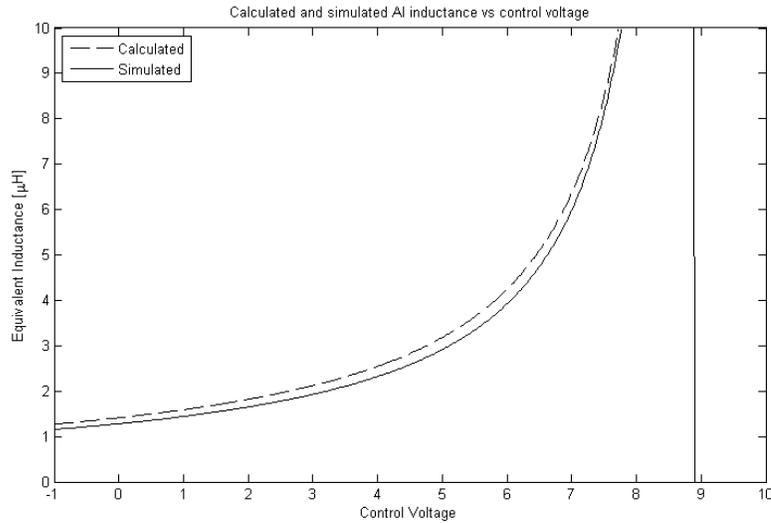
Figure 2.5: Calculated versus simulated AI equivalent inductances.

Figure 2.5 shows a comparison of the equivalent inductance calculated using eq. 2.6 and simulated inductance of an actual active inductor versus the control voltage. The schematic used for simulation is shown in figure 2.6, and is based on the schematic used to design the discrete AI described in section 3. A PMOS with a simple custom model (Mtest1) was used instead of an existing model to limit the current generation over the full range of control voltages (I_{b2} only needs to be $160 \mu A$

for the discrete AI). The parameters needed for eq. 2.6 were extracted from the various models.

Figure 2.6: Schematic used to test AI inductance versus control voltage equation.

The small difference between calculated and simulated inductance in figure 2.5 is likely due to the fact that the effect of the parasitic parallel capacitance, C_p, tends to reduce the effective inductance of the AI (eq. 2.5), but is not taken into account when calculating L_{eq} using eq.2.6.

The equation for the equivalent inductance (eq. 2.6) is then differentiated with respect to the control voltage to find the small signal gain from the control voltage to equivalent inductance:

$$\frac{\partial L_{eq}}{\partial V_{control}} = \frac{L_{eq}}{V_{DD} - V_{control} - V_{tp}} \tag{2.7}$$

Assuming $V_{tp} \approx \frac{V_{DD}}{5}$ (an approximation of the PMOS threshold voltage), and an operating point at $V_{control} \approx \frac{V_{DD}}{2}$ for maximum possible signal swing, a 1% change in $V_{control}$ will result in a 1.6667% change in inductance. Because of the nature of equation 2.7, the gain increases as $V_{control}$ approaches V_{DD}, and decreases as it progresses further away.

MOSFET sensitivity to temperature is typically modeled as variations in the threshold voltage and carrier mobility [9]. The effects of threshold voltage temperature variation can be minimized by using a temperature independent biasing scheme to generate the reference currents that bias the active inductor. Variations in carrier mobility, however, directly effect the small signal transconductance, g_m, resulting in variations in all component values in equations 2.1-2.4, except C_p.

At a given bias current, the transconductance is proportional to the square root of the carrier mobility:

$$g_m = \sqrt{2\mu C_{ox}\left(\frac{W}{L}\right)I_D}$$

Using equation 9.49 from [9], the carrier mobility can be modeled as:

$$\mu(T) = \mu(T_o)\left(\frac{T_o}{T}\right)^{1.5}$$

Substituting the equation for transconductance back into the equation for equivalent inductance:

$$L_{eq}(T) = \frac{L_{eq}(T_o)}{\left(\frac{T_o}{T}\right)^{1.5}} = L_{eq}(T_o)\left(\frac{T}{T_o}\right)^{1.5}$$

For a commercial temperature range (0C to 70C) and active inductor designed at room temperature (27C), the inductance can vary from 87% of the designed inductance at the low end of the temperature range to 122% at the high end even without any variations in bias conditions.

One other important characteristic of this active inductor topology is distortion. Bucossi [5] found that the active inductor significantly distorted above signal levels of $\sim 80mV_{p-p}$, rendering it unusable above that level. [2] notes that the level at which the active inductor distorts can be increased by increasing the transistor overdrive voltages, but this is limited by the available supply voltage.

Lumped Element Wilkinson

Along with the Gilbert cell, the lumped element Wilkinson divider is an extremely important part of the system. The Wilkinson is both an important application of the active inductor and the way in which the control system detects the inductance. Thorough analysis of the Wilkinson divider is therefore needed. A schematic of the lumped element Wilkinson divider is shown in figure 2.7.
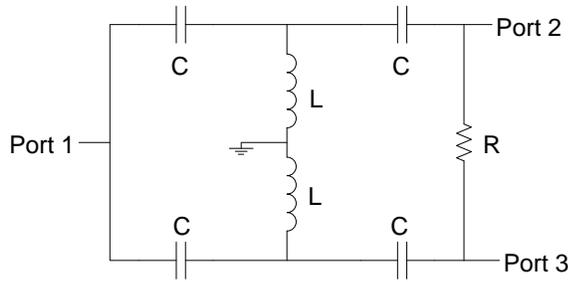
Figure 2.7: Lumped element Wilkinson divider schematic from [3].

For matching, the components must have the following parameters:

$$L = \frac{\sqrt{2}Z_o}{\omega} \tag{2.8}$$

$$C = \frac{1}{\sqrt{2}Z_o\omega} \tag{2.9}$$

$$R = 2Z_o \tag{2.10}$$

The first step in analyzing the Wilkinson divider is to replace the ideal inductors with the equivalent circuit shown in figure 2.3. This greatly complicates the analysis, but is necessary to determine the effect of active inductor characteristics on the performance of the Wilkinson. The transfer function from the voltage at Port 1 to the voltage at Port 2, assuming ideal inductance, perfect matching at all ports,

and excitation through port 1 is shown in equation 2.11. The transfer function using the active inductor equivalent circuit is too long to include here.

$$\frac{V_{p2}}{V_{p1}} = -\frac{C^2\,L\,\mathrm{Zo}\,\omega^3\,\left(\mathrm{Zo}\,C\,\omega - L\,C\,\omega^2\,2\,\mathrm{i} - L\,\mathrm{Zo}\,C^2\,\omega^3 + \mathrm{i}\right)}{C^4\,L^2\,\mathrm{Zo}^2\,\omega^6 - 2\,C^3\,L\,\mathrm{Zo}^2\,\omega^4 + 4\,C^2\,L^2\,\omega^4 + C^2\,\mathrm{Zo}^2\,\omega^2 - 4\,C\,L\,\omega^2 + 1} \tag{2.11}$$

The phase of the transfer function is then:

$$\angle\left(\frac{V_{p2}}{V_{p1}}\right) = -\arctan\left(-\frac{2\,C\,L\,\omega^2 - 1}{C\,\mathrm{Zo}\,\omega\,(C\,L\,w^2 - 1)}\right) \tag{2.12}$$

It is very important that the components in the equivalent circuit other than the inductance itself do not have a large impact on the output phase of the Wilkinson divider. If these components representing the imperfections of the active inductor have a significant impact on the phase at realistic values then this control scheme will not accurately control the inductance.

One of the most significant impacts is that of the equivalent shunt capacitance. If the active inductor is operated at a significant fraction of its self resonant frequency, greater than roughly 10%, the shunt capacitance adds a significant offset to the output phase. This occurs because the shunt capacitance effectively reduces the equivalent inductance of the equivalent circuit as shown in equation 2.5.

As long as the active inductor has a high quality factor at the Wilkinson design frequency, the shunt and series resistances of the equivalent circuit have a negligible effect on the Wilkinson response.

The effect of a change in inductance can be found by differentiating the phase transfer function with respect to the inductance and evaluating it at the design point defined be equations 2.8 and 2.9:

$$\left.\frac{\partial \angle TF}{\partial L}\right|_{L=\frac{\sqrt{2}Z_o}{\omega},\,C=\frac{1}{\sqrt{2}Z_o\omega}} = \frac{1}{\sqrt{2}L}\,[rad/H]$$

Multiplying by a 1% change in inductance:

$$\Delta\angle TF = \left.\frac{\partial\angle TF}{\partial L}\right|_{L=\frac{\sqrt{2}Z_o}{\omega},C=\frac{1}{\sqrt{2}Z_o\omega}} * \Delta L = \frac{1}{\sqrt{2}L}0.01L = -0.005\sqrt{2}[rad] = -0.4[\text{deg}]$$

This relationship was also verified using the more complicated transfer function with the AI equivalent circuit instead of an ideal inductance. The 0.4 degree phase change for a 1% change in inductance holds so long as the active inductor is operated well below its self-resonant frequency and designed such that the quality factor is relatively high (the resistances cancel).

The lumped element Wilkinson capacitors also have a large effect on the output phase. The effect of a change in capacitance can be analyzed in the same way as a change in inductance. First, the angle of the transfer function (equation 2.12) needs to be differentiated with respect to capacitance and evaluated at the design point:

$$\left.\frac{\partial\angle TF}{\partial C}\right|_{L=\frac{\sqrt{2}Z_o}{\omega},C=\frac{1}{\sqrt{2}Z_o\omega}} = \frac{1}{\sqrt{2}C}[rad/F]$$

Again, if the above equation is multiplied by a 1% change in capacitance:

$$\Delta\angle TF = \left.\frac{\partial\angle TF}{\partial C}\right|_{L=\frac{\sqrt{2}Z_o}{\omega},C=\frac{1}{\sqrt{2}Z_o\omega}} * \Delta C = \frac{1}{\sqrt{2}C}0.01C = -0.005\sqrt{2}[rad] = -0.4[\text{deg}]$$

This is exactly the same change in phase for a 1% change in inductance. This means that if the capacitances are some percentage larger than their nominal value, the inductance will have to be that same percentage smaller than their nominal value to maintain 90 deg output phase. Therefore, any error in capacitance introduces a systematic offset to the control loop.

Temperature variations typically have a very small effect on capacitance (around 20ppm/℃ [9]). Process variations are therefore typically the cause of capacitor tolerances. High accuracy capacitors should be used if available, or the capacitors may need to be trimmed after manufacturing to achieve the necessary level of accuracy.
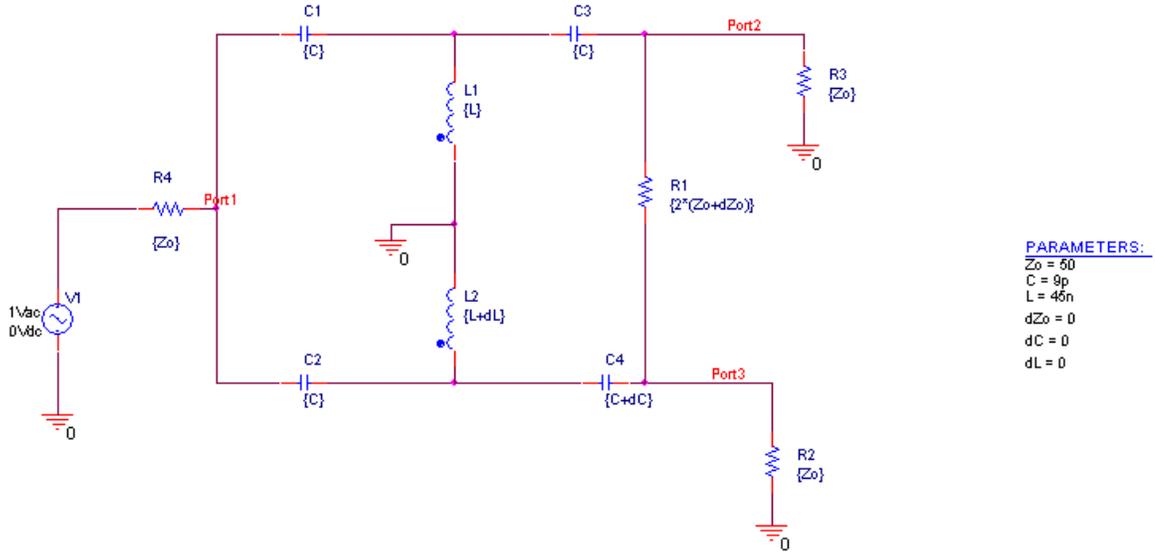
Figure 2.8: Schematic of circuit used to simulate effect of inductance and capacitance changes on the transfer function phase.

The effects of changes in inductance and capacitance were also simulated to verify the above calculations. Figure 2.8 shows the PSPICE schematic used for these simulations. The design point for the Wilkinson was chosen to be similar to that of Bucossi [5]: $f = 250MHz$, $Z_o = 50\Omega$, $L = 45nH$, $C = 9pF$. Each component was then swept $\pm 10 - 20\%$ of the design point and the phase difference between ports 1 and 2 was observed.

Figure 2.9 shows the variation of phase with respect to changes in capacitance. A 1% change in capacitance is 0.09pF or just less than one minor grid space. This

Figure 2.9: Change in phase for various capacitance values.
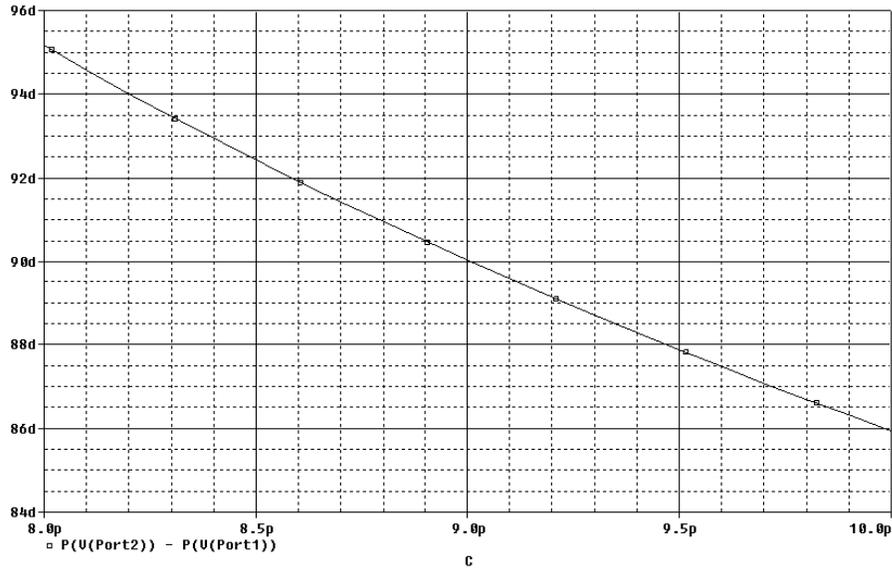
change in capacitance corresponds to an approximately 0.4 degree change in phase around the 90 degree nominal point, confirming the above calculations.

The variation of phase with respect to inductance is shown in figure 2.10. Again, a 1% change in inductance is 0.45nH, about half of a minor grid space. The change in phase for this change in inductance is just less than one half minor grid space, or approximately 0.4 degrees, again confirming the calculations performed above.

The effects of changes in the characteristic impedance, Z_o, had only a negligible effect on the phase (less than a 0.01 degree variation for a 20% variation in impedance). Temperature varations of the load and isolation resistors will therefore have little to no effect on Wilkinson phase, although the magnitudes of the signals are likely to change.

The effects of mismatches between the AI inductances were also investigated. Using a technique similar to that used to find the effect of a 1% change in inductance above, the effect of a 1% change in just L_1 was found to be $-0.3\,\mathrm{deg}$ and the effect
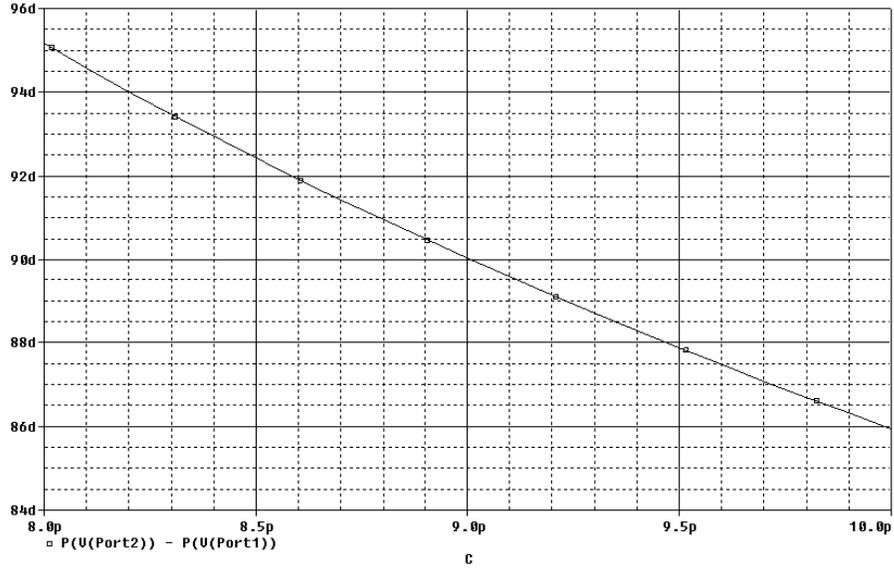
Figure 2.10: Change in phase for various capacitance values.

of a 1% change in only L_2 was found to be $-0.1\,$deg. The mismatch between the two inductances can be analyzed by setting the base inductance to the average of the two inductances:

$$L_{base} = \frac{L_1 + L_2}{2}$$

Each inductance can then be represented as the base inductance plus or minus the mismatch:

$$L_1 = L_{base} + \frac{\Delta L}{2}$$

$$L_2 = L_{base} - \frac{\Delta L}{2}$$

Where $\Delta L = L_1 - L_2$.

Now the total phase difference for a 1% mismatch ($\Delta L = 0.01L$):

$$\Delta Phase = \Delta Phase_{L_1} + \Delta Phase_{L_2} = \frac{-0.3\,\text{deg}}{2} + -1\frac{-0.1\,\text{deg}}{2} = -0.1\,\text{deg}$$

This shows that small mismatches should not have a large effect on the operation of the circuit. A simulation verifying these calculations is shown in figure 2.11.

Figure 2.11: Simulation results verifying 0.1 degree phase shift per 1% inductor mismatch.
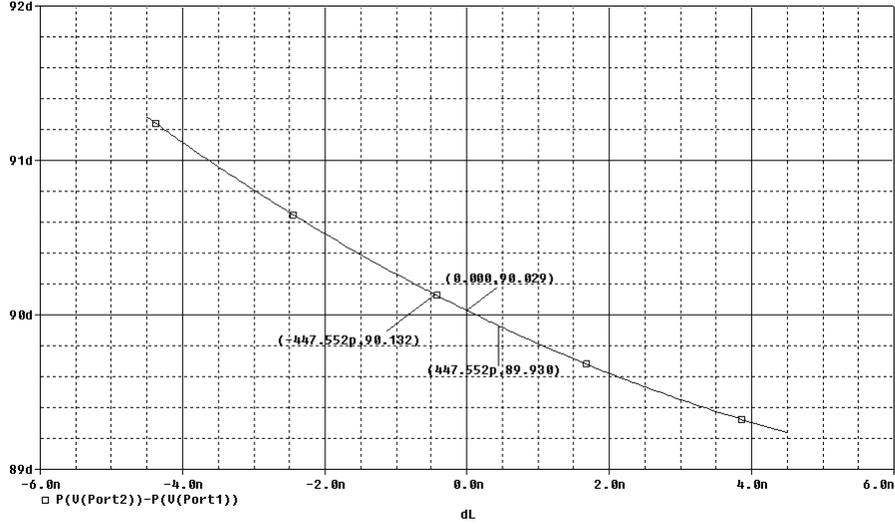
The same mismatch calculations were repeated for the capacitors, C_1 - C_4. It was found that small variations in C_3 and C_4 had negligible effect on the phase transfer function. A 1% change in C_1 changed the phase by -0.3 deg; the same change in C_2 changed the phase by -0.1 deg. Therefore, C_1 and C_2 should be matched, while matching C_3 and C_4, to each other or C_1/C_2, is completely unnecessary. Using the same technique as for the inductance mismatch, a 1% mismatch between capacitors C_1 and C_2 results in a 0.1 degree phase shift. Simulation results verifying these calculations is shown in figure 2.12.

A differential Wilkinson type circuit, as introduced by Bucossi [5], can also be used in place of the single ended version analyzed here. Although a thorough analysis of this circuit was not performed, the same phase response should be observed [5], and the same design and matching concerns should apply.
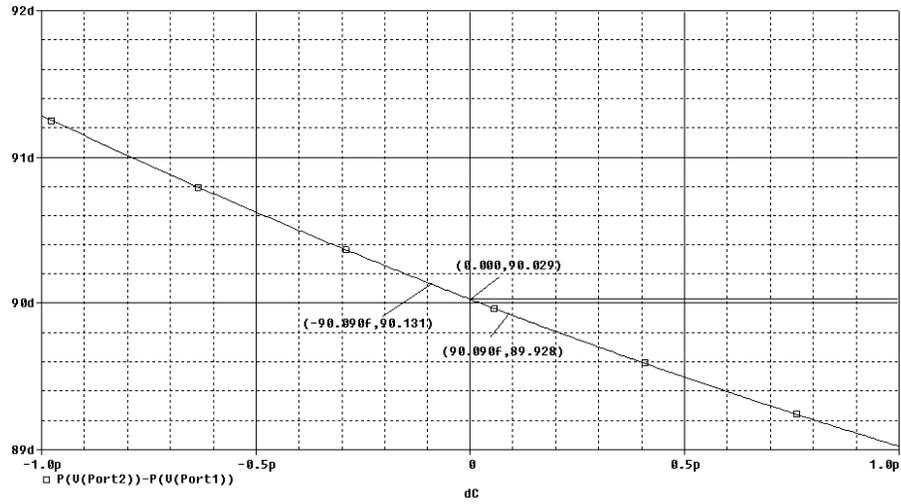
Figure 2.12: Simulation results to verify 0.1 degree phase shift per 1% mismatch between capacitors C_1 and C_2.

Preamplifiers

The preamplifiers prior to the Gilbert cell are necessary to provide adequate signal levels to the Gilbert cell and perform a single-ended to differential signal conversion if a normal, single-ended Wilkinson divider is used. They may not be necessary if the amplitude of the signal through the Wilkinson divider is adequate and a differential Wilkinson circuit is used. The internal circuitry of these amplifiers is not important; the analysis will only consider gain, frequency response, common mode rejection, and offsets.

The most important aspect of the preamplifiers is that they both have the same phase response at the frequency of operation. Any differences in the phase response will result in the control loop locking to an offset instead of the ideal 90 degrees. If, for instance, the frequency of operation is close to the amplifier pole location where the phase vs frequency slope is high, any small shift in pole location will result in a larger phase difference than if the frequency used is more than a decade away from the amplifier pole location, where the phase slope is low. The absolute phase shift

generated by each amplifier is not a concern, however, only the difference in phase shift between the two amplifiers.

Any equivalent input offsets of the preamplifiers will be amplified before being applied to the Gilbert cell, then multiplied by the Gilbert cell, resulting in a differential offset current at the output of the Gilbert cell that is indistinguishable from the phase signal. The preamplifiers must therefore be carefully designed to minimize any offsets.

The common mode response of the preamplifiers is important if they are being used to perform a single-ended to differential conversion. When performing this conversion, one of the amplifier inputs is held at a reference voltage (small signal ground), and the other input is connected to the single-ended signal. The effective differential input voltage is: $V_{in\ diff} = V_{in1} - V_{in2} = V_{sig}$, while the effective common mode input voltage is: $V_{in\ cm} = \frac{V_{in1}+V_{in2}}{2} = \frac{1}{2}V_{sig}$. The input common mode voltage variation is simply the input signal with its amplitude halved.

The common mode variations have the same phase as their respective input signals, so the common mode signals can be mixed by the Gilbert cell to result in a phase dependent common mode offset at the output of the Gilbert cell. It is very important for the preamplifiers to have good common mode rejection to reduce this effect.

If the signal levels from the Wilkinson are very low, it may be necessary to include noise performance in the required specifications of the preamplifiers. Other techniques, including bandpass filtering the preamplifier inputs and outputs through capacitive coupling can be used to improve noise performance if the size penalty imposed by the coupling capacitors is not too large. The use of capacitive coupling also eliminates the effects of offsets in the premplifiers.

Gilbert Cell

The Gilbert cell multiplier is the heart of the control system. It takes the high frequency phase shifted signals from the Wilkinson and outputs a phase signal to be fed back into active inductor control voltage. The schematic for a Gilbert cell is shown in figure 2.13.
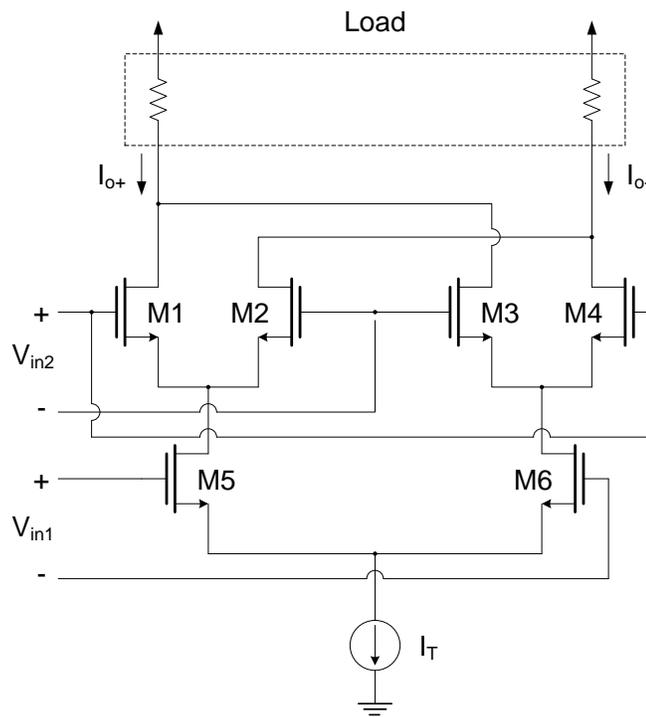
Figure 2.13: Gilbert cell schematic.

In figure 2.13, the Gilbert cell has resistive loads, but other loads can be used depending on whether the low pass filter and feedback amplifier are configured for a current or voltage signal. The output signals of interest from the Gilbert cell itself are the output currents, I_{o+} and I_{o-}. These currents can be converted to voltages using resistive loads, or re-directed using current mirror loads, or some other type of load can be used.

The first step to analyzing the Gilbert cell is to find the output current of a single differential pair. Chapter 3 in Gray [10] includes this analysis, but does not include the possibility of mismatch, which greatly complicates the analysis and results in equations too long to replicate in this paper. The output currents for a single differential pair with tail current, I_T, are shown in equations 2.13 and 2.14, neglecting mismatch (identical to equations 3.158 and 3.159 in Gray [10]). The equations with mismatch are too long to include here.

$$I_{d1} = \frac{I_T}{2} + \frac{V_{id}\sqrt{K_n'\left(\frac{W}{L}\right)\left(4I_T - V_{id}^2\left(\frac{W}{L}\right)K_n'\right)}}{4} \tag{2.13}$$

$$I_{d2} = \frac{I_T}{2} - \frac{V_{id}\sqrt{K_n'\left(\frac{W}{L}\right)\left(4I_T - V_{id}^2\left(\frac{W}{L}\right)K_n'\right)}}{4} \tag{2.14}$$

These equations can be applied to the differential pairs of M5/M6, M1/M2, and M3/M4 to determine a formula for the output currents, assuming matched devices:

$$\begin{aligned}
I_o &= I_{o+} - I_{o-} \\
&\approx \frac{V_{in2}\sqrt{K_n'}\left(\sqrt{2\left(\frac{W}{L}\right)\left(I_T + V_{in1}\sqrt{2K_n'I_T\left(\frac{W}{L}\right)}\right)} - \sqrt{2\left(\frac{W}{L}\right)\left(I_T - V_{in1}\sqrt{2K_n'I_T\left(\frac{W}{L}\right)}\right)}\right)}{2}
\end{aligned} \tag{2.15}$$

with $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)$ and $\left(\frac{W}{L}\right)_5 = \left(\frac{W}{L}\right)_6 = 2\left(\frac{W}{L}\right)$. Transistors 5 and 6 should be twice the size of 1,2,3, and 4 to keep the input loading identical between the two inputs.

Equation 2.15 can then be separated into the second input times a function of the first:

$$I_o = V_{in2} \cdot f(V_{in1})$$

Now the Taylor series expansion of $f(V_{in1})$ can be found:

$$f(V_{in1}) = V_{in1}\left(\frac{W}{L}\right)K_n' + \frac{V_{in1}^3\left(\frac{W}{L}\right)^2 K_n'^2}{4I_T} + O\left(V_{in1}^4\right) \approx V_{in1}\left(\frac{W}{L}\right)K_n'$$

The output current to a first order is then:

$$I_o = \left[\left(\frac{W}{L} \right) K'_n \right] V_{in1} V_{in2} \qquad (2.16)$$

The inputs will be phase shifted sine waves:

$$V_{in1} = A_1 cos(2 * \pi * f_o * t)$$

$$V_{in2} = A_2 cos(2 * \pi * f_o * t + \phi)$$

$$I_o = \frac{A_1 A_2 (W/L) K'_n}{2} cos\phi + 2 * f_o \text{ Term} \qquad (2.17)$$

If V_{in1} is the Wilkinson input and V_{in2} is the output, the nominal phase shift, ϕ will be 270 degrees. The linear gain around the operating point is then:

$$\frac{I_o}{\phi} \approx \frac{A_1 A_2 (W/L) K'_n}{2} \qquad (2.18)$$

If any offsets, from the previous stage or V_t mismatch in the Gilbert cell, are present at the inputs they will be multiplied as shown in equation 2.16. In order for the offsets to introduce less than a 1% error in the AI inductance, the offsets must introduce less than a 0.4 degree(0.007[rad]) change in the detected phase:

$$\frac{A_1 A_2 (W/L) K'_n}{2} \phi > V_{off1} V_{off2} K'_n (W/L) \qquad (2.19)$$

$$\frac{A_1 A_2}{V_{off1} V_{off2}} > 286.5$$

$$\frac{A}{V_{off}} \gtrsim 17$$

According to equation 2.19, any offsets at the input to the Gilbert cell must be 17 times less than the amplitude of the input signals to maintain phase, and, therefore, AI inductance, accuracy. For 5% error in inductance this drops to a ratio of 7.6; for 10% it drops to a ratio of 5.4.

Equations for the output current with mismatch parameters for V_t and $\left(\frac{W}{L} \right)$ were calculated using MATLAB's symbolic math toolbox. Due to length and complexity, the full equations will not be repeated here. Using the symbolic math toolbox,

various matching arrangements were tested to determine which combination worked
the best. Ideally, all six transistors would be matched, but it may not be possible
to have a layout configuration that can ensure good matching between that many
transistors. Layout techniques can easily accomodate matching between two transis-
tors, so the matching of various transistor pairs was investigated. It was found that
only matching between M1/M4, M2/M3, and M5/M6 eliminated offsets in the output
current. If the size mismatch was ignored, matching between M1/M2,M3/M4, and
M5/M6 also worked. The Gilbert cell circuit can then be re-drawn to show which
transistors need to be matched (figure 2.14).

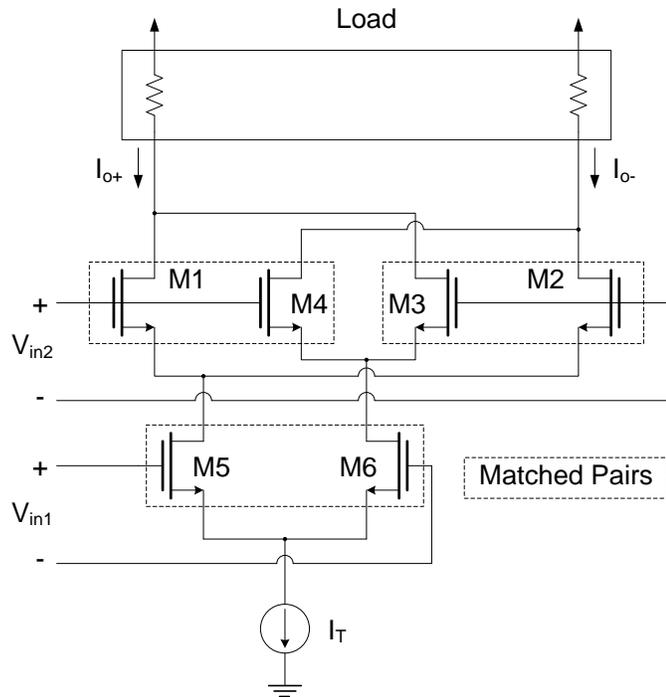Figure 2.14: Gilbert cell schematic with matching pairs shown.

Another important characteristic of the Gilbert cell is the response to common
mode variations. A change in the common mode voltage at V_{in1} will result in a change
in the common mode current of $V_{in1\ CM}/R_T$ where R_T is the output resistance of the
current mirror generating I_T. Any common mode input on V_{in2} will see a much higher

equivalent tail current output resistance due to the effective cascoding of M5/M6 over the tail current, and will, therefore, create a much smaller common mode output current.

The use of a differential circuit should preserve the phase signal integrity over a wide range of process and temperature variations. Any offsets that are present may drift with temperature, but this can be minimized with careful layout techniques, and care must be taken that the total offset not exceed the limit determined by the amount of acceptable phase variation and equation 2.19.

Low Pass Filter

The Gilbert cell output of interest is the phase signal at DC, but the Gilbert cell also outputs signals at higher frequencies, f_o (if DC offsets present at GC input), $2f_o$, etc. These unwanted higher frequency signals need to be attenuated so that they do not corrupt the feedback signal. A low pass filter is needed for this purpose.

A single pole low-pass filter is assumed for this system because it should be able to attenuate the signals at f_o, $2f_o$, etc, without adding undue phase to the feedback system. The pole of the LPF and the pole of the feedback amplifier are typically the dominant poles of the system. Using only a single pole LPF significantly reduces the complexity of stability analysis and design. The exact topology of the LPF will typically depend on the Gilbert cell output (voltage or current, impedance, etc), and on the input conditions of the feedback amplifier. The use of a differential configuration typically reduces the complexity of the filter, but two single-ended configurations can also be used. Single-ended configurations do have the added bonus of filtering both differential and common-mode signals, while differential filters can typically only filter differential signals.

Feedback Amplifier

The feedback amplifier is necessary to provide the required gain to make the loop converge to a steady state with minimum error. The exact type of amplifier used is determined by the signals from the Gilbert cell and LPF. The important characteristics of the amplifier are the gain, bandwidth, common mode rejection, and input offset. The tradeoff between gain and bandwidth needs to be analyzed with respect to full system performance, and is discussed in the next section.

The input offset of the amplifier can be analyzed with respect to its effect on the phase signal. The effects of current and voltage offsets depend on the amplifier configuration and the configuration of the low-pass filter which can be chosen depending on overall circuit needs. However, because the offsets of the feedback amplifier apply after the gain of the Gilbert cell, they will typically have less of an effect than the offsets due to the Gilbert cell itself.

Loop Design

The total loop gain of the system can be approximated as:

$$K_{tot} \approx K_{cntl-L} K_{L-\phi} K_{PD} K_{FB} \tag{2.20}$$

Where K_{cntl-L} is the gain from the control voltage to the AI inductance, $K_{L-\phi}$ is the gain from inductance to change in Wilkinson output phase, K_{PD} is the phase detection gain, and K_{FB} is the feedback amplifier gain. These will all depend on circuit conditions that will change from design to design, but can easily be found using the formulas found in the preceding sections.

The total open-loop transfer function can be approximated as:

$$TF_{OL} = \frac{K_{tot}}{\left(\frac{s}{p_1} - 1\right)\left(\frac{s}{p_2} - 1\right)} \tag{2.21}$$

With the closed loop transfer function taking the form:

$$TF_{CL} = \frac{K_{tot}p_1p_2}{s^2 - s(p_1 + p_2) - p_1p_2(K_{tot} - 1)} \tag{2.22}$$

Where p_1 and p_2 are the poles introduced by the low pass filter and the feedback amplifier.

This second order approximation can then be used to design desired closed loop system characteristics, such as overshoot, settling time, DC error, etc. Process, temperature, and supply voltage variations will typically vary the absolute gains and pole locations in the above transfer functions. The servo action of the control loop will tend to minimize the effect of these variations on the inductance of the active inductor, resulting in an inductance that has a very stable value.

The largest sources of possible error in this system are due to the absolute accuracy of the capacitors in the Wilkinson divider and differential offsets in the amplifiers and Gilbert cell.

The capacitors in the Wilkinson divider need to be very accurate to ensure a nominal 90 degree phase shift when the inductance of the AI is correct. A 1% error in capacitance will result in a 1% offset in inductance to achieve the correct 90 degree shift. The capacitor accuracy must therefore be better than the required inductor accuracy for whatever application is being considered. For instance, Bucossi [5] noted an allowable ±16% inductance range for a Wilkinson application; that inductance range would require that the capacitors not deviate beyond 16% of their nominal value over the full process and temperature range.

Differential offsets also must be considered when determining total loop accuracy. Equation 2.19 shows the relationship between the total offset at the input to the Gilbert cell, the input amplitudes, and the resulting phase error. The total

offset at the input of the Gilbert cell includes offsets from the feedback amplifier, the Gilbert cell itself, and the preamplifiers if they are DC coupled to the Gilbert cell.

If the preamplifiers are DC coupled, the largest offset at the Gilbert cell input is usually the offset due to the preamplifier as its input offset must be multiplied by its gain to find its contribution at the input of the Gilbert cell. The input signal to the Gilbert cell is also multiplied by the preamplifier gain, so the ratios found using equation 2.19 must apply at the *input* of the preamplifiers. The signal amplitudes at the inputs of the preamplifiers are relatively weak with amplitudes lower than 40mV peak [5], so the preamplifier input offsets must be very low, less than 10mV even for an inductance errors up to 16%.

If the preamplifiers are AC coupled to the Gilbert cell, their offsets will be blocked, so that all offsets will be compared to the input signals after they have been multiplied by the preamplifier gain. As long as there is still significant gain through the coupling capacitors, the effect of the offsets will be much reduced. There is a size penalty associated with using coupling capacitors, but the high output resistances that are typical with common source topology based amplifiers helps keep the required capacitor size small. For example, a 100fF coupling capacitor used between an amplifier with an output resistance of 5kΩ and the Gilbert cell with an input resistance of 50kΩ, the corner frequency of the high pass response is 26MHz, well below the frequencies this circuit would typically be used at (the capacitors in the Wilkinson divider become very large at low frequencies). A 100fF capacitor will typically only take up 10μm by 10μm, a minimal size penalty to eliminate the issues associated with preamplifier offsets. The high-pass filter effect of coupling capacitors also helps reduce the amount of noise power coupled to the Gilbert cell.

The effect of the preamplifier offsets can also be reduced by redesigning the active inductor to allow higher signal swings as noted in section 2.

DISCRETE DEMONSTRATION SYSTEM

To fully design, simulate, layout, fabricate (with the help of MOSIS), and test the entire control scheme is outside of the scope of this project. It is still important, however, to have concrete results, outside of simulation, to demonstrate that the theory of the system actually fits the observed behavior.

To this end, a version of the control scheme was designed using discrete components and much lower operating frequency. There are many benefits to a discrete realization:

- The circuitry can easily be modified if necessary.

- All of the circuit nodes are available for test and debug.

- Process variations can be simulated by swapping components.

Differences from IC system

There are many differences between a discrete realization and an integrated system. Resistive biasing, for instance, is very inaccurate for use in integrated circuits, where more complex biasing circuits are used, but is very easy to apply in a discrete system.

The largest difference between a discrete system and a system implemented in a CMOS integrated circuit is the types of components available. In a CMOS process, there may not be good quality bipolar transistors or resistors available, but each individual MOSFET can be designed for its individual purpose. In the discrete version a wide range of components are available, but the individual components cannot be re-designed.

Due to component availability, most of the transistors that would be MOS-FETs in a CMOS integrated circuit have been replaced by small signal bipolar transistors. In fact, the only MOSFETs that remain in the discrete system are the MOSFETs at the heart of the active inductor itself.

<div align="center">Design of Discrete System</div>

Active Inductor

The NMOS device chosen for the active inductor is the 2N7000 due to the ready supply of available parts at ECE Department Stockroom. Normally when designing an active inductor, one would begin with some specifications of inductance, quality factor, and operating frequency, and build the circuit to those specifications. However, because the parameters of the discrete transistors cannot be changed, the transistors were simply put in the correct cascoded active inductor configuration, and the bias currents varied to determine the best frequency to operate at. Figure 3.1 shows the circuit used to determine the optimum frequency of operation.

This circuit was simulated over a wide range of different bias currents to determine the best frequency of operation. To determine the best frequency of operation, the design of the Wilkinson power divider must be considered as well. (reference Wilkinson divider equation here) shows the relationship between the inductance, operating frequency, and system impedance of the lumped element Wilkinson divider. Figure 3.2 shows an example of simulation results used to determine the optimum design point. The AI can be used in the Wilkinson divider where the calculated AI inductance and required Wilkinson divider inductance curves are equal. Additional constraints include using the AI well below its self-resonant frequency, and using it where the quality factor is high.
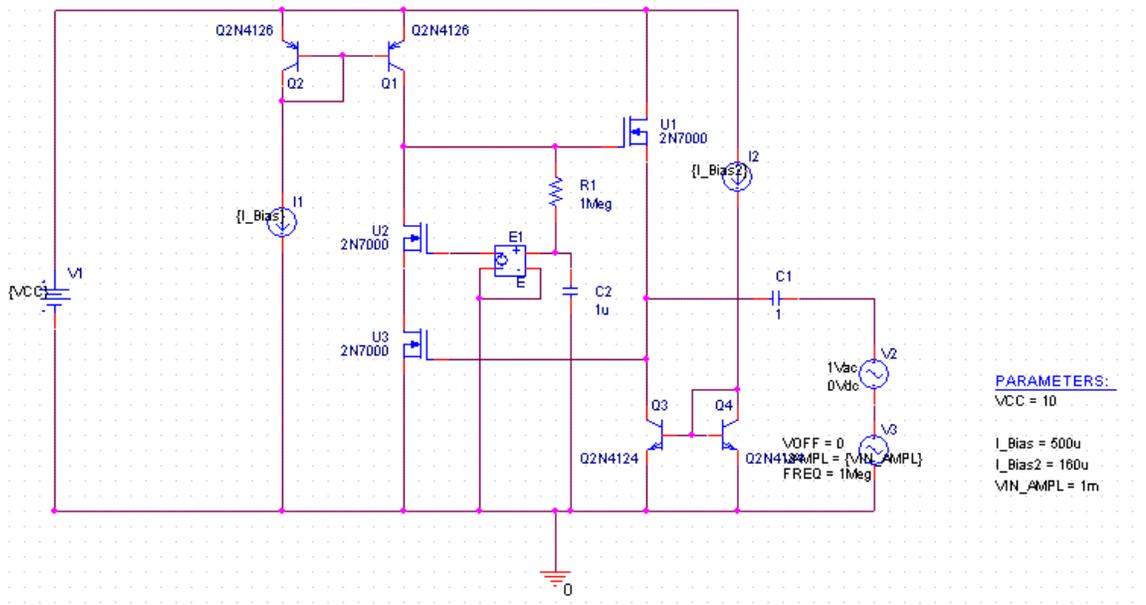
Figure 3.1: AI Schematic used to determine optimum bias point and frequency of operation. The voltage-controlled voltage source, E1, along with R1 and C2 is used to keep the transistor U2 in the saturation region over a wide range of bias currents.

As can be seen in figure 3.2, the active inductor constructed with 2N7000 transistors is very close to its self-resonant frequency for all Wilkinson system impedances above 10 Ohms. The quality factor of the active inductor is also included to show that it is imperative to choose a design point near where the quality factor peaks. The chosen design point for the discrete system was at a frequency of 1MHz, a system impedance of 10Ω, and bias currents of $500\mu A$ and $160\mu A$, respectively.

Simulations showed that the operation of this active inductor begins to distort at signal levels as low as $5mV_{pp}$. This is likely due to the MOSFETs being operated at a very low overdrive voltage. When the gate voltage of M1 is very close to its threshold voltage, any small negative voltage deviation can drive it out of saturation and into sub-threshold operation, resulting in the distortion.

This distortion can be mitigated by operating the transistors at higher overdrive voltages [2], which can be easily achieved in an integrated circuit by changing
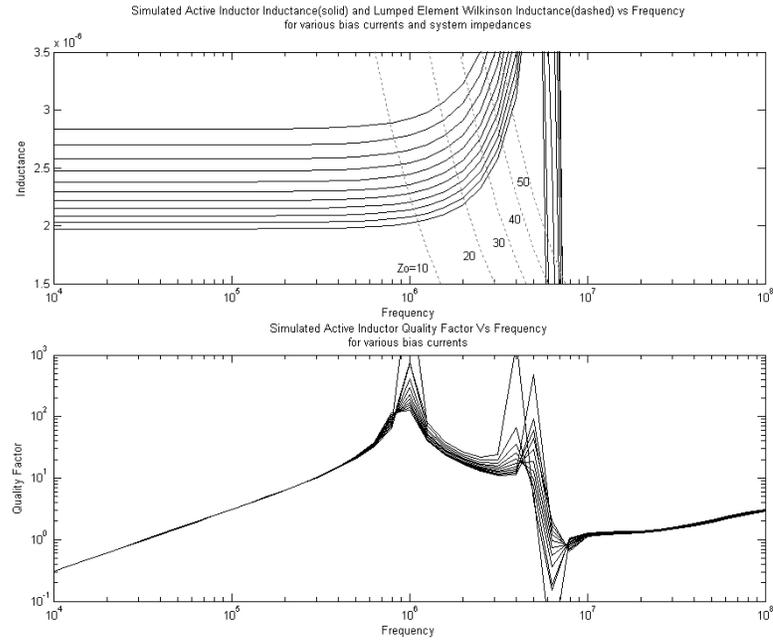
Figure 3.2: Simulation output used to determine optimum AI design point.

transistor sizes, and otherwise re-designing the circuit. Unfortunately this is not possible using discrete transistors. In order to operate discrete transistors at higher overdrive voltages the bias current must also rise, lowering the effective inductance, and forcing either the Wilkinson system impedance to decrease or the operating frequency to increase. To lower the characteristic impedance below 10Ω is difficult, and increasing the frequency of operation much beyond 1MHz makes the system much more sensitive to the parasitic elements that are inescapable on a prototyping board.

The discrete system still works at such low signal levels, but it is much more sensitive to differential offsets and noise than the system would be in a CMOS integrated circuit.

The active inductor is slightly modified for inclusion into the full system as shown in figure 3.3. Resistive biasing is used for simplicity. A $20k\Omega$ emitter degeneration resistor is used to linearize the control voltage to bias current conversion and increase its sensitivity; without the emitter degeneration, small variations in the

control voltage would result in extremely large bias current variations. With the emitter degeneration resistance, the bias current can be effectively determined by Equation 3.1.

$$I_b = \frac{V_{CC} - V_{control} + V_{be}}{R_{emitter}} \approx \frac{V_{CC} - V_{control} - 0.7}{R_{emitter}} \tag{3.1}$$

From [2], the effective inductance of the AI is:

$$L_{eq} = \frac{C_{GS2}}{g_{m1}g_{m2}} = \frac{C_{GS2}}{2\,\text{Kn}\,\sqrt{(\text{W/L})_1\,(\text{W/L})_2\,I_{b1}\,I_{b2}}} \tag{3.2}$$

Substituting equation 3.1 into equation 3.2:

$$L_{eq} = \frac{C_{GS2}}{2\,\text{Kn}\,\sqrt{-\frac{(\text{W/L})_1\,(\text{W/L})_2\,I_{b1}\,(V_{control}-V_{CC}+0.7)}{R_e}}} \tag{3.3}$$

Differentiating equation 3.3 with respect to $V_{control}$ and substituting in nominal values results in the small signal gain $\frac{\partial L_{eq}}{\partial V_{control}} = 0.3517\frac{\mu H}{V}$.
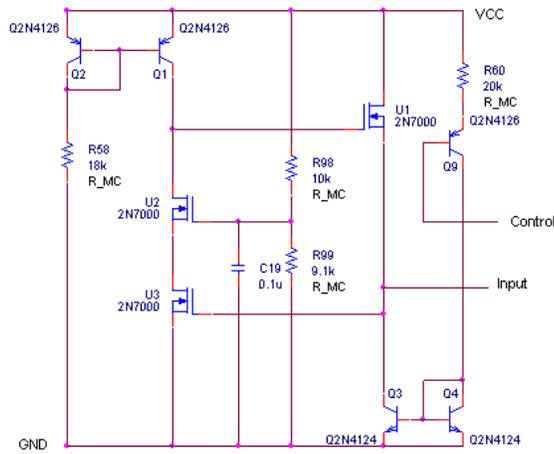

Figure 3.3: Active Inductor schematic with biasing and control input shown.

Wilkinson Power Divider

With the design point chosen, the design of the Wilkinson power divider follows from Equations (reference to Wilkinson design equations). With a design frequency of 1MHz and a system impedance of 10Ω, the required inductance is 2.25μH, and the required capacitance is 11nF. A resistive divider was used on the signal generator to reduce both the source impedance seen by the divider, and the signal level such that the active inductors do not distort.

Using (reference equations from analysis), the small signal gain $\frac{\partial \phi}{\partial L_{eq}} = -17.72 \frac{\text{deg}}{\mu H}$.

Gilbert Cell

The Gilbert cell phase detector is one of the most important components of the design. The transistors of the Gilbert cell must be well matched as described in (refer to gilbert cell analysis section here) in order to prevent mismatch from introducing a phase detection offset. Discrete components cannot be guaranteed to match, so an integrated NPN transistor array, the CA3046, was used for those transistors that require a good match (M5/M6 used one CA3046, and M1-4 used a second). The CA3046 only guarantees matching parameters for two of the five transistors in each package, but all of the transistors will be matched to a certain extent simply because they are on the same die. Figure 3.4 shows the schematic of the Gilbert cell.

The Gilbert cell uses resistor dividers to bias the bipolar transistor bases at the correct voltage levels. The total tail current through the cell is set by the voltage across the tail resistor. The base voltage of the bottom differential pair is set to roughly 1.7V, so that the voltage across the tail resistor will be $\approx$ 1mA.
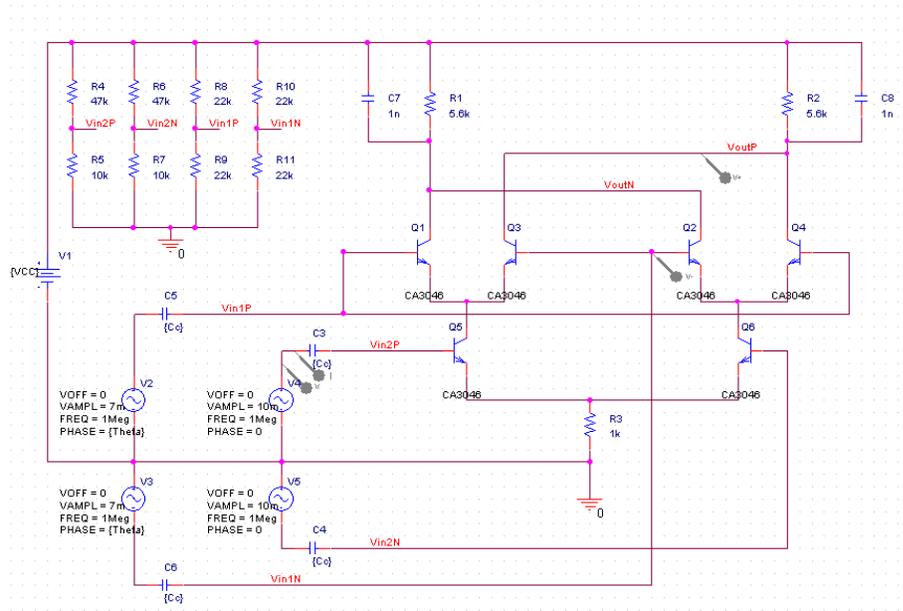
Figure 3.4: Discrete system gilbert cell schematic.

The load resistors are chosen such that the output common mode is roughly halfway between the supply voltage rail and the base voltage of the upper differential pairs. This maximizes the available range of the Gilbert cell output. The load capacitors are chosen to roll off the high frequency signals generated by the phase detector. Multiplication of the inputs will create the phase term of interest at DC, a frequency doubled term at $2 * f_o$, and any offsets will multiply with the inputs to create signals at f_o. Both high frequency terms are unwanted, and need to be highly attenuated so as not to compromise the feedback signal.

Figure 3.5 shows the simulated spectrum of the Gilbert cell differential output voltage with an ideal 90 deg phase shift between input signals. The capacitance of the Gilbert cell load was reduced by a factor of ~ 2200 from the actual design so that the outputs would settle quickly, reducing simulation time. This increases the 3dB corner frequency of the low pass response from $f_{3dB} = \frac{1}{2\pi RC} = 13 Hz$ to $f_{3dB} = \frac{1}{2\pi RC} = 28.4 kHz$. Assuming a normal, first-order, low-pass filter roll-off of

20dB/decade past the corner frequency, the unwanted high frequency components will be reduced by an additional 67dB compared to what is shown in figure 3.5.
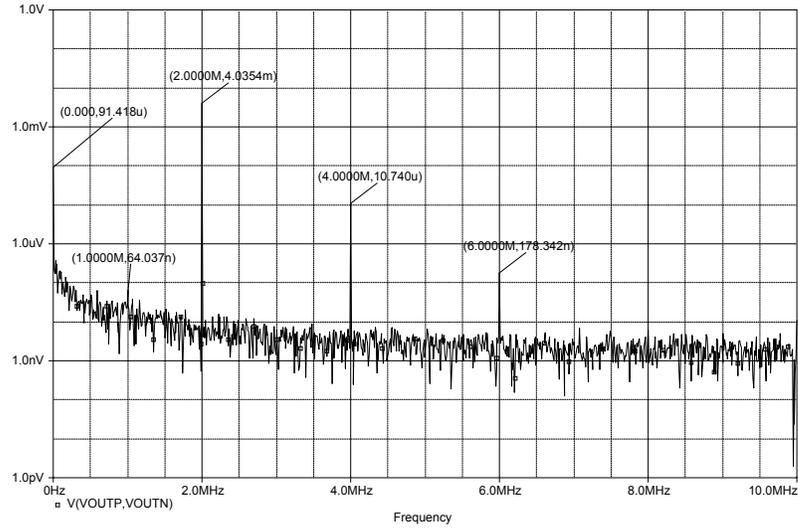

Figure 3.5: FFT of Gilbert cell output showing high frequency components.

The pole introduced by the load resistor and capacitor directly affects the frequency response of the phase term and feedback term, and, therefore, plays a very important role in the feedback stability of the system.
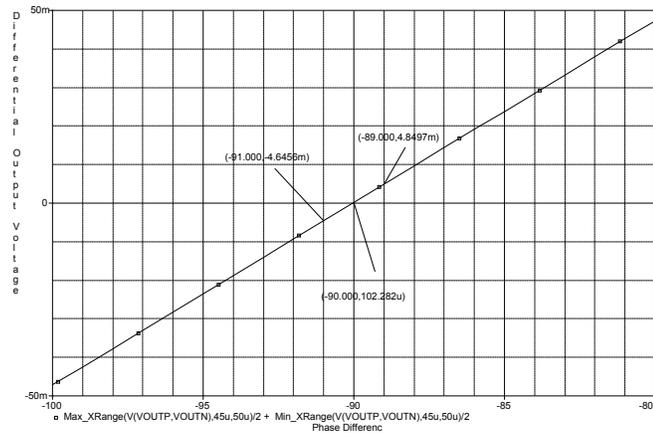

Figure 3.6: Conversion gain of Gilbert cell.

Another important characteristic of the Gilbert cell is the conversion gain. The output term of interest for phase detection is:

$$I_o = A_1 A_2 K_{GC} \cos(\phi) \tag{3.4}$$

Where A_1 and A_2 are the amplitude of the inputs, ϕ is their phase difference, and K_{GC} is the multiplication gain of the Gilbert cell. Linearized around the operating point $\phi = 90$ deg, the actual conversion gain is:

$$K_{conv} = A_1 A_2 K_{GC} \tag{3.5}$$

The simulated conversion gain, as shown in figure 3.6, is $K_{conv} = \frac{102.3\mu V - -4.6456mV}{-90 \text{ deg} - -91 \text{ deg}} = 4.75mV/\text{deg}$ with input amplitudes: $A_1 = 7mV$ and $A_2 = 10mV$. These input amplitudes were chosen to be somewhat representative of the actual input amplitudes that would be seen in the actual circuit; the 3dB difference is due to the 3dB amplitude difference between the Wilkinson input and output, and the absolute amplitudes are for a 1mV reference signal input and 20dB of preamplifier gain. The multiplication gain of the Gilbert cell using the input amplitudes is then: $K_{GC} = \frac{K_{conv}}{A_1 A_2} = 67.8(V \text{ deg})^{-1}$.

Pre-Amplifiers

The preamplifiers need to amplify the signals from the Wilkinson such that they are large enough for the Gilbert cell to have enough phase detection gain. The Wilkinson power divider uses a single-ended design, so the preamplifiers must also convert the single ended signals into differential signals for the phase detector. The preamplifiers for each path need to have an identical phase response, so that a phase offset is not introduced.

A simple resistive load differential pair circuit was chosen for the preamplifiers. Extremely high gain is not required in this application, and the frequency response
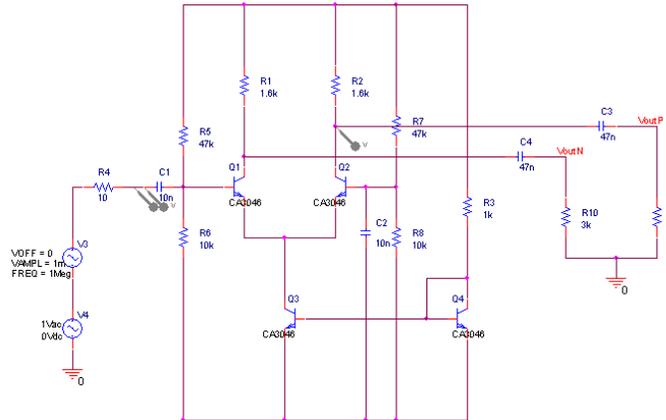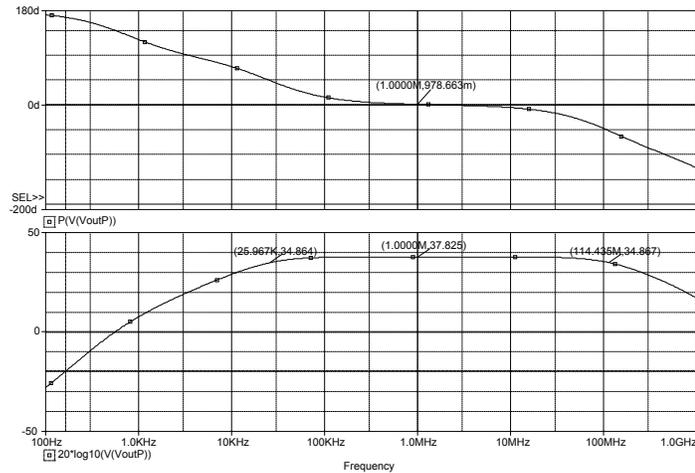
Figure 3.7: Preamplifier schematic.

Figure 3.8: Frequency response of preamplifiers.

necessary is easily achievable using the CA3046 NPN transistor arrays. The bias of the preamps is chosen so that there is little attenuation when loaded by the Gilbert multiplier. The schematic for the preamplifiers is shown in figure 3.7. The single-ended gain and phase for the preamplifiers is shown in figure 3.8. The differential gain is twice the single-ended gain, or $37.825dB + 6dB \approx 44dB \approx 160V/V$.

One issue with using a differential pair to perform a single-ended to differential signal conversion is that the effective common mode input voltage varies with the input. This means that a high common mode rejection ratio is important to

prevent this common mode variation to propagate through the circuit. The single-ended common mode rejection ratio (CMRR) is simulated to be $\sim$64dB. The ideal differential CMRR is infinite, but any mismatches will introduce a common-mode to differential conversion and reduce the CMRR. Because any common mode signals that are generated here also have to pass through another differential circuit, the Gilbert cell, they will likely be highly attenuated before the differential to single-ended conversion is performed by the instrumentation amplifier, and not disrupt the proper operation of the control system.

Instrumentation Amplifier

An instrumentation amplifier is used to amplify the phase detector output and provide the control voltage feedback to the active inductor. The instrumentation amplifier topology was chosen because it balanced input impedance, high CMRR, and the gain can easily be changed. The schematic for the instrumentation amplifier is shown in figure 3.9. The LM324 Quad Opamp was used because of its availability.
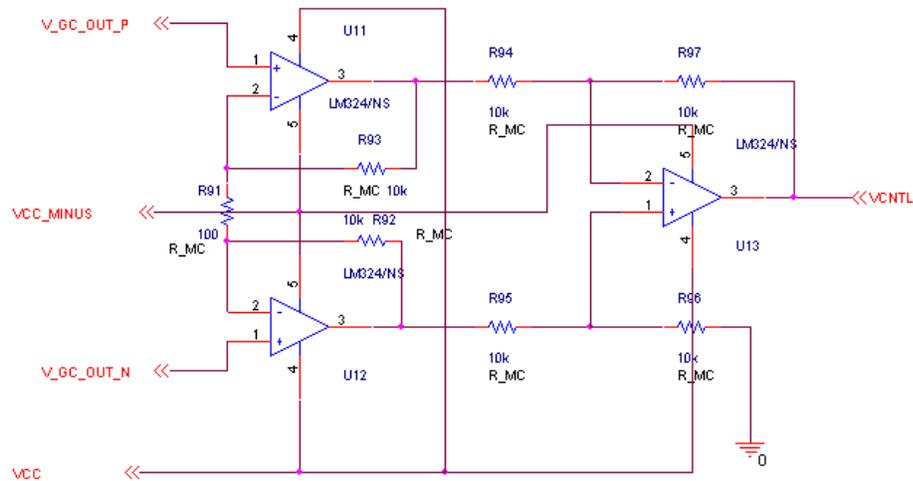

Figure 3.9: Schematic of instrumentation amplifier used to generate feedback term.

Along with the LPF load of the Gilbert cell, the poles of the instrumentation amplifier also directly impact the frequency response of the feedback term, and therefore must also be taken into account when analyzing the stability of the system. As long as the output opamp, U13 in figure 3.9, has low gain (unity gain in most cases), the instrumentation amplifier configuration has a dominant pole determined by the feedback configuration of the two input amplifiers (U11 and U12 in figure 3.9). The dominant pole can be approximated by dividing the gain-bandwidth product of the opamp by the equivalent non-inverting gain of the input opamp feedback network (Equation 3.6)

$$f_p = \frac{GBW}{1 + \frac{R_{93}}{R_{91}/2}} \tag{3.6}$$

Full System

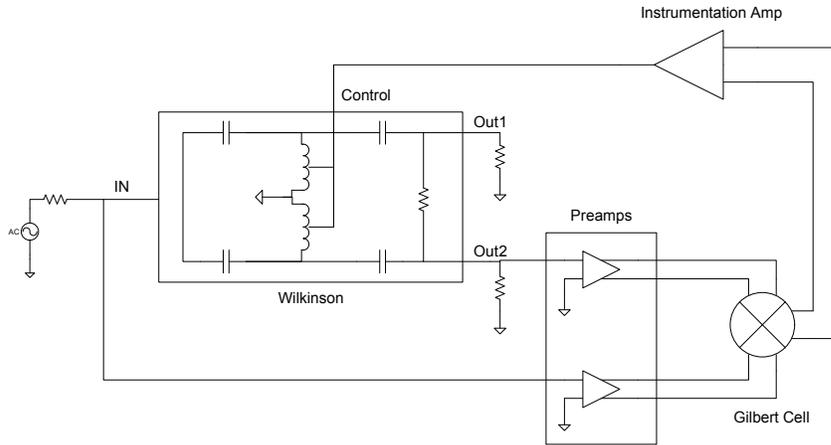A block diagram for the full system is shown in figure 3.10.

Figure 3.10: Full discrete system block diagram.

Using the relationships determined for each of the system blocks, the full loop stability of the system can be analyzed. Equation 3.7 is used to calculate DC loop gain.

$$K_{tot} = (K_{AI}\ \frac{\mu H}{V}) * (K_{Wilk}\ \frac{\text{deg}}{\mu H}) * (A_1 A_2 K_{GC}\ \frac{V}{\text{deg}}) * (K_{Inst-Amp}\ \frac{V}{V}) \qquad (3.7)$$

Where A_1 and A_2 are the amplitudes of the Gilbert cell input waveforms, which can be found using Equations 3.8 and 3.9.

$$A_1 = A_{V_{in}} A_{Preamp} = \frac{1}{2} A_{V_s} A_{Preamp} \qquad (3.8)$$

$$A_2 = 0.707 * A_{V_{in}} A_{Preamp} = \frac{1}{2} 0.707 * A_{V_s} A_{Preamp} \qquad (3.9)$$

Substituting in the gains found for each block and a source amplitude of 1mV the loop gain can be calculated to be: $K_{tot} = -1.912 * K_{Inst-Amp}$. Using the locations of the poles, the open loop transfer function can be found (Equation 3.10).

$$G(s) = \frac{-1.912 * K_{Inst-Amp}}{(\frac{s}{p_1} - 1)(\frac{s}{p_2} - 1)} \qquad (3.10)$$

Where p_1 is the pole defined by the Gilbert cell RC load: $p_1 = \frac{1}{RC}$; and p_2 is the pole resulting from the instrumentation amplifier: $p_2 = 2\pi \frac{GBW}{Gain}$. Substituting in values for the designed gain of the instrumentation amplifier, $201 \frac{V}{V}$, and the gain-bandwidth product of the LM324, 1MHz, the closed loop system has a phase margin of 53 deg. The Gilbert cell pole was chosen by using the standard value capacitor that gave the fastest system rise time without a noticeable overshoot as shown in figure 3.11.
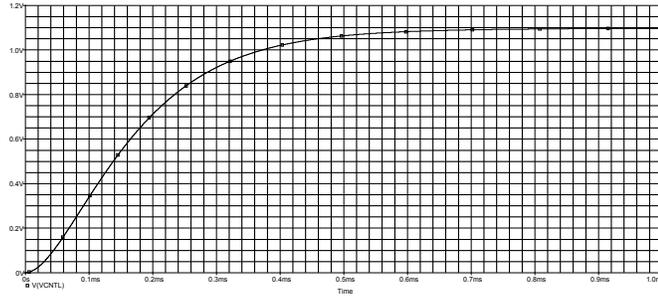
Figure 3.11: Simulation of closed loop step response.

Simulation Results

Next the full system was simulated over a variety of temperature and supply voltage conditions to compare the controlled and uncontrolled active inductor responses.

Figure 3.12(a) shows the simulated variation of controlled and uncontrolled inductances for various supply voltages. The controlled inductance shows much less variation than the uncontrolled case, although the control scheme appears to fail at voltages lower than 8V. The control scheme failed due to the saturation of the instrumentation amplifier: the required control voltage for supply voltages less than 8V would be below the negative supply rail (ground).

Figure 3.12(b) shows the simulated quality factor versus supply voltage. In figure 3.12(b), the uncontrolled Q tends to be much higher than the controlled Q. This is due to the fact that the control variable, the Wilkinson phase output, has a much higher dependence on the inductance than the quality factor. This means that the control loop will tend to correct the AI inductance at the expense of the quality factor. If a high quality factor is needed, it must either be carefully designed into the active inductor so that the control loop will not affect it, or a different control scheme chosen.
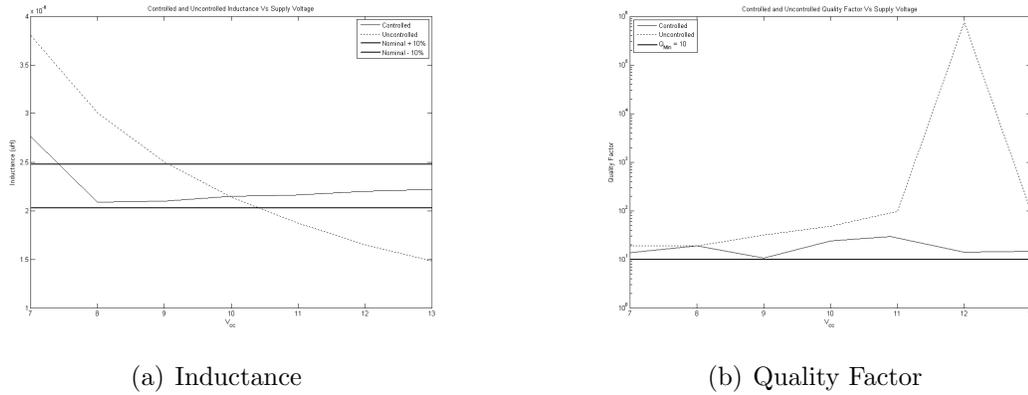
(a) Inductance

(b) Quality Factor

Figure 3.12: Simulated controlled and uncontrolled active inductor parameters versus supply voltage.

Figure 3.13(a) shows controlled and uncontrolled AI inductances versus temperature. The controlled inductance stays within a tight tolerance for wide range of temperatures. Above ~ 85℃, the control loop does not lock, and the inductance exceeds the tolerances (in this case +/- 10%). Again, the control loop failure is due to the required control voltage being outside of the range of the instrumentation amplifier output.

Figure 3.13(b) shows the AI quality factor versus temperature. Again, the quality factor is not controlled by the loop, so the controlled quality factor is much lower than the uncontrolled quality factor.

Monte Carlo simulations were also performed to determine the sensitivity of the control loop to component parameter variations. This requires manually entering device parameter tolerances for the various devices and their parameters. In PSPICE Monte Carlo simulations, there are two different types of tolerances, lot tolerances and device tolerances. Lot tolerances change a model parameter for all devices in each simulation run, and device tolerances change a model parameter for each individual device in each simulation run. This means that device parameters with large lot
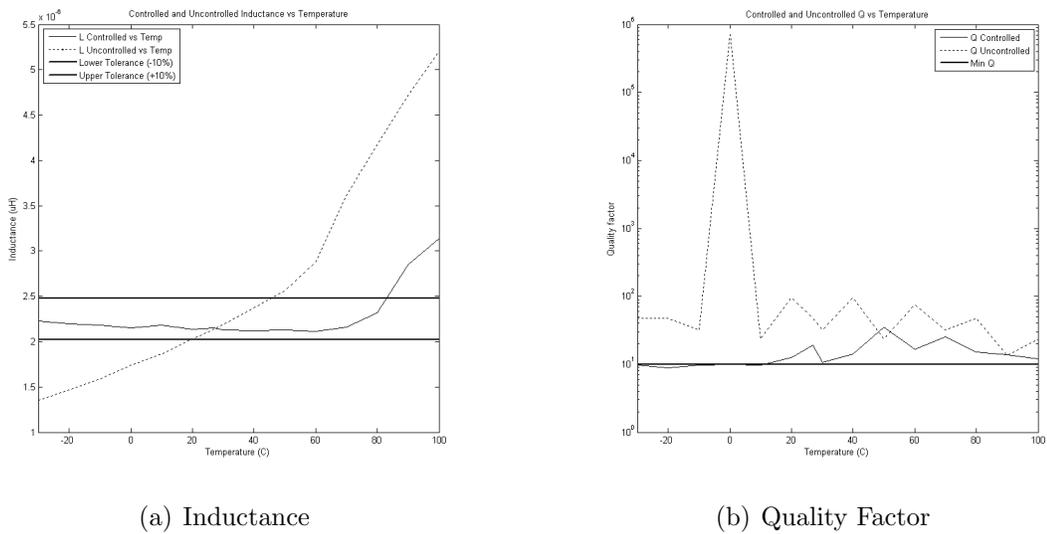
(a) Inductance   (b) Quality Factor

Figure 3.13: Simulated controlled and uncontrolled active inductor parameters versus temperature.

tolerances and small device tolerances will have large variations run to run, but that the differences between individual devices will be small. Lot tolerances are, therefore a good way to simulate things like parameter variation due to large scale process variations, temperature effects, etc, while device tolerances are good for simulating device mismatch.

Through many Monte Carlo simulations, the simulated control loop was found to be very insensitive to large lot tolerances, while also very sensitive to device tolerances, especially in the Gilbert cell circuit.

As shown in figure 3.4, the Gilbert cell inputs are biased at a DC voltage using resistor dividers. If these resistor dividers are mismatched, a differential offset is introduced to the output of the Gilbert cell, resulting in a DC phase error. Because the output of the preamplifiers is less than 100mV, these mismatches can easily overwhelm the Gilbert cell phase output, and the offsets can even force the feedback amplifier into saturation if they are large enough.

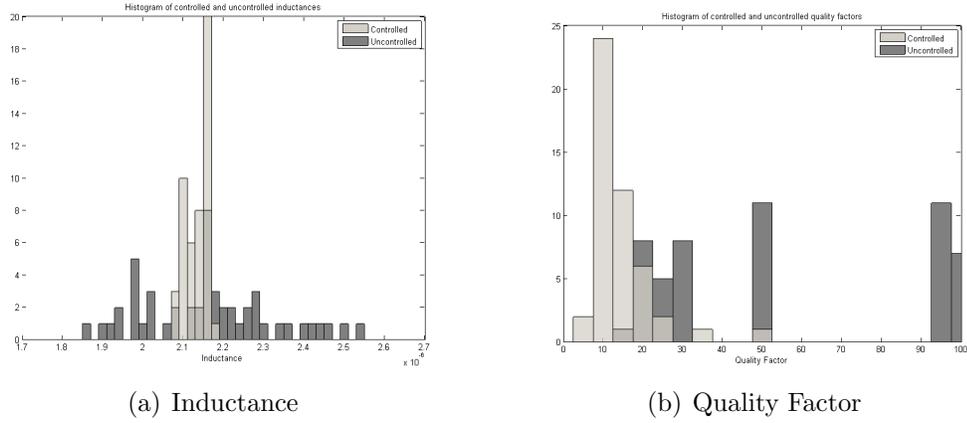(a) Inductance   (b) Quality Factor

Figure 3.14: Inductance and quality factor histograms with high lot tolerances and low device tolerances

In order to provide more realistic modeling for a simulated integrated circuit application, large device tolerances were reduced to very small values and large lot tolerances were introduced to simulate high large scale process variations and good on-chip matching. Figure 3.14 shows AI parameter histograms with these tolerances. Tolerance parameters for this Monte Carlo simulation are shown in table 3.1.

Device	Model Parameter	Lot Tolerance	Device Tolerance
	VT0	50%	1%
2N7000	CGS0	30%	0.5%
	KP	20%	0.5%
2N4124	BF	5%	
2N4126	BF	5%	
CA3046	BF	10%	
Low Tol R	R		
High Tol R	R		5%

Table 3.1: Monte Carlo tolerance parameters used in figure 3.14

Figure 3.14 shows very low quality factors for the controlled versus uncontrolled case. This is due to the control system sacrificing quality factor to control the inductance, because the quality factor has very little impact on the phase of

the Wilkinson divider (see section 2). If this system were being implemented in an integrated circuit, care must be taken to ensure that the quality factor of the active inductor will remain high when controlled.

Demo Results

The discrete system was then built on a solderless breadboard to test its performance. A photograph of the completed system is shown in figure 3.15.
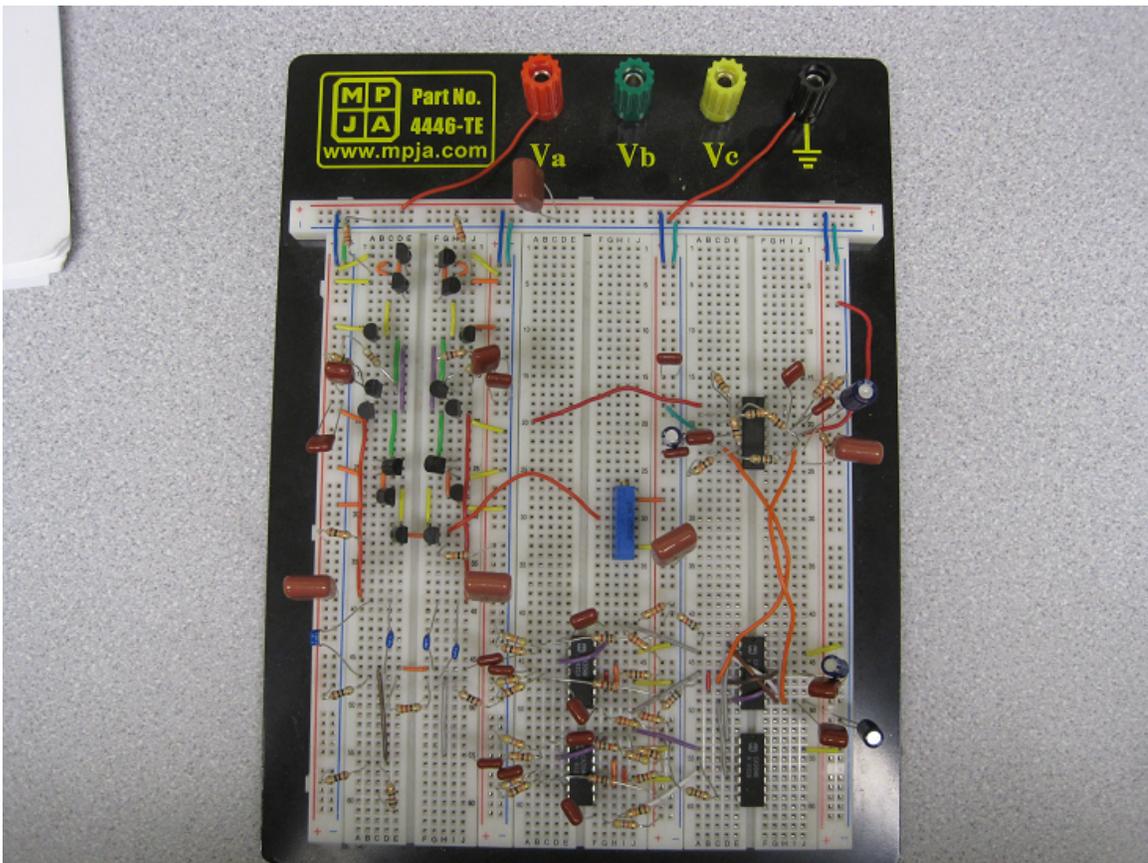

Figure 3.15: Photograph of completed demonstration system.

Using this system, it is effectively impossible to directly measure the controlled active inductor inductance to verify circuit operation because of the extremely small signal levels involved:

- Using a slave active inductor is not feasible due to discrete device mismatches and the necessity of measuring extremely small voltages and currents (the AI distorts at input voltages much over 1mV), and

- directly measuring the inductance of the active inductors in the Wilkinson divider itself is also not feasible because of the small signal levels and the lack of a way to measure the current without disrupting circuit operation.

Because the inductance cannot be directly measured, other, more easily measurable, signals must be recorded, and the circuit's performance derived from them.

The phase of the preamplifier outputs was measured because this signal is the most directly affected by the active inductors. The signals are recorded after the preamplifiers because the signal levels before the preamplifiers are too small ($<$1mV) to be easily measurable without amplification. Equation (reference equation in analysis section here) shows the relationship between the Wilkinson divider phase and AI inductance, so the inductance can be calculated from the phase difference that is measured. Figure 3.16 shows an ideal phase difference of 90 deg at the output of the preamplifiers, indicating that the active inductor has the correct inductance (the control voltage was manually set using a potentiometer for this test).

Unfortunately, it is very difficult to use the phase signal to look at the transient response of the system. The phase must be measured using the averaging function of the oscilloscope to remove any noise, and the system must therefore be kept stable while measuring the phase. The easiest way to measure the transient response of the system is to measure the control voltage. There are two possible circuit startup
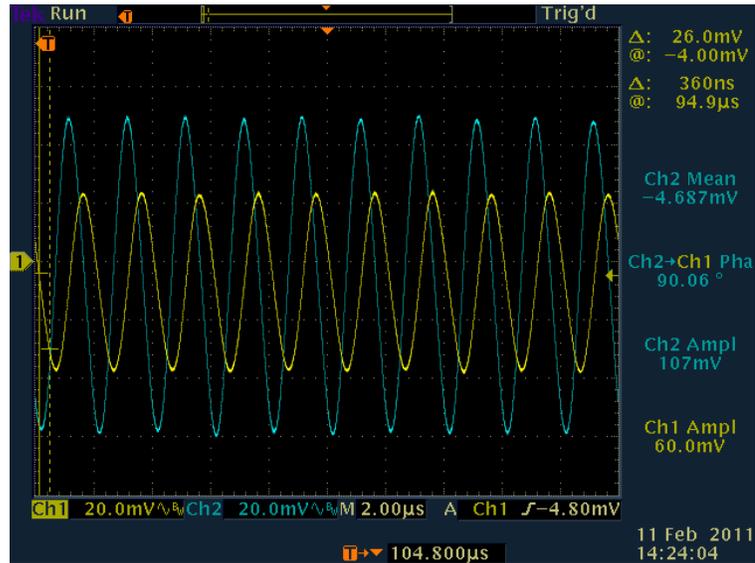
Figure 3.16: Oscilloscope screen capture showing ideal phase relationship between input signal and Wilkinson output.

sequences: apply the reference signal first, then power up the control system, or power up first, then apply the reference signal. Figure 3.17(a) shows the power up transient that occurs when power is applied with the reference signal already on. Figure 3.17(b) shows the startup transient that occurs when the reference signal is applied after the circuit is powered up.

The waveform in figure 3.17(a) shows a response that approximates a ramp and has no overshoot. This waveform shape is likely due to the way the power supply ramps its output voltage. Figure 3.17(b) appears to be closer to an ideal step response, showing a 15-20% overshoot that is indicative of a slightly underdamped system. This fits well with the calculated phase margin of 53°, although it is more underdamped than the simulated control voltage in figure 3.11.

The circuit was tested against variations in supply voltage. For the uncontrolled case, the control voltage was connected to a potentiometer which was then tuned such that the measured phase difference was a nominal 90°at the nominal supply
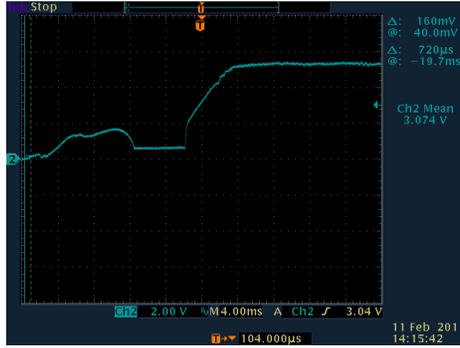
(a) Reference signal startup before control system startup.
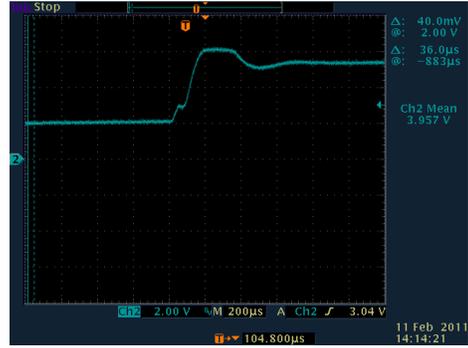
(b) Control system power-up before reference signal.

Figure 3.17: Control voltage transients observed on startup.

voltage (10V). Figure 3.18 shows the measured phase relationships for the controlled and uncontrolled cases. The calculated percent deviation is determined by dividing the phase difference by the $0.4\frac{\text{deg}}{\%\ \Delta L}$ found in (refer to analysis equation here). The uncontrolled case shows that the measured phase, and, therefore, the inductance of the active inductor varies significantly over the supply voltage range. The controlled case shows very little variation over the measured supply voltage range. There is, however, a significant offset in the controlled case. Section 2 showed that the control system is extremely sensitive to offsets in the Gilbert cell, and normal, 5% tolerance resistors were used to bias the Gilbert cell inputs. The likely cause of the offsets is, therefore, probably a result of offsets in the DC bias of the Gilbert cell inputs due to the use of 5% tolerance resistors (section 3 notes the sensitivity of the simulated control scheme to these resistors as well).

Because the use of a potentiometer to generate the control voltage for the uncontrolled case, the control voltage will follow the supply voltage to a certain extent. This actually reduces the amount that the bias current will vary with supply voltage, than if a simple resistively biased current mirror was used, as is the case in
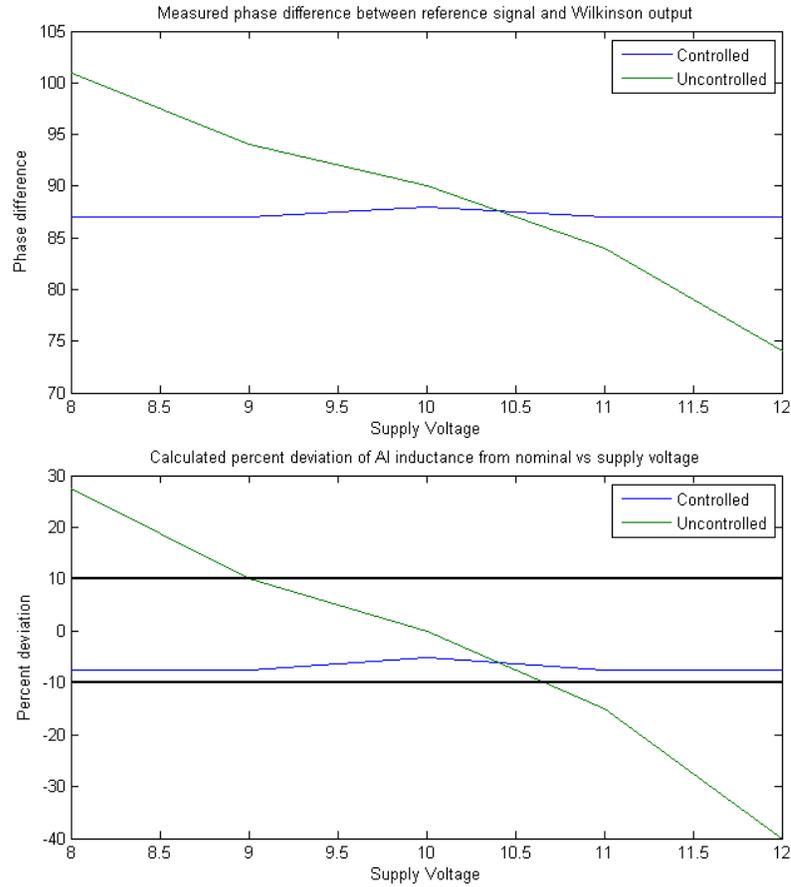
Figure 3.18: Measured phase and deviation from nominal inductance versus supply voltage.

the simulations performed in section 3. A fully uncontrolled AI would actually vary more than was measured. A potentiometer tuned to a nominal control voltage was used to simplify the process of getting each of the two individual active inductors tuned correctly for nominal conditions, even though the use of the potentiometer reduces the uncontrolled active inductor's observed variability.

Temperature variations could not be investigated due to the lack of an available controlled temperature environment and the unknown characteristics of the solderless breadboard.

Due to the use of a solderless breadboard, components can easily be replaced, and the effect on the system recorded. The transistor M1 in each active inductor was replaced by a transistor made by a different manufacturer. When the control loop was active, no measurable change in the phase recorded. When the control voltage was supplied by the potentiometer, the phase changed by over $3\,\mathrm{deg}$, or an inductance variation of roughly 7.5%. This component replacement simulates the effects of process variations, and the recorded controlled and uncontrolled phase changes show that these simulated process variations had no effect on the controlled active inductor, while an uncontrolled active inductor would have significant inductance variation.

CONCLUSION

An improved control system for PVT compensation of CMOS active inductors was introduced. The design of the control system was analyzed, including sensitivity to various design parameters. A low-frequency discrete version of the active inductor and control scheme was designed, simulated, built, and tested. The ability of the discrete version to compensate the active inductor for various temperature and supply voltage variations was demonstrated in simulation, and Monte Carlo simulations that show that the discrete version is also robust to changes in component model variations, similar to process variations in an integrated circuit. The completed discrete system was tested against supply voltage variations and simulated process variations (replacement of individual components), and was able to compensate the active inductor over a wide range of supply voltage variations and all tested simulated process variations. The control system presented here is a excellent candidate for the PVT compensation that is required for active inductor use in commercial devices.

Future Work

Verify System on IC

Although this work shows that the improved compensation scheme is viable, it needs to be designed, simulated, fabricated, and verified on an actual integrated circuit over a full range of PVT variations to show that it will work in that environment. It is likely that the compensation scheme presented in this work will perform better in an integrated circuit environment due to the increased ability to match components. There should be no surprises found in a fabricated IC as all the components needed are well known analog components, and Bucossi [5] demonstrated that the fabricated

behavior of both the lumped element Wilkinson divider and the simple cascoded active inductor match simulation results.

Noise Performance

The noise performance of the active inductor topology used for this work was not investigated. The active devices used in the active inductor will generate noise, and the impact of this noise on both the compensation system and the actual application needs to be taken into account when making the decision to use an active inductor and the necessary compensation scheme. And, because this active inductor topology (SCAI) has been shown to distort at fairly low signal levels (75mVpp), the noise generated by the active inductor could severely reduce the available dynamic range of the device.

Other Active Inductor Configurations

Although this work focused on the simple cascoded active inductor (SCAI) configuration, many other active inductor configurations are possible. The control system presented here should be able to compensate any active inductor configuration, provided that it is tunable, with minor changes to the way that the control voltage is used to tune the active inductor itself. Other active inductor configurations may have better noise performance or have more dynamic range, or may just be more suited to different applications.

AI Compensation Schemes for Other Applications

This work, and the work of Lyson [4] and Bucossi [5], focused on the application of the active inductor in a lumped element Wilkinson configuration. Although the compensation scheme presented here is applicable to any active inductor application,

other compensation systems may be better suited to different applications that have different requirements on AI behavior, whether inductance, quality factor, etc. The analysis presented in section 2 of this work should be enough to determine if this compensation scheme is right for the application that is being considered, with its particular requirements, and the process being used, with its particular limitations.

REFERENCES CITED

[1] A. Thanachayanont, A. Payne. VHF CMOS integrated active inductor. *Electronics letters*, 32:999, 1996.

[2] H.H. Hsieh, L.H. Lu. A compact quadrature hybrid MMIC using CMOS active inductors. *Microwave Theory and Techniques, IEEE Transactions on*, 55(6):1098–1104, 2007.

[3] L.H. Lu, C.R. Wu. A miniaturized Wilkinson power divider with CMOS active inductors. *Microwave and Wireless Components Letters, IEEE*, 15(11):775–777, 2005.

[4] Kyle J Lyson. On-chip automatic tuning of cmos active inductors for use in radio frequency integrated circuit (rfic) applications. Master's Thesis, Montana State University - Bozeman, 2006.

[5] William Bucossi. Process voltage temperature compensated on-chip cmos active inductors for wilkinson power dividing applications. Master's Thesis, Montana State University - Bozeman, 2008.

[6] W. Bucossi, J.P. Becker. Practical considerations in the use of cmos active inductors. *Silicon Monolithic Integrated Circuits in RF Systems, 2008. SiRF 2008. IEEE Topical Meeting on*, pages 90 –93, jan. 2008. `doi:10.1109/SMIC.2008.29`.

[7] B. Gilbert. A precise four-quadrant multiplier with subnanosecond response. *Solid-State Circuits, IEEE Journal of*, 3(4):365 – 373, dec 1968. `doi:10.1109/JSSC.1968.1049925`.

[8] Adel S Sedra, Kenneth C Smith. *Microelectronic Circuits*. Oxford University Press, edition fifth, 2004.

[9] R.J. Baker. *CMOS: Circuit design, layout, and simulation*. Wiley-IEEE Press, 2008.

[10] Paul R Gray, Paul J Hurst, Stephen J Lewis, Robert G Meyer. *Analysis and Design of Analog Integrated Circuits*. Wiley, edition fifth, 2009.

APPENDICES

<u>APPENDIX A</u>

SYMBOLIC MATH ANALYSIS CODE

Wilkinson Analysis

Analysis of ideal Wilkinson divider

```
Vo_1  :=  Io_1*Zo
Vo_1  :=  subs(Vo_1,Io_1=V_B/(1/(s*C) + Zo))
Vo_1  :=  subs(Vo_1,V_B=I_B*(1/(L*s) + 1/(1/(s*C)+Zo))^(-1))
Vo_1  :=  subs(Vo_1,I_B=V_A/(1/(s*C) + (1/(L*s)+1/(1/(s*C)+Zo))
    ^(-1)))
Vo_1  :=  simplify(expand(subs(Vo_1,s = I*w)/V_A))
assume(L,  Type::Real):  assume(C,Type::Real):  assume(w,Type::Real)
    :  assume(Zo,  Type::Real)
simplify(Im(Vo_1)/Re(Vo_1))
angle  :=  arctan(Im(Vo_1)/Re(Vo_1))
dangle_dL  :=  simplify(diff(angle,L))
```

```
Find  the  change  in  output  angle  (in  degrees)  for  a  1%  change  in  L
    at  the  design  point
subs(dangle_dL*L,C=1/(sqrt(2)*w*Zo),L=sqrt(2)*Zo/w,Zo=10,w=
    1000000)*0.01*180/PI
```

```
float(-(0.9*2^(1/2))/PI)
```

```
dangle_dC  :=  simplify(diff(angle,C))
float(subs(dangle_dC*C,C=1/(sqrt(2)*w*Zo),L=sqrt(2)*Zo/w,Zo=10,w=
    1000000)*0.01*180/PI)
```

```
subs(dangle_dC*C,C=1/(sqrt(2)*w*Zo),L=sqrt(2)*Zo/w)
```

Analysis of AI equivalent circuit component effects on Wilkinson divider assuming matched components

```
Vo_1 := Io_1*Zo
Vo_1 := subs(Vo_1,Io_1=V_B/(1/(s*C) + Zo))
Vo_1 := subs(Vo_1,V_B=I_B*(1/(s*C_p + 1/R_p + 1/(L_e_q*s + R_s))
    ^(-1) + 1/(1/(s*C)+Zo))^(-1))
Vo_1 := subs(Vo_1,I_B=V_A/(1/(s*C) + (1/(s*C_p + 1/R_p + 1/(L_e_q
    *s + R_s))^(-1)+1/(1/(s*C)+Zo))^(-1)))
Vo_1 := Vo_1/V_A
Vo_1 := simplify(subs(Vo_1,s=I*w))
assume(L_e_q, Type::Positive): assume(C,Type::Positive): assume(w
    ,Type::Positive): assume(Zo, Type::Positive):
assume(C_p, Type::Positive): assume(R_s,Type::Real): assume(R_p,
    Type::Positive)
tf_im := Im(Vo_1)
angle := simplify(arctan(Im(Vo_1)/Re(Vo_1)))
dangle_dL := simplify(diff(angle,L_e_q))
```

```
Find the change in output angle (in degrees) for a 1% change in L
    at the design point
float(simplify(subs(dangle_dL*L_e_q,C_p=0.0*C,R_s=0,R_p=100000,C=
    1/(sqrt(2)*w*Zo),L_e_q=sqrt(2)*Zo/w,Zo=50))*0.01*180/PI)
```

```
float ( subs ( dangle_dL , C_p=0.1*10^(−9) ,Q=1000,C=1/( sqrt (2) *w*Zo) ,
    L_e_q=sqrt (2) *Zo/w, Zo=10 ,w=2*PI *10^6) *10^(−6) *180/ PI )
```

```
dangle_dCp  :=  simplify ( diff ( angle , C_p ) )
```

```
float ( simplify ( subs ( dangle_dCp *C_p , C_p=0.1*C, R_s=2 ,R_p=1000,C=1/(
    sqrt (2) *w*Zo) , L_e_q=sqrt (2) *Zo/w, Zo=10) ) *0.01*180/ PI )
```

```
dangle_dRs  :=  simplify ( diff ( angle , R_s ) )
```

```
float ( simplify ( subs ( dangle_dRs , C_p=0.1*C, R_s=5 ,R_p=1000,C=1/( sqrt
    (2) *w*Zo) , L_e_q=sqrt (2) *Zo/w, Zo=50) ) *0.05*180/ PI )
```

```
dangle_dRp  :=  simplify ( diff ( angle , R_p ) )
```

```
float ( simplify ( subs ( dangle_dRp *R_p , C_p=0.1*C, R_s=1 ,R_p=1000,C=1/(
    sqrt (2) *w*Zo) , L_e_q=sqrt (2) *Zo/w, Zo=50) ) *0.01*180/ PI )
```

Analysis of mismatched inductances on Wilkinson divider

```
Clear  variables  and  make  assumptions  on  all  component  values :
```

```
delete  Z_o , C_1 , C_2 , C_3 , C_4 , V_o_1 , V_o_2 , V_A , V_B , V_C , Z_L_1 , Z_L_2 ,
    L_e_q_1 , L_e_q_2 , C_p_1 , C_p_2 , R_s_1 , R_s_1 ,C,w,dZ_o , R_p_1 , R_p_2
```

```
assume ( Z_o , Type :: Real ) ; assume ( C_1 , Type :: Real ) ; assume ( C_2 , Type ::
    Real ) ; assume ( C_3 , Type :: Real ) ; assume ( C_4 , Type :: Real ) ;  assume (
    dZ_o , Type :: Real )
```

assume (L_e_q_1 , Type :: Real) ; assume (L_e_q_2 , Type :: Real) ; assume (
    C_p_1 , Type :: Real) ; assume (C_p_2 , Type :: Real) ; assume (R_s_1 , Type ::
    Real) ; assume (R_s_2 , Type :: Real) ;

assumeAlso (L_e_q_1 , Type :: Positive) ; assumeAlso (L_e_q_2 , Type ::
    Positive) ; assumeAlso (C_p_1 , Type :: Positive) ; assumeAlso (C_p_2 ,
    Type :: Positive) ; assumeAlso (dZ_o , Type :: Positive) ;

assumeAlso (Z_o , Type :: Positive) ; assumeAlso (C_1 , Type :: Positive) ;
    assumeAlso (C_2 , Type :: Positive) ; assumeAlso (C_3 , Type :: Positive) ;
    assumeAlso (C_4 , Type :: Positive) ;

assume (R_p_1 , Type :: Positive) ; assume (R_p_2 , Type :: Positive) ;

assume (C, Type :: Real) ; assumeAlso (C, Type :: Positive) ; assume (w, Type ::
    Real) ; assumeAlso (w, Type :: Positive) ;

Sum **of** all currents flowing out **of** Vo1 :

Node_Vo1 := 0= V_o_1 / (Z_o) + (V_o_1−V_o_2) / (2∗Z_o) + (V_o_1−V_B)
    / (1 / (**I** ∗w∗C_3))

Node_Vo2 := 0= V_o_2 / Z_o + (V_o_2−V_o_1) / (2∗Z_o) + (V_o_2−V_C)
    / (1 / (**I** ∗w∗C_4))

Node_V_B := 0=(V_B−V_o_1) / (1 / (**I** ∗w∗C_3)) + V_B / (Z_L_1) + (V_B−V_A)
    / (1 / (**I** ∗w∗C_1))

solve(Node_V_B,V_B)

V_B := (C_1*V_A*w*I + C_3*V_o_1*w*I)/(C_3*w*I + 1/Z_L_1 + C_1*w*I
)

Node_V_C := 0=(V_C−V_o_2)/(1/(I*w*C_4)) + V_C/(Z_L_2) + (V_C−V_A)
     /(1/(I*w*C_2))

solve(Node_V_C,V_C)

V_C := (C_2*V_A*w*I + C_4*V_o_2*w*I)/(C_4*w*I + 1/Z_L_2 + C_2*w*I
)

Node_Vo2

solve(Node_Vo2,V_o_2)

V_o_2 := (V_o_1/(2*Z_o) − (C_2*C_4*V_A*w^2)/(C_4*w*I + 1/Z_L_2 +
     C_2*w*I))/(3/(2*Z_o) − C_4*w*(− 1 + (C_4*w*I)/(C_4*w*I + 1/
     Z_L_2 + C_2*w*I))*I)

Node_Vo1

solve(Node_Vo1,V_o_1)

```
TF_Vo1_Va := ((C_1*C_3*V_A*w^2)/(C_3*w*I + 1/Z_L_1 + C_1*w*I) + (
    C_2*C_4*V_A*w^2)/(2*Z_o*(3/(2*Z_o) - C_4*w*(- 1 + (C_4*w*I)/(
    C_4*w*I + 1/Z_L_2 + C_2*w*I))*I)*(C_4*w*I + 1/Z_L_2 + C_2*w*I)
    ))/((1/(2*Z_o*(3/(2*Z_o) - C_4*w*(- 1 + (C_4*w*I)/(C_4*w*I +
    1/Z_L_2 + C_2*w*I))*I)) - 1)/(2*Z_o) - 1/Z_o + C_3*w*(- 1 + (
    C_3*w*I)/(C_3*w*I + 1/Z_L_1 + C_1*w*I))*I)/V_A

TF_Vo1_Va := simplify(subs(TF_Vo1_Va,C_1=C,C_2=C,C_3=C,C_4=C))
Z_L_1 := simplify(1/(1/(L_e_q_1*I*w + R_s_1) + 1/R_p_1 + 1/(1/(
    C_p_1*I*w))))

Z_L_2 := simplify(1/(1/(L_e_q_2*I*w + R_s_2) + 1/R_p_2 + 1/(1/(
    C_p_2*I*w))))

TF_Vo1_Va_simp := combine(simplify(combine(TF_Vo1_Va))):
Im_TF := Im(TF_Vo1_Va_simp):

Re_TF := Re(TF_Vo1_Va_simp):

Angle_Vo1_Va := arctan(Im_TF/Re_TF):

Mag_Vo1_Va := sqrt(Re_TF^2 + Im_TF^2):

float(simplify(subs(Angle_Vo1_Va,R_s_1=0,R_s_2=0,R_p_1=10000,
    R_p_2=10000,C_p_1=0,C_p_2=0,L_e_q_1=sqrt(2)*Z_o/w,L_e_q_2=sqrt
    (2)*Z_o/w,C=1.1/(sqrt(2)*Z_o*w),Z_o=10))*180/PI)
```

```
dangle_dL1 := diff(Angle_Vo1_Va, L_e_q_1):


float(subs(dangle_dL1*L_e_q_1, R_s_1 = 0, R_s_2 = 0, C=1/(sqrt(2)*
    Z_o*w), L_e_q_1=sqrt(2)*Z_o/w, L_e_q_2=sqrt(2)*Z_o/w, C_p_1=
    0.01*1/(sqrt(2)*Z_o*w), C_p_2=0.01*1/(sqrt(2)*Z_o*w))
    *0.01*180/PI)


dangle_dL2 := diff(Angle_Vo1_Va, L_e_q_2):


float(subs(dangle_dL2*L_e_q_2, R_s_1 = 0, R_s_2 = 0, C=1/(sqrt(2)*
    Z_o*w), L_e_q_1=sqrt(2)*Z_o/w, L_e_q_2=sqrt(2)*Z_o/w, C_p_1=
    0.01*1/(sqrt(2)*Z_o*w), C_p_2=0.01*1/(sqrt(2)*Z_o*w))
    *0.01*180/PI)


dangle_dCp1 := diff(Angle_Vo1_Va, C_p_1):


float(subs(dangle_dCp1*C_p_1, R_s_1 = 0, R_s_2 = 0, C=1/(sqrt(2)*
    Z_o*w), L_e_q_1=sqrt(2)*Z_o/w, L_e_q_2=sqrt(2)*Z_o/w, C_p_1=
    0.01*1/(sqrt(2)*Z_o*w), C_p_2=0.01*1/(sqrt(2)*Z_o*w))
    *0.01*180/PI)


dangle_dCp2 := diff(Angle_Vo1_Va, C_p_2):


dangle_dC := diff(Angle_Vo1_Va, C):


dangle_dRs1 := diff(Angle_Vo1_Va, R_s_1):
```

```
dangle_dRs2  :=  diff(Angle_Vo1_Va,R_s_2):


float(subs(dangle_dCp2*C_p_2,R_s_1 = 0,  R_s_2 = 0,  C=1/(sqrt(2)*
    Z_o*w),L_e_q_1=sqrt(2)*Z_o/w,L_e_q_2=sqrt(2)*Z_o/w,C_p_1=
    0.01*1/(sqrt(2)*Z_o*w),  C_p_2=0.01*1/(sqrt(2)*Z_o*w))
    *0.01*180/PI)


float(subs(dangle_dC*C,R_s_1 = 0,  R_s_2 = 0,  C=1/(sqrt(2)*Z_o*w),
    L_e_q_1=sqrt(2)*Z_o/w,L_e_q_2=sqrt(2)*Z_o/w,C_p_1=0.01*1/(sqrt
    (2)*Z_o*w),  C_p_2=0.01*1/(sqrt(2)*Z_o*w))*0.01*180/PI)


float(subs(dangle_dRs1*R_s_1,R_s_1 = 0,  R_s_2 = 0,  C=1/(sqrt(2)*
    Z_o*w),L_e_q_1=sqrt(2)*Z_o/w,L_e_q_2=sqrt(2)*Z_o/w,C_p_1=
    0.01*1/(sqrt(2)*Z_o*w),  C_p_2=0.01*1/(sqrt(2)*Z_o*w))
    *0.01*180/PI)


float(subs(dangle_dL1*L_e_q_1,R_s_1 = 1,  R_s_2 = 1,  C=1/(sqrt(2)*
    Z_o*w),L_e_q_1=sqrt(2)*Z_o/w,L_e_q_2=sqrt(2)*Z_o/w,C_p_1=
    0.05*1/(sqrt(2)*Z_o*w),  C_p_2=0.05*1/(sqrt(2)*Z_o*w),Z_o=10,w=
    10^6)*0.01*180/PI)


float(subs(dangle_dL1*L_e_q_1,R_s_1 = 5,  R_s_2 = 5,  C=1/(sqrt(2)*
    Z_o*w),L_e_q_1=sqrt(2)*Z_o/w,L_e_q_2=sqrt(2)*Z_o/w,C_p_1=
    0.01*1/(sqrt(2)*Z_o*w),  C_p_2=0.01*1/(sqrt(2)*Z_o*w),Z_o=10,w=
    10^6)*0.01*180/PI)
```

```
float (subs (dangle_dRs1*R_s_1, R_s_1 = 5, R_s_2 = 5, C=1/(sqrt(2)*
    Z_o*w),L_e_q_1=sqrt(2)*Z_o/w,L_e_q_2=sqrt(2)*Z_o/w,C_p_1=
    0.1*1/(sqrt(2)*Z_o*w), C_p_2=0.1*1/(sqrt(2)*Z_o*w),Z_o=10,w=
    10^6)*0.01*180/PI)
```

```
float (subs (dangle_dRs2*R_s_2, R_s_1 = 5, R_s_2 = 5, C=1/(sqrt(2)*
    Z_o*w),L_e_q_1=sqrt(2)*Z_o/w,L_e_q_2=sqrt(2)*Z_o/w,C_p_1=
    0.1*1/(sqrt(2)*Z_o*w), C_p_2=0.1*1/(sqrt(2)*Z_o*w),Z_o=10,w=
    10^6)*0.01*180/PI)
```

Analysis of mismatched capacitances on Wilkinson divider

```
Clear variables and make assumptions on all component values:
```

```
delete Z_o,C_1,C_2,C_3,C_4,V_o_1,V_o_2,V_A,V_B,V_C,Z_L_1,Z_L_2,
    L_e_q_1,L_e_q_2,C_p_1,C_p_2,R_s_1,R_s_1,C,w,dC_2
assume(Z_o,Type::Real);assume(C_1,Type::Real);assume(C_2,Type::
    Real);assume(C_3,Type::Real);assume(C_4,Type::Real); assume(dC
    ,Type::Real)
assume(L_e_q_1,Type::Real);assume(L_e_q_2,Type::Real);assume(
    C_p_1,Type::Real);assume(C_p_2,Type::Real);assume(R_s_1,Type::
    Real);assume(R_s_2,Type::Real);
assumeAlso(L_e_q_1,Type::Positive);assumeAlso(L_e_q_2,Type::
    Positive);assumeAlso(C_p_1,Type::Positive);assumeAlso(C_p_2,
    Type::Positive);assumeAlso(dC,Type::Real);
assumeAlso(Z_o,Type::Positive);assumeAlso(C_1,Type::Positive);
    assumeAlso(C_2,Type::Positive);assumeAlso(C_3,Type::Positive);
    assumeAlso(C_4,Type::Positive);
```

assume(C, Type :: Real); assumeAlso(C, Type :: Positive); assume(w, Type :: Real); assumeAlso(w, Type :: Positive);

Sum **of** all currents flowing out **of** Vo1:

Node_Vo1 := 0= V_o_1/(Z_o) + (V_o_1−V_o_2)/(2∗Z_o) + (V_o_1−V_B) /(1/(**I**∗w∗C_3))

Node_Vo2 := 0= V_o_2/Z_o + (V_o_2−V_o_1)/(2∗Z_o) + (V_o_2−V_C) /(1/(**I**∗w∗C_4))

Node_V_B := 0=(V_B−V_o_1)/(1/(**I**∗w∗C_3)) + V_B/(Z_L_1) + (V_B−V_A) /(1/(**I**∗w∗C_1))

solve(Node_V_B, V_B)

V_B := (C_1∗V_A∗w∗**I** + C_3∗V_o_1∗w∗**I**)/(C_3∗w∗**I** + 1/Z_L_1 + C_1∗w∗**I**)

Node_V_C := 0=(V_C−V_o_2)/(1/(**I**∗w∗C_4)) + V_C/(Z_L_2) + (V_C−V_A) /(1/(**I**∗w∗C_2))

solve(Node_V_C, V_C)

V_C := (C_2∗V_A∗w∗**I** + C_4∗V_o_2∗w∗**I**)/(C_4∗w∗**I** + 1/Z_L_2 + C_2∗w∗**I**)

Node_Vo2

solve(Node_Vo2, V_o_2)

V_o_2 := (V_o_1/(2*Z_o) - (C_2*C_4*V_A*w^2)/(C_4*w***I** + 1/Z_L_2 +
    C_2*w***I**))/(3/(2*Z_o) - C_4*w*(- 1 + (C_4*w***I**)/(C_4*w***I** + 1/
    Z_L_2 + C_2*w***I**))***I**)

Node_Vo1

solve(Node_Vo1, V_o_1)

TF_Vo1_Va := ((C_1*C_3*V_A*w^2)/(C_3*w***I** + 1/Z_L_1 + C_1*w***I**) + (
    C_2*C_4*V_A*w^2)/(2*Z_o*(3/(2*Z_o) - C_4*w*(- 1 + (C_4*w***I**)/(
    C_4*w***I** + 1/Z_L_2 + C_2*w***I**))***I**)*(C_4*w***I** + 1/Z_L_2 + C_2*w***I**)
    ))/((1/(2*Z_o*(3/(2*Z_o) - C_4*w*(- 1 + (C_4*w***I**)/(C_4*w***I** +
    1/Z_L_2 + C_2*w***I**))***I**)) - 1)/(2*Z_o) - 1/Z_o + C_3*w*(- 1 + (
    C_3*w***I**)/(C_3*w***I** + 1/Z_L_1 + C_1*w***I**))***I**)/V_A

TF_Vo1_Va := subs(TF_Vo1_Va, C_1=C+dC, C_2=C, C_3=C, C_4=C)
Z_L_1 := **I***w*L_e_q_1

Z_L_2 := **I***w*L_e_q_2

TF_Vo1_Va_simp := combine(simplify(combine(TF_Vo1_Va)))

Im_TF := simplify(Im(TF_Vo1_Va_simp))

Re_TF := simplify(Re(TF_Vo1_Va_simp))

Angle_Vo1_Va := simplify(arctan(Im_TF/Re_TF))

Mag_Vo1_Va := simplify(sqrt(Re_TF^2 + Im_TF^2))

dAngle_dC := diff(Angle_Vo1_Va,dC)

float(subs(simplify(subs(dAngle_dC*C,C=1.001/(sqrt(2)*w*Z_o),
    L_e_q_1=sqrt(2)*Z_o/w,L_e_q_2=sqrt(2)*Z_o/w)),dC=0)*0.01*180/
    PI)

Analysis of mismatched loads on Wilkinson divider

Clear variables and make assumptions on all component values:

delete Z_o,C_1,C_2,C_3,C_4,V_o_1,V_o_2,V_A,V_B,V_C,Z_L_1,Z_L_2,
    L_e_q_1,L_e_q_2,C_p_1,C_p_2,R_s_1,R_s_1,C,w,dZ_o

assume(Z_o,Type::Real);assume(C_1,Type::Real);assume(C_2,Type::
    Real);assume(C_3,Type::Real);assume(C_4,Type::Real); assume(
    dZ_o,Type::Real)

assume(L_e_q_1,Type::Real);assume(L_e_q_2,Type::Real);assume(
    C_p_1,Type::Real);assume(C_p_2,Type::Real);assume(R_s_1,Type::
    Real);assume(R_s_2,Type::Real);

assumeAlso (L_e_q_1 , Type :: Positive) ; assumeAlso (L_e_q_2 , Type ::
    Positive) ; assumeAlso (C_p_1 , Type :: Positive) ; assumeAlso (C_p_2 ,
    Type :: Positive) ; assumeAlso (dZ_o , Type :: Positive) ;
assumeAlso (Z_o , Type :: Positive) ; assumeAlso (C_1 , Type :: Positive) ;
    assumeAlso (C_2 , Type :: Positive) ; assumeAlso (C_3 , Type :: Positive) ;
    assumeAlso (C_4 , Type :: Positive) ;

assume (C , Type :: Real) ; assumeAlso (C , Type :: Positive) ; assume (w , Type ::
    Real) ; assumeAlso (w , Type :: Positive) ;

Sum **of** all currents flowing out **of** Vo1 :
Node_Vo1 := 0= V_o_1 / (Z_o + dZ_o) + (V_o_1−V_o_2) / (2 ∗ Z_o) + (
    V_o_1−V_B) / (1 / (**I** ∗w∗ C_3))

Node_Vo2 := 0= V_o_2 / Z_o + (V_o_2−V_o_1) / (2 ∗ Z_o) + (V_o_2−V_C)
    / (1 / (**I** ∗w∗ C_4))

Node_V_B := 0=(V_B−V_o_1) / (1 / (**I** ∗w∗ C_3)) + V_B / (Z_L_1) + (V_B−V_A)
    / (1 / (**I** ∗w∗ C_1))

solve (Node_V_B , V_B)

V_B := (C_1 ∗V_A∗w∗ **I** + C_3 ∗ V_o_1 ∗w∗ **I**) / (C_3 ∗w∗ **I** + 1 / Z_L_1 + C_1 ∗w∗ **I**
)

Node_V_C := 0=(V_C–V_o_2)/(1/(**I**∗w∗C_4)) + V_C/(Z_L_2) + (V_C–V_A)/(1/(**I**∗w∗C_2))

solve(Node_V_C,V_C)

V_C := (C_2∗V_A∗w∗**I** + C_4∗V_o_2∗w∗**I**)/(C_4∗w∗**I** + 1/Z_L_2 + C_2∗w∗**I**)

Node_Vo2

solve(Node_Vo2,V_o_2)

V_o_2 := (V_o_1/(2∗Z_o) − (C_2∗C_4∗V_A∗w^2)/(C_4∗w∗**I** + 1/Z_L_2 + C_2∗w∗**I**))/(3/(2∗Z_o) − C_4∗w∗(− 1 + (C_4∗w∗**I**)/(C_4∗w∗**I** + 1/Z_L_2 + C_2∗w∗**I**))∗**I**)

Node_Vo1

solve(Node_Vo1,V_o_1)

TF_Vo1_Va := ((C_1∗C_3∗V_A∗w^2)/(C_3∗w∗**I** + 1/Z_L_1 + C_1∗w∗**I**) + (C_2∗C_4∗V_A∗w^2)/(2∗Z_o∗(3/(2∗Z_o) − C_4∗w∗(− 1 + (C_4∗w∗**I**)/(C_4∗w∗**I** + 1/Z_L_2 + C_2∗w∗**I**))∗**I**)∗(C_4∗w∗**I** + 1/Z_L_2 + C_2∗w∗**I**)))/(− 1/(Z_o + dZ_o) + (1/(2∗Z_o∗(3/(2∗Z_o) − C_4∗w∗(− 1 + (C_4∗w∗**I**)/(C_4∗w∗**I** + 1/Z_L_2 + C_2∗w∗**I**))∗**I**)) − 1)/(2∗Z_o) + C_3∗w∗(− 1 + (C_3∗w∗**I**)/(C_3∗w∗**I** + 1/Z_L_1 + C_1∗w∗**I**))∗**I**)/V_A

```
TF_Vo1_Va := simplify(subs(TF_Vo1_Va, C_1=C, C_2=C, C_3=C, C_4=C))

Z_L_1 := I*w*L_e_q_1


Z_L_2 := I*w*L_e_q_2


TF_Vo1_Va_simp := combine(simplify(combine(TF_Vo1_Va)))

Im_TF := simplify(Im(TF_Vo1_Va_simp))


Re_TF := simplify(Re(TF_Vo1_Va_simp))


Angle_Vo1_Va := simplify(arctan(Im_TF/Re_TF))


Mag_Vo1_Va := simplify(sqrt(Re_TF^2 + Im_TF^2))


dAngle_dZ_o := simplify(diff(Angle_Vo1_Va, dZ_o))


subs(dAngle_dZ_o, C=1/(sqrt(2)*w*Z_o), L_e_q_1=sqrt(2)*Z_o/w,
    L_e_q_2=sqrt(2)*Z_o/w, dZ_o=0)
```

Gilbert Cell Analysis Including Mismatch

```
Clean up workspace:


delete V_gs1, V_gs2, I_T, I_d_1, I_d_2, kn, ar1, ar2, ar_1, ar_2,
    ar_3, ar_4, ar_5, ar_6
```

```
delete vt, I_d_solution, I1, I2, I3, I4, I5, I6, I_op, I_on, I_o,
    I_o_allmatch

delete Vid, Vid1, Vid2, F_Vid1_allmatch, dvt1, dvt2, dvt_1, dvt_2
    , dvt_3, dvt_4, dvt_5, dvt_6
```

Circuit equations:

```
V_gs1 := vt + dvt1 + (2*I_d_1/(kn*ar1))^(1/2)

V_gs2 := vt + dvt2 + (2*(I_T−I_d_1)/(kn*ar2))^(1/2)

Vid_eq := 0 = V_gs1 − V_gs2 − Vid

subs(Vid_eq, Vid = Vid_new − dvt2 + dvt1)
```

Solve **for** Id1 **and** Id2
```
I_d_solution := solve(subs(Vid_eq,Vid=Vidnew−dvt2+dvt1),I_d_1)
    assuming I_d_1>0 and ar1>0 and ar2>0 and kn>0 and I_T>0

I_d_1 := simplify(subs(piecewise::expression(I_d_solution,2),
    Vidnew=Vid+dvt2−dvt1))

I_d_2 := simplify(I_T − I_d_1)
```

```
simplify(subs(I_d_1,ar1=ar,ar2=ar,dvt1=0,dvt2=0))


simplify(subs(I_d_2,ar1=ar,ar2=ar,dvt1=0,dvt2=0))


I5 := subs(I_d_1,Vid='Vid1',ar1=ar_5,ar2=ar_6,dvt1=dvt_5,dvt2=
    dvt_6)


I6 := subs(I_d_2,Vid='Vid1',ar1=ar_5,ar2=ar_6,dvt1=dvt_5,dvt2=
    dvt_6)


I1 := subs(I_d_1,I_T=I5,Vid='Vid2',ar1=ar_1,ar2=ar_2,dvt1=dvt_1,
    dvt2=dvt_2)


I2 := subs(I_d_2,I_T=I5,Vid='Vid2',ar1=ar_1,ar2=ar_2,dvt1=dvt_1,
    dvt2=dvt_2)


I3 := subs(I_d_2,I_T=I6,Vid='Vid2',ar1=ar_4,ar2=ar_3,dvt1=dvt_4,
    dvt2=dvt_3)


I4 := subs(I_d_1,I_T=I6,Vid='Vid2',ar1=ar_4,ar2=ar_3,dvt1=dvt_4,
    dvt2=dvt_3)


I_op := I1 + I3


I_on := I2 + I4
```

I_o := simplify(I_op − I_on)

I_o_allmatch := simplify(subs(I_o, ar_1=ara, ar_2=ara, ar_3=ara, ar_4
    =ara, ar_5=ara*2, ar_6=ara*2, dvt_1=0, dvt_2=0, dvt_3=0, dvt_4=0,
    dvt_5=0, dvt_6=0, Vid1^2=0, Vid2^2=0))

F_Vid1_allmatch := I_o_allmatch/Vid2

diff(F_Vid1_allmatch, Vid1)

Test transistor matching (assume 5 **and** 6 matched, **and** try various
    combinations **of** matching between 1,2,3, **and** 4)
With Vid1=0, output current should be zero regardless **of** Vid2

Matching 1/2, **and** 3/4
simplify(subs(I_o, Vid1=0, dvt_5=0, dvt_6=0, ar_1=ara, ar_2=ara, ar_3=
    arb, ar_4=arb, ar_5=arc, ar_6=arc, dvt_1=dvta, dvt_2=dvta, dvt_3=
    dvtb, dvt_4=dvtb))

Matching 2/3, **and** 1/4
simplify(subs(I_o, Vid1=0, dvt_5=0, dvt_6=0, ar_1=ara, ar_2=arb, ar_3=
    arb, ar_4=ara, ar_5=arc, ar_6=arc, dvt_1=dvta, dvt_2=dvtb, dvt_3=
    dvtb, dvt_4=dvta))

Matching 1/3, **and** 2/4

simplify (subs (I_o , Vid1=0 , dvt_5=0 , dvt_6=0 , ar_1=ara , ar_2=arb , ar_3= ara , ar_4=arb , ar_5=arc , ar_6=arc , dvt_1=dvta , dvt_2=dvtb , dvt_3= dvta , dvt_4=dvtb))

As can be seen **from** above , the only matching (threshold **and** area) combination that keeps the outputs balanced is 1/4 , **and** 2/3 ; Not the individual diff pairs **of** 1/2 **and** 3/4 as originally assumed .

However , **if** we assume that all transistors are large enough **to** make the areas match regardless , matching both 1/2 , **and** 3/4 works just as well as matching 1/4 ,2/3 :

1/4 ,2/3 :
simplify (subs (I_o , Vid1=0 , dvt_5=0 , dvt_6=0 , ar_1=ara , ar_2=ara , ar_3= ara , ar_4=ara , ar_5=arc , ar_6=arc , dvt_1=dvta , dvt_2=dvtb , dvt_3= dvtb , dvt_4=dvta))

1/2 ,3/4
simplify (subs (I_o , Vid1=0 , dvt_5=0 , dvt_6=0 , ar_1=ara , ar_2=ara , ar_3= ara , ar_4=ara , ar_5=arc , ar_6=arc , dvt_1=dvta , dvt_2=dvta , dvt_3= dvtb , dvt_4=dvtb))

1/3 ,2/4 does **not** work , as shown :
simplify (subs (I_o , Vid1=0 , dvt_5=0 , dvt_6=0 , ar_1=ara , ar_2=ara , ar_3= ara , ar_4=ara , ar_5=arc , ar_6=arc , dvt_1=dvta , dvt_2=dvtb , dvt_3= dvta , dvt_4=dvtb))

Start looking at Taylor series expansion:

F_Vid1_allmatch := Simplify(I_o_allmatch/Vid2)

F_Vid1_allmatch1 := −(kn^(1/2)∗((2∗I_T∗ara − 2∗2^(1/2)∗Vid1∗ara∗
    kn^(1/2)∗(I_T∗ara)^(1/2))^(1/2) − (2∗I_T∗ara + 2∗2^(1/2)∗Vid1∗
    ara∗kn^(1/2)∗(I_T∗ara)^(1/2))^(1/2)))/2

expand(diff(F_Vid1_allmatch,Vid1))

Linear term is ar∗kn
simplify(taylor(F_Vid1_allmatch1,Vid1,3))
I_o_simple_linear := Vid2∗(Vid1∗ara∗kn)
I_o_simple_sine_in := collect(simplify(expand(subs(
    I_o_simple_linear,Vid1=A1∗cos(2∗PI∗f_o∗t)+Vin1_o_f_f,Vid2=A2∗
    cos(2∗PI∗f_o∗t + 'φ')+Vin2_o_f_f)),cos),cos('φ'))

Gain **for** phase difference around 90 degrees (d/dphi cos(phi) **for**
    phi ˜= 90 is ˜1) is:
((A1∗A2∗ara∗kn)/2)∗'φ'

Other DC term is the multiplied offsets:
Vin1_o_f_f∗Vin2_o_f_f∗ara∗kn

For an offset less than one degree:

simplify(subs(('φ'*A1*A2*ara*kn)/2 > Vin1_o_f_f*Vin2_o_f_f*
    ara*kn,'φ'=PI*2/180))*(360/(2*PI))/(ara*kn*Vin1_o_f_f*
    Vin2_o_f_f) assuming ara>0 **and** kn>0 **and** Vin1_o_f_f>0 **and**
    Vin2_o_f_f>0

Assuming equal amplitude inputs **and** identical offsets **from** the
    preceding stage:

subs((180/PI) < (A1*A2)/(Vin1_o_f_f*Vin2_o_f_f),A1=A,A2=A,
    Vin1_o_f_f=V_off, Vin2_o_f_f=V_off)

float(simplify(sqrt(180/PI) < sqrt((A^2)/V_off^2),sqrt)) assuming
    A>0 **and** V_off>0

This shows that the absolute value ratio **of** the amplitude **of** the
    input signal(s) **to** the input offset(s) must be greater than
    sqrt(360/pi) **or** ~11
for the equivalent phase detector error **to** be <1 degree

<u>Active Inductor Equivalent Circuit Calculations</u>

delete C_G_S_2,C_G_S_1,C_G_S_3,g_M_1,g_M_2,g_M_3,L_e_q,R_p,R_s,
    C_p,I_D_1,I_D_2,I_D_3,I_b_1,I_b_2,ar1,ar2,ar3,Kn

Equations **from** Lu (p17 Bucossi)
L_e_q := C_G_S_2 / (g_M_1 * g_M_2)

$R\_p := 1/g\_M\_1$

$C\_p := C\_G\_S\_1$

$R\_s := -w^2 * C\_G\_S\_2 * C\_G\_S\_3 / (g\_M\_1 * g\_M\_2 * g\_M\_3)$

Sub **in for** transconductance

$g\_M\_1 := (2 * Kn * ar1 * I\_D\_1)^{(1/2)}$

$g\_M\_2 := (2 * Kn * ar2 * I\_D\_2)^{(1/2)}$

$g\_M\_3 := (2 * Kn * ar3 * I\_D\_3)^{(1/2)}$

$I\_D\_1 := I\_b\_1$

$I\_D\_2 := I\_b\_2$

$I\_D\_3 := I\_b\_1$

L_e_q

C_p

R_s

R_p

ar1 := '(W/L)_1'

ar2 := '(W/L)_2'

ar3 := '(W/L)_3'

L_e_q

L_e_q := C_G_S_2/(2*Kn*('(W/L)_1'*I_b_1*'(W/L)_2'*I_b_2)^(1/2))

simplify(R_s)

C_p

R_p

subs(L_e_q,'(W/L)_1'=1,'(W/L)_2'=1,I_b_1=500*10^(−6),I_b_2=
    160*10^(−6))

Equation for getting Bias current from control voltage
I_b_2 := 1/2*K_p*'(W/L)_8'*(V_D_D − V_C_N_T_L − V_t_p)^2

L_e_q

subs(diff(L_e_q, V_C_N_T_L), `(W/L)_1`=1, `(W/L)_2`=1, I_b_1=
500*10^(-6), V_C_C=10, R_e=20000, V_C_N_T_L=6.1)