

FABRICATION OF SUBWAVELENGTH SCALE OPTICAL
NANOSTRUCTURES

by

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TABLE OF CONTENTS

| | |
|--|----|
| 1. INTRODUCTION | 1 |
| 1.1 Background and Motivation..... | 1 |
| 1.2 Summary of the Fabrication Process..... | 2 |
| 1.3 Research Work Presented in this Thesis | 4 |
| 2. FABRICATION OF SUBWAVELENGTH-SIZE SOLID IMMERSION LENSES | 7 |
| 2.1 Introduction | 7 |
| 2.2 Calibration of Spinning Process for Nano-SIL | 8 |
| 2.3 Calibration of Lithography for Nano-SIL | 11 |
| 2.3.1 Introduction to Electron Beam Lithography | 11 |
| 2.3.2 Dose Calibration | 12 |
| 2.3.3 Calibration Sequence for Nano-SILs..... | 13 |
| 2.4 Fabrication of Nano-SIL | 15 |
| 2.4.1 Complete Fabrication Sequence of Nano-SIL..... | 15 |
| 2.4.2 Design of Final Device | 16 |
| 2.5 Measurement of Nano-SIL Shape after Lithography..... | 19 |
| 2.5.1 450nm Diameter | 19 |
| 2.5.2 600nm Diameter | 22 |
| 2.5.3 Comparing 600 nm and 450 nm Nano-SILs..... | 23 |
| 2.5.4 Issues with 300nm Diameter Nano-SILs..... | 25 |
| 2.5.5 Shape Measurements After Reflow and Replication..... | 26 |
| 2.6 Nano-SIL Fabrication and Characterization by our Collaborators | 28 |
| 2.6.1 Reflow and Replication Process | 29 |
| 2.6.2 Optical Characterization | 29 |
| 2.7 Conclusion..... | 30 |
| 3. FABRICATION OF ANTI REFLECTIVE GRATINGS IN SILICON..... | 31 |
| 3.1 Introduction | 31 |
| 3.2 Calibrating Mask Patterning for 1D Gratings | 32 |
| 3.2.1 PMMA Bilayer Spinning and Liftoff Process | 32 |
| 3.2.3 Calibrating EBL for 1D Gratings | 35 |
| 3.5 Etching | 38 |
| 3.5.1 ICP-RIE Etching..... | 38 |
| 3.5.2 Etchrate Calibration..... | 40 |
| 3.7 Fabrication of AR Gratings..... | 43 |
| 3.8 Simulation and Characterization | 47 |

TABLE OF CONTENTS CONTINUED

| | |
|--|----|
| 3.8.1 Device 1 (DH5) | 47 |
| 3.8.2 Device 2 (TH68)..... | 50 |
| 3.9 Conclusion..... | 51 |
| 4. MID INFRARED POLARIZING BEAM SPLITTER..... | 54 |
| 4.1 Introduction | 54 |
| 4.2 Fabrication Steps up to Etching | 55 |
| 4.2.1 Field Stitching in Lithography..... | 55 |
| 4.2.2 Lithography | 57 |
| 4.2.2 Etching and Dimension Measurements | 57 |
| 4.3 Gold Deposition | 60 |
| 4.3.1 Gold Film Measurements | 60 |
| 4.3.2 Directionality and Thickness Calibration | 61 |
| 4.4 Conclusion..... | 66 |
| 5. CONCLUSION..... | 67 |

LIST OF TABLES

| Table | Page |
|---|------|
| 2.1: Spin speeds and PMMA concentrations for different required resist thicknesses | 9 |
| 2.2: Spin speeds for a batch of 100nm thick samples spun with 2% PMMA | 10 |
| 2.3: Dose and diameters for different PMMA nano-SIL shapes | 14 |
| 2.4: Design parameters of nano-SIL PMMA cylinders | 16 |
| 2.5: Measured diameter data for 450nm nominal diameter nano-SIL (all units in nm) | 20 |
| 2.6: Measured diameter data for 600nm nominal diameter nano-SIL | 22 |
| 2.7: Comparing statistical data between the two types of nano-SIL | 24 |
| 2.8: Sample measurement data for 450nm nominal diameter nano-SIL after reflow and replication | 27 |
| 3.1: Table showing data relating software and hard mask line width. | 36 |
| 3.2: ICP recipes used for silicon etching | 39 |
| 3.3: Multistep etching results of DH5 | 43 |
| 3.4: Dimensions of DH5 sample | 47 |
| 4.1: Summary of data for stage alignment errors..... | 58 |
| 4.2: Etch times and etch depths for multistep etching of IR PBS sample TH69 | 58 |
| 4.3: Required and measured dimensions of fabricated TH69 sample along with percentage errors | 58 |
| 4.4: Gold thickness calibration | 65 |

LIST OF FIGURES

| Figure | Page |
|---|------|
| 1.1: Fabrication process sequence for the mid-infrared polarizing beam splitter..... | 3 |
| 2.1: Underexposed PMMA, small islands of PMMA visible outside the cylinder | 14 |
| 2.2: Shape of PMMA nano-SILs before and after reflow | 16 |
| 2.3: Overview of mask (there are actually 6 rows A - F)..... | 18 |
| 2.4: Details of one square..... | 18 |
| 2.5: A single square of a 450nm nominal diameter nano-SIL sample after lithography | 21 |
| 2.6: Details of one PMMA cylinder, showing diameter measurements in horizontal and vertical direction | 22 |
| 2.7: Details of one PMMA Cylinder of a 600nm nominal diameter nano-SIL | 23 |
| 2.8: Comparing measured and expected diameters after lithography of the two types of nano-SIL..... | 24 |
| 2.9: 300nm nominal diameter nano-SIL | 26 |
| 2.10: SEM picture of a nano-SIL after reflow and replication | 28 |
| 3.1: Bilayer PMMA and liftoff process | 33 |
| 3.2: SEM image of lifted off grating..... | 34 |
| 3.3: Graph showing relation of software and hard mask line width for 3 different samples. | 37 |
| 3.4: Etch rate over several trials..... | 41 |

LIST OF FIGURES - CONTINUED

| Figure | Page |
|---|------|
| 3.5 SEM profile view of an etched grating showing sidewall slant. | 44 |
| 3.6: SEM picture of TH68 sample, showing a measurement of upper line width | 45 |
| 3.7: SEM picture (profile view) of a cleaved sample TH22 | 46 |
| 3.8: RCWA results for a grating of line width 404nm..... | 48 |
| 3.9: Optical characterization results of DH5 sample | 59 |
| 3.10: RCWA simulation results of TH68 sample | 50 |
| 3.11: Optical characterization results of TH68 sample..... | 51 |
| 4.1: Design parameters for the mid-IR PBS | 55 |
| 4.2: Profile view of fabricated TH69 sample. | 59 |
| 4.3: Top down view of fabricated TH69 sample | 59 |
| 4.4: Diagram showing orthogonal mounting of sample in the deposition chamber. | 62 |
| 4.5: Gold deposition without directionality control. | 63 |
| 4.6: First trial of gold deposition with orthogonal mounting of the sample. | 64 |
| 4.7: Second trial of gold deposition with orthogonal mounting of the sample. | 64 |

ABSTRACT

Sub-wavelength scale optical nanostructures can be engineered for specific applications in multiple disciplines. This thesis describes the fabrication of three such optical nanostructures and the process development and optimization performed to improve the nanofabrication capabilities of our research group. Along with our collaborators we have fabricated a subwavelength-scale solid immersion lens. The fabrication process of cylinders of precise dimensions in resist is discussed as well as the measurements and characterization of the final fabricated device. The second device is a 1-D antireflective rectangular grating in silicon with 800nm period, which is fabricated, simulated and characterized. The lithography process is calibrated for gratings with 250-600nm line widths and the etching process is optimized to obtain depths precise to within ± 10 nm. The final device is a mid-infrared polarizing beam splitter. The fabrication of this device is not yet complete, but the correct grating structure in silicon is fabricated and some process improvements for gold deposition have been realized.

INTRODUCTION

1.1 Background and Motivation

The field of nano-optics is a relatively new area of study. With the advancement of semiconductor fabrication technology, it has become possible to fabricate devices on the nano scale. By adapting these technologies, it is possible to make sub-wavelength scale optical structures which can have a wide range of applications. However, adaptation of these fabrication methods requires some process development and optimization, tailored specifically for the structures of interest.

Sub-wavelength scale optical structures can be engineered for a wide range of functionalities and applications. For example, a nanostructured surface can act as an effective medium with engineered material properties, which can be used to make antireflective structures [1-10] or blazed gratings and Fresnel lenses [11]. Resonance effects from simple gratings can be used to make Bragg wavelength filters [12-14] or couplers for waveguides [15-16]. Single or multilayer gratings or wire grids of subwavelength scale can be engineered to make polarizers and polarizing beam splitters [17-25]. Subwavelength scale solid immersion lenses can be used to create high intensity sub-diffraction spots [26]. These devices can have applications in areas such as imaging, biochemical or atmospheric sensing, data storage and optical communications.

All of our fabrication processes are based on silicon. Silicon is advantageous for two specific reasons. The processes for fabrication of silicon are well known and have been developed by the semiconductor industry for decades, and thus we “borrow” most

of the methods and modify them for our own specific needs. Secondly, fabrication in silicon gives us the potential opportunity to integrate our devices with other optical devices, electronics or microelectromechanical systems (MEMS) [27-28].

One of the major challenges of nano-optics is precise fabrication of structures on the nanoscale. For feature sizes on the order of tens of nanometers or even a few hundred nanometers, this can become somewhat of a challenge. Although the technology and processes required for this do exist [29-30], it requires a fair amount of process control to be able to make the final device with the necessary fabrication tolerances. For each step in the fabrication chain we need to calibrate the process and optimize the recipes to get the desired results. In this thesis we will demonstrate the calibration and optimization of electron beam lithography and etching, as well as some process improvement performed for metal deposition. These capabilities then allow us to fabricate three example devices, the successful completion and testing of which will establish that we have achieved basic nanofabrication capabilities.

1.2 Summary of the Fabrication Process

Most nanostructures made in silicon are fabricated using a similar process chain, the fundamentals of which are generally common knowledge [31-32]. The basic sequence of fabrication steps is often the same, but some structures may use a subset of the processes or some modified version of the standard process. In this thesis, each chapter addresses the optimization of a few related process steps, and presents an example device

produced using those steps. Thus, to gain a better understanding of the whole fabrication process chain, an overview is first presented here.

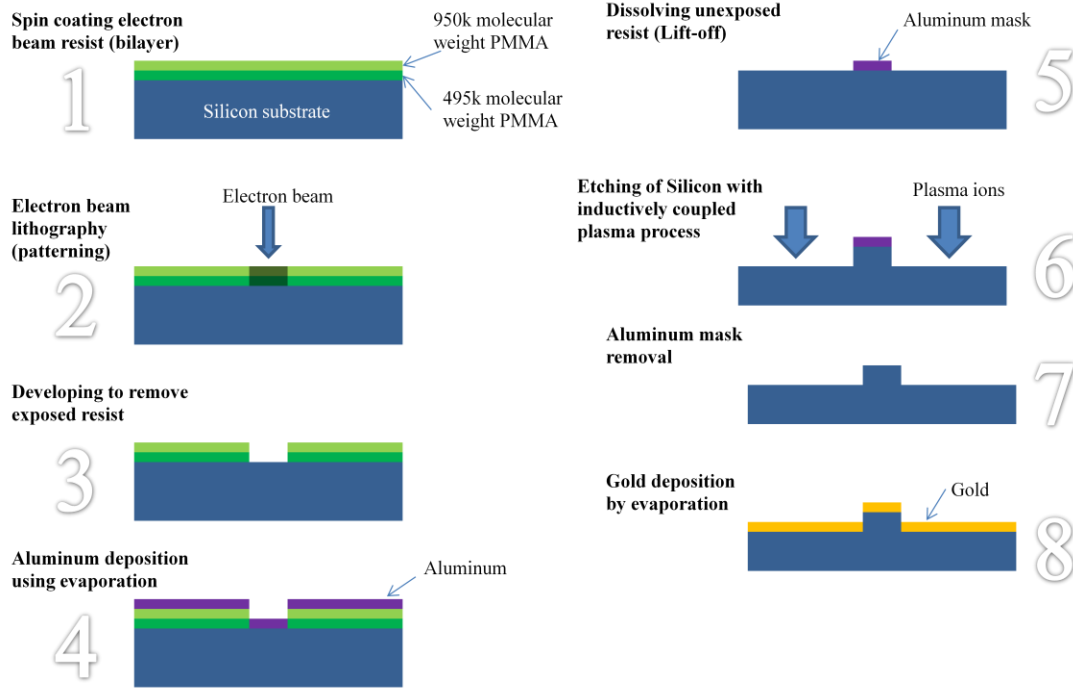


Figure 1.1: Fabrication process sequence for the mid-infrared polarizing beam splitter

Figure 1.1 shows the fabrication steps for the device described in Chapter 4, which is the most complex of the three devices, and will utilize all of the fabrication steps.

Fabrication starts with the spinning of a resist layer on top of the silicon substrate. We use an electron beam resist, Poly-methyl methacrylate (PMMA), which is deposited as a bi-layer of two different molecular weights. In step two, the resist is patterned using electron beam lithography. A field emission scanning electron microscope (SEM), modified for use for lithography with the Nanometer Pattern Generation System (NPGS), is used to write the desired pattern. The electrons change the chemical structure of the

resist, and in the subsequent development step (step 3), the exposed resist is removed using a mixture of Isopropanol and Methyl isobutyl ketone. This leaves the desired pattern in the resist.

This pattern then needs to be transferred into the silicon substrate itself, which is achieved through an etching step. The resist layer is too soft to survive the etching process and act as a mask, thus the pattern is transferred into a metal mask in a lift-off process. An 80 nm thick aluminum layer is deposited on the substrate using an electron beam evaporator (step 4) and then the resist is removed by dissolving away with solvents and ultrasonic agitation in acetone (step 5). This leaves the aluminum on the areas exposed in the lithography step, thus becoming an inverse image of the resist mask. The pattern is then transferred into the substrate with a directional dry etching step consisting of a fluorine-based chemistry in an inductively coupled plasma–reactive ion etching process (step 6). This is followed by chemical removal of the aluminum mask using a PAN (a solution of “Phosphoric - Acetic – Nitric” acids) etchant (step 7). Finally a layer of gold is deposited directionally on the top of the sample using electron beam evaporation (step 8).

1.3 Research Work Presented in this Thesis

The work presented in this thesis primarily addresses the fabrication of nanostructures. Three different optical nanostructures are presented. These devices are discussed in order of increasing complexity of fabrication, and it is demonstrated how we have learned from fabricating the simpler structures first and have used this knowledge

with the more complex structures. The fabrication processes for each of these devices are presented in detail, as well as summary results concerning simulation and characterization. Besides the devices, another important aspect of this thesis is the development of nanofabrication capabilities. This involves calibration or optimization of recipes and processes, thus achieving better process control.

Although my work is almost exclusively based on fabrication, I have to rely on other members of our research group for work on characterization and simulation. There are also other group members with whom I have worked in fabrication. Also, much of our work is done in collaboration with other researchers from Neuchâtel, Switzerland and from MSU as well. The work done by collaborators or other group members will be properly cited.

This thesis has three body chapters, each discussing the fabrication of one of the devices. Each device uses a subset of the whole process chain, and they are discussed in the order of increasing complexity in fabrication. Chapter 2 is about the subwavelength size Solid Immersion Lens (nano-SILs). The calibration of the spinning process and the electron beam lithography for making the devices is shown, as well as discussion of the actual fabrication process. This deals with the process optimizations for steps 1-3 in Figure 1.1. The results of optical characterization of the nano-SILs are also summarized. Chapter 3 is about antireflective gratings. The spinning of the resist bilayer, calibration of lithography for 1-D gratings and also a discussion of the etching process is shown, as well as a summary of the characterization and simulation work. This encompasses steps 1 through 7 in Figure. 1.1. Chapter 4 is about a mid infrared polarizing beam splitter. This

device, the most complex of the three, will use all of the fabrication techniques of the previous chapters, as well as directional gold deposition, thus using the entire process chain from steps 1 to 8 in Figure. 1.1. Thus each chapter builds on the fabrication processes discussed before, culminating in the final device which brings all of the steps together.

This thesis will present the fabrication process of the three devices and discuss the process optimizations done to improve our fabrication capabilities. Although, our optimizations are far from complete, we now have the capability to fabricate subwavelength scale nanostructures.

FABRICATION OF SUBWAVELENGTH-SIZE SOLID IMMERSION LENSES

2.1 Introduction

The fabrication of any nanostructure starts with spin-coating of a resist material and lithography (patterning). The optimization of these processes in order to make structures with precise features on the order of hundreds of nanometers is the first step towards nanofabrication. In order to demonstrate our capability in doing so, we first fabricate simple cylinders in a resist which is used in a collaborative project, the Subwavelength-size Solid Immersion Lens [26].

A solid immersion lens (SIL), first demonstrated by Mansfield and Kino [33], is a small (typically hemispherically shaped) lens placed in the path of the incoming light rays, usually before the sample and the objective lens. Because of the curvature of the lens and the higher index of the material, incoming rays will not be diffracted away, and will form a tight cone of light which can be imaged with an objective lens. The use of a SIL in a standard microscopy setup results in an increase in the numerical aperture by a factor of n (the refractive index of the solid material), and a decrease in the spot size by the same factor. This translates to increased light gathering efficiency and improved resolution.

Following Mansfield [33], there have been many demonstrations at different size scales: micrometer-size SILs [34-36], and wavelength-scale SILs [37-38]. However all of these so far have used a SIL of a size either larger than or approximately equal to the wavelength of light used. Previous work has suggested that SILs reduced to

subwavelength scale would still exhibit similar optical properties [39-40]. Thus our collaborators suggested fabricating sub-wavelength size SILs (called nano-SILs) and characterizing them. The nano-SIL can reduce the spot size of a focused beam of visible light to beyond the diffraction limit. This will create a highly concentrated optical field in a small area, with potential applications in data storage, high-resolution lithography, or sensing applications.

The main part of the work for this project was performed by our collaborators: Myun-Sik Kim, Vincent Paeder, Toralf Scharf and Hans Peter Herzig from the Optics & Photonics Technology Laboratory, Swiss Federal Institute of Technology, Lausanne, in Neuchâtel, Switzerland. Our work in this project included the fabrication of the PMMA cylinder samples and structural characterization of the nano-SILs using SEM and AFM. The remainder of the work (including the device design, reflow and replication, and optical characterization) was performed by our collaborators.

The first step in the fabrication of the nano-SILs is to make PMMA cylinders of a specific height and diameter. To do this we need precise control of the spinning process and lithography. Thus, our work consists of the calibration of these processes, producing the final device, and then measuring the dimensions to confirm that they were within the design specifications.

2.2 Calibration of Spinning Process for Nano-SIL

The first step in the fabrication process for the nano-SIL is to deposit a smooth layer of electron beam resist on top of a silicon substrate. The resist thickness was

required to be 100, 150 and 200 nm, and accurate to within a few nanometers. The resist we use is Poly-methyl methacrylate (PMMA), which is a high resolution positive resist and is also a transparent thermoplastic. PMMA was one of the first electron resists developed [41] and is still one of the highest resolution resists available. PMMA has been demonstrated to achieve sub-10 nm resolution by many researchers, for example 4.4nm features in resist [42], and 5-7 nm etched lines in silicon [43]. PMMA is available in different molecular weights, and we chose to use a 950k molecular weight PMMA.

To realize the required layer thicknesses we needed to make PMMA of different concentrations as well as calibrate the spin speeds. The spin curve as supplied by the manufacturer [44] shows the thicknesses for different concentrations (the solvent is anisole) and spin speeds. After estimating from the spin curve, we did some initial trials and selected three different PMMA concentrations: 2%, 2.5%, and 3% (see Table 2.1).

Table 2.1: Spin speeds and PMMA concentrations used to produce the desired PMMA layer thicknesses

| Layer thickness | PMMA concentration | Spin speed (RPM) |
|-----------------|--------------------|------------------|
| 100nm | 2% | 2500-2700 |
| 150nm | 2.5% | 1500-1700 |
| 200nm | 3% | 4300-4500 |

We next estimated the spin speed required from the manufacturer's spin curve and then after several trials and measurements, we obtained the required thicknesses. One problem we noted was that the solvent from the PMMA evaporated very quickly and gave us thicker layers for each successive sample within the same batch. The solvent

from the PMMA which was held in pipettes would evaporate over the range of minutes. To counter this we had to increase the spin speed every couple of samples by a small amount. When making batches of samples we measured every sample immediately after it was spun. If the sample was more than 5 nm above or below the required thickness (we chose a 5 nm tolerance), we discarded the sample and then changed the spin speed of the next sample slightly to compensate. We saw that we usually had to increase the spin speed by 50 RPM after about every two samples. An example of a sequence of sample production for 100nm thick 2% PMMA samples is shown in Table 2.2.

Table 2.2: Spin speeds for a batch of 100 nm thick samples spun with 2% PMMA, showing increase of spin speed to counter the evaporation of solvent over time.

| Sample number | Spin speed (RPM) | Thickness (nm) |
|---------------|------------------|----------------|
| 1 | 1500 | 105 |
| 2 | 1550 | 101 |
| 3 | 1550 | 104 |
| 4 | 1600 | 103 |
| 5 | 1650 | 104 |
| 6 | 1650 | 102 |
| 7 | 1700 | 101 |
| 8 | 1700 | 100 |

The samples were measured using a Nanospec 3000, which measures thin film thicknesses using spectroscopic reflectometry. The Nanospec has a measurement precision of 0.1 nm, but its accuracy depends on the calibration and other input parameters such as the refractive index of PMMA. We have not verified the accuracy of

these measurements, but we have noticed from multiple measurements that they are fairly reproducible (range of variation < 1 nm) and thus self consistent.

The data for the spin speeds and final thicknesses are shown in Table 2.2. We have demonstrated a simple method to spin the required thicknesses of PMMA with a maximum 5 nm deviation. Each sample is measured and shown to be within the tolerance range for resist thickness.

2.3 Calibration of Lithography for Nano-SIL

2.3.1 Introduction to Electron Beam Lithography

Electron Beam lithography (EBL) is a process for patterning a resist on a nanometer scale. This pattern can later be transferred into the substrate material. EBL is preferred over other forms of lithography in nano-optics because it has a much higher resolution.

During EBL a focused beam of electrons impacts the sample and induces local chemical changes in the resist. There are many factors which affect the resultant pattern being written: the electron dose (which depends on the beam current and the exposure time), the electron acceleration voltage, the beam spot size, the aperture size, the resist thickness and the resist development process. All of these factors will affect the feature size of the pattern being written. Instead of studying the effects of all of these factors we chose to control only two, the electron dose and the feature size in the software design mask. There is no simple method to predict values for these two factors for a specific

structure. Thus, we need to perform several tests and calibration runs to obtain detailed calibration data.

2.3.2 Dose Calibration

The required dose depends on the PMMA thickness, development (time and developer concentration), feature size and the exact type of pattern. Generally PMMA has a fairly large range of doses over which the resist will be properly exposed. However, too low of a dose will result in residual PMMA (see Section 2.3.4) and too high of a dose may distort the shape and size of the resulting patterns.

There are two ways to perform the calibration: a dose calibration test to find a dose that works, and then fine adjusting the software feature sizes to get the correct final feature size; or a first test with an array of different feature sizes to get close to the expected size, and then fine adjusting by varying the dose. We use the first method since the feature size does not change linearly with dose, and thus it is more predictable and reproducible.

In the first trial we make an array of the original pattern with widely varying doses. For example an array of 3x3 of the pattern can be made with the dose varying from 200 to 520 $\mu\text{C}/\text{cm}^2$, in increments of 40 $\mu\text{C}/\text{cm}^2$. After development we check the resulting patterns and select the dose which gives the feature size closest to the required size. For PMMA this dose will probably be within the range 250 to 400 $\mu\text{C}/\text{cm}^2$ depending on the type of pattern and the PMMA thickness.

For example, for a 1-D grating with a feature size of about 600nm, a dose of 260 $\mu\text{C}/\text{cm}^2$ is ideal. We know from experimental trials that this dose will work for similar

gratings with feature sizes approximately 250-800nm. Thus, we can skip this step when making similar gratings in the future. For patterns much smaller or larger, or which are quite different, we will need to perform a dose calibration again. Dose calibration is required to make the exact feature size for the specific structure, but calibrations done for similar structures can help save trials and help us estimate the processing steps for new devices.

2.3.3 Calibration Sequence for Nano-SILs

To make the nano-SILs we need to make cylinders of specific diameters for each PMMA thicknesses. We did a few rounds of lithography and tried to calibrate the dose and mask sizes to realize the correct diameter.

For the first round, we made a mask with an array of similar structures with increasing dose. We used a large range of doses and found the dose which resulted in a diameter roughly close to the required one. In the next round we varied the dose above and below this value in increments of $20\mu\text{C}/\text{cm}^2$ with a narrower dose range. This test determined the required dose more accurately.

In the next step of the calibration, we varied the actual diameters in the mask itself. This is because at lower doses there are more droplets of the PMMA left in the empty spaces (Figure 2.1). If we try to control the diameter by varying the dose, we saw that the ones with the smallest diameter (and thus smallest dose) had remaining PMMA droplets. So we selected a dose which is high enough to expose the PMMA completely, and varied the diameter of the mask instead. Another reason for this was that varying the dose did not seem to vary the diameter linearly, thus making our calculations and

calibrations more complicated. Controlling the diameter of the software design mask allowed the variation to be linear and more predictable.

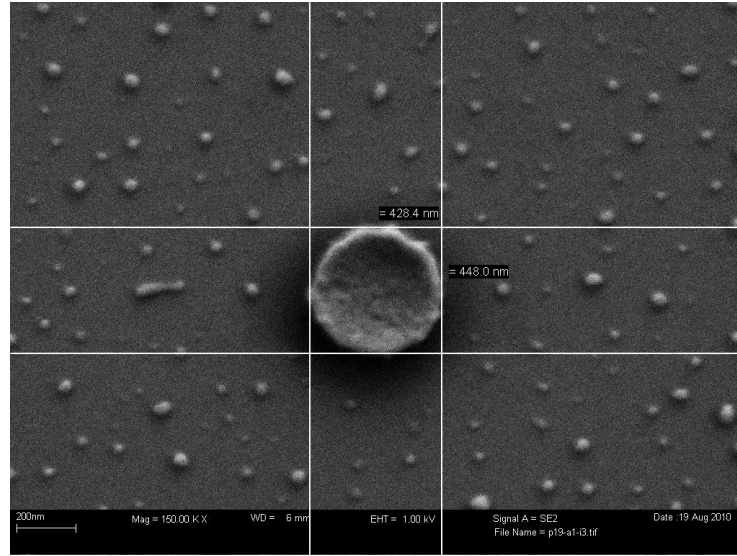


Figure 2.1: Underexposed PMMA- small islands of PMMA visible outside the cylinder

The following table summarizes the results of the calibration runs. Each PMMA thickness had a different ideal dose. The diameter of the circle in the software mask is also shown.

Table 2.3: Dose and diameters for different PMMA nano-SIL shapes

| PMMA thickness(nm) | Dose($\mu\text{C}/\text{cm}^2$) | Software mask diameter (nm) | Required Diameter (nm) |
|--------------------|-----------------------------------|-----------------------------|------------------------|
| 100 | 350 | 385 | 300 |
| 150 | 400 | 555 | 450 |
| 200 | 490 | 710 | 600 |

Once we achieved the required diameters, we performed another round with the same mask and dose to compare the variability between samples, and establish

reproducibility. We found that there was always a variation from chip to chip in the feature size of a few nanometers. Thus we have calibrated the EBL to make PMMA cylinders of the desired diameter.

2.4 Fabrication of Nano-SIL

2.4.1 Complete Fabrication Sequence of Nano-SIL

After the lithography of the PMMA cylinders, the rest of the fabrication of the nano-SILs is done by our collaborators at the Swiss Federal Institute of Technology, Lausanne (EPFL), Switzerland. A short summary of the fabrication process performed by our collaborators is presented below.

The fabrication process for this nano-SIL starts with making cylinders of PMMA of specific dimensions on a silicon substrate, as described in the previous section. PMMA is chosen since it is an electron beam resist and also a thermoplastic and thus it enables the use of thermal reflow. During reflow, the samples are heated to a high temperature which causes the PMMA to partially melt, and surface tension pulls the cylinders into hemispheres. The ratio of height to diameter of the cylinders is critical to ensure the proper hemispherical shape after reflow.

Since silicon is not transparent in the visible, the pattern needs to be transferred to a glass substrate. This is done using a soft lithography process onto glass cover slips, and this time a UV curable polymer (Norland, NOA65) is used. The reflow and replication processes are described in more detail in section 2.6.1.

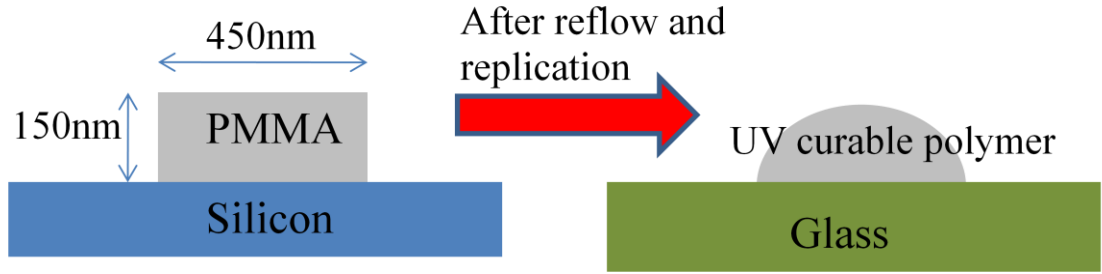


Figure 2.2: Nano-SILs on a transparent substrate are produced from cylindrical islands of PMMA on Silicon substrates using a thermal reflow and replication process, The fabricated devices will then be characterized using a high-resolution interference

The fabricated devices will then be characterized using a high-resolution interference microscope. The reduction in spot size and increase in peak intensity of the spot will reveal the actual optical performance characteristics of the nano-SIL.

2.4.2 Design of Final Device

The proposed design of the PMMA cylinders requires the diameter to be 3 times the height in order to get the correct curvature after reflow. The design parameters are shown below in Table 2.4. Initially there were three designs of the nano-SIL that we attempted to fabricate. After initial lithography, we had several issues with the smallest size nano-SILs, and we discontinued the fabrication of that series (explained in more details in section 2.5.4).

Table 2.4: Design parameters of nano-SIL PMMA cylinders

| Height(nm) | Diameter(nm) |
|------------|--------------|
| 100 | 300 |
| 150 | 450 |
| 200 | 600 |

The final design mask consists of circles written inside a 4 μm square. Since PMMA is a positive resist, the area where the electron beam exposes the resist is actually dissolved away by the developer. Thus the mask was designed to scan the electron beam across a 4 μm square area with a circular gap in the middle.

A row of five of these squares was written with slightly varying circle diameters (15nm diameter increments). This row is then repeated 6 times. Thus there is a 5x6 array of the squares. The spacing of the squares is 50 μm in the horizontal and 40 μm in the vertical direction. The squares are labeled with letters(A - F) indicating rows and roman numerals (I - V) denoting columns. Each square has its own label just above it in small (~ 2 μm) letters, and there are also larger labels(~ 10 μm) along the top and left sides of the array.

The following images (Figures 2.3 & 2.4) show the mask as produced by the design software (DesignCAD).

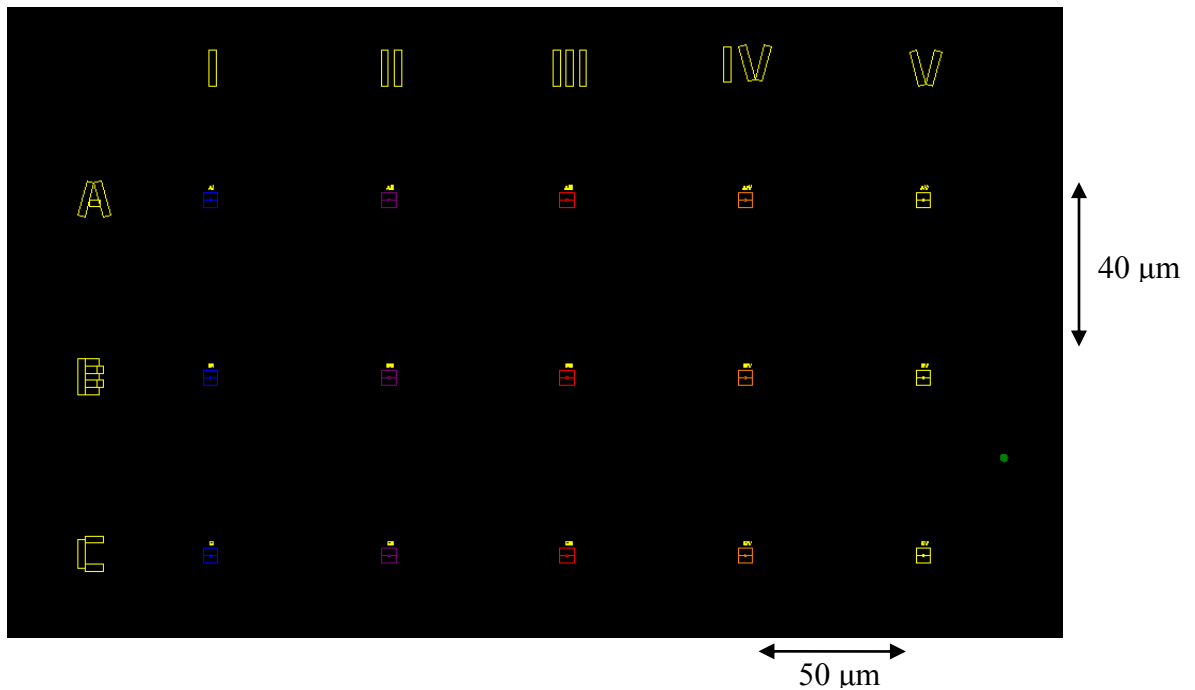


Figure 2.3: Overview of the DesignCad mask for the nano-SILs (there are actually 6 rows, A - F). Each column contains slightly different circle diameters, while the multiple rows provide redundant samples.

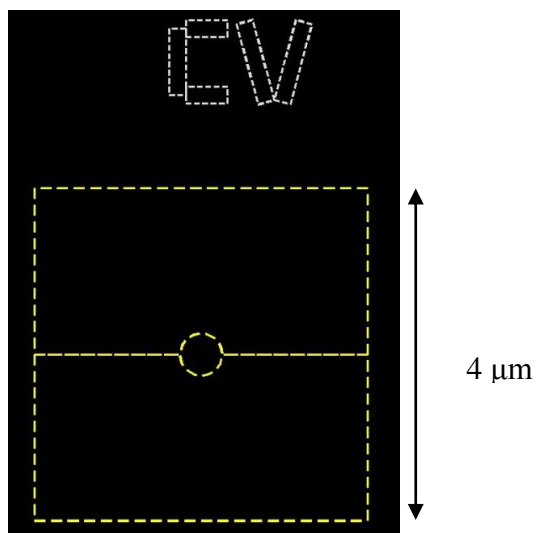


Figure 2.4: Detailed view of one square of the DesignCad mask. Since PMMA is a positive resist, the lithography pattern exposes a square of side dimension $4\ \mu\text{m}$, while leaving an unexposed circle at the center. After development, this produces a “window” of bare Silicon with a PMMA cylinder at its center.

Using this mask design, five final production chips were made. The actual samples which will be used for reflow and replication cannot be imaged after fabrication. This is because we need to coat the sample with metal before imaging due to charging effects, which would make the sample unusable for reflow. Thus, to check for variation and get statistical data, 3 chips were checked during the production run. A total of 8 samples were made, and the first, fourth, and last chip were imaged, and the rest were the actual final samples. This sequence was used for both the 600 nm and 450 nm diameter lenses. Thus we successfully fabricated five samples of each of the two types of nano-SILs, and forwarded them to our collaborators for reflow, replication and characterization.

2.5 Measurement of Nano-SIL Shape after Lithography

As described above, the size and shape of the PMMA cylinders on three sample chips of each type of nano-SIL (450 nm and 600 nm diameter) were measured in detail, and we will now discuss the data sets for both and then compare them.

2.5.1 450 nm Diameter

The size and shape of the nano-SILs in the three chips during the production run were checked in the SEM in detail. There are 6 rows for each column which are supposed to be the same diameter, and the average of the six is calculated. Table 2.5 gives a summary of the data for the 450nm diameter lenses.

Table 2.5: Measured diameter data for 450 nm diameter nano-SIL (all units in nanometers)

| Column | I | II | III | IV | V |
|----------------------------------|-------|--------|--------|--------|--------|
| Expected diameter | 420 | 435 | 450 | 465 | 480 |
| Average measured diameter of p18 | 424 | 448 | 454 | 475 | 484 |
| Average measured diameter of p20 | 418 | 446 | 458 | 474 | 487 |
| Average measured diameter of p38 | 415 | 430 | 446 | 466 | 471 |
| Average for 3 chips: | 419 | 441.33 | 452.67 | 471.67 | 480.67 |
| SD among 6 rows and 3 chips | 9.21 | 12.97 | 7.71 | 7.96 | 12.14 |
| Max deviation from mean | 18.03 | 26.60 | 13.19 | 20.63 | 35.93 |

The average diameters of the three chips for each column are fairly close to the expected values. Each chip does show a variation or bias above or below the expected values. Another issue is the variation of the diameters of the lenses within the same chip and column. It is difficult to statistically analyze and differentiate between these two types of variation. This is because there are only three samples, and thus the data population is not large enough to derive any statistical conclusion about the chip-to-chip variation. The standard deviation for all the rows among the three chips is calculated. This takes into account both types of variation. The maximum standard deviation (SD) among the five rows is 12.97 nm. We also calculated the deviation from the mean for each data set, and the maximum of this deviation for each column is shown. The maximum deviation among all the measurements is 35.93 nm.

We also noticed the shape of the cylinders from top view were not always perfectly circular. The average difference between the horizontal and vertical diameters is 1.27%. The horizontal diameter usually was slightly larger. We did not investigate this effect further, as it was assumed that a small anomaly in the symmetry of the cylinders (on the order of a few nanometers) would not significantly affect the shape of the nano-SILs after thermal reflow.

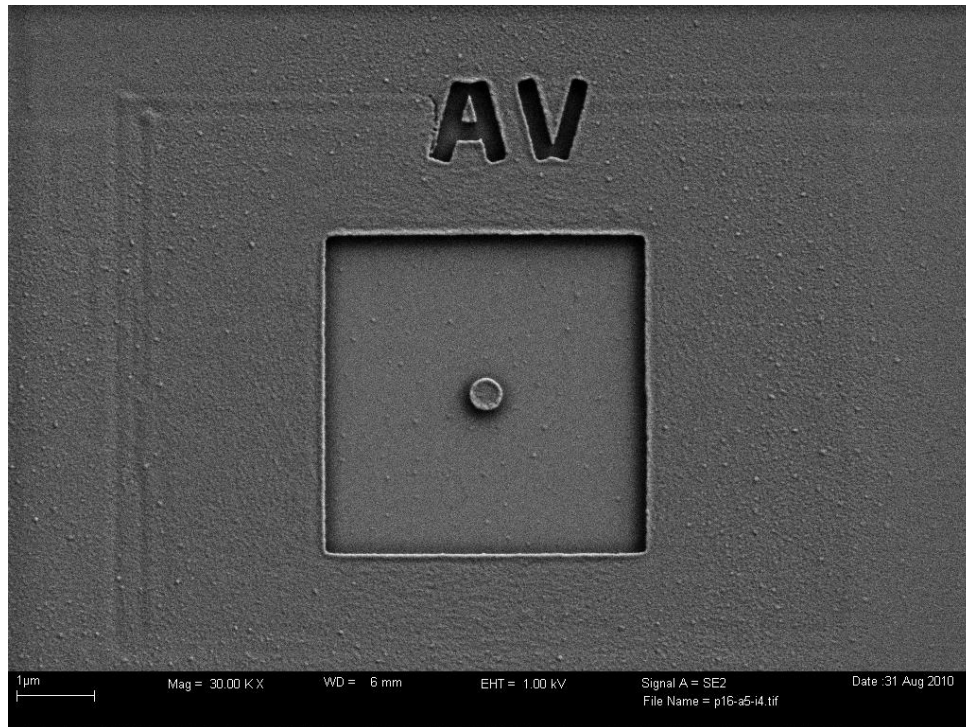


Figure 2.5: A single square of a 450 nm diameter nano-SIL sample after lithography

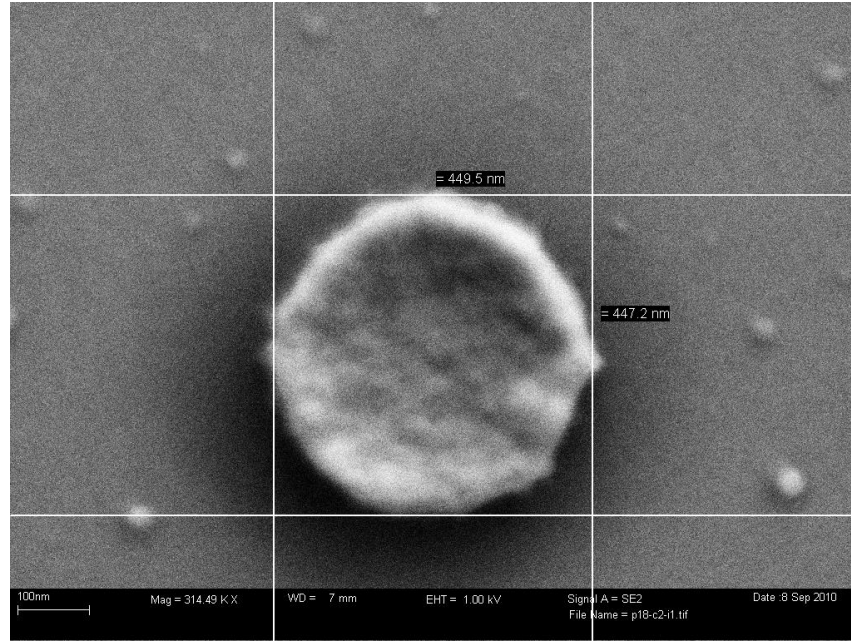


Figure 2.6: Magnified image of one PMMA cylinder, showing diameter measurements in the horizontal and vertical direction

2.5.2 600 nm Diameter

Table 2.6: Measured diameter data for 600 nm nominal diameter nano-SILs (units are all nanometers):

| Column | I | II | III | IV | V |
|----------------------------------|--------|-------|--------|--------|-------|
| Expected diameter | 560 | 580 | 600 | 620 | 640 |
| average measured diameter of p52 | 561 | 580 | 614 | 621 | 650 |
| average measured diameter of p57 | 566 | 576 | 607 | 618 | 652 |
| average measured diameter of p48 | 567 | 575 | 602 | 617 | 642 |
| Average for column: | 564.66 | 577 | 607.66 | 618.66 | 648 |
| SD among 6 rows and 3 chips | 8.01 | 11.11 | 12.28 | 9.62 | 9.84 |
| Max deviation from mean | 21.98 | 32.28 | 29.05 | 22.00 | 25.25 |

The summary of the 3 chips with 600 nm diameter PMMA cylinders that were characterized (P52, P57 and P48) is shown in Table 2.6.

Once again, the average diameters of the three chips for each column are fairly close to the expected values. The maximum standard deviation for the columns was 12.98 nm. The horizontal diameters were found to be larger than the vertical by an average of 0.46%. Among the whole data set, the maximum of the deviation of the measurements from the mean is 32.28 nm.

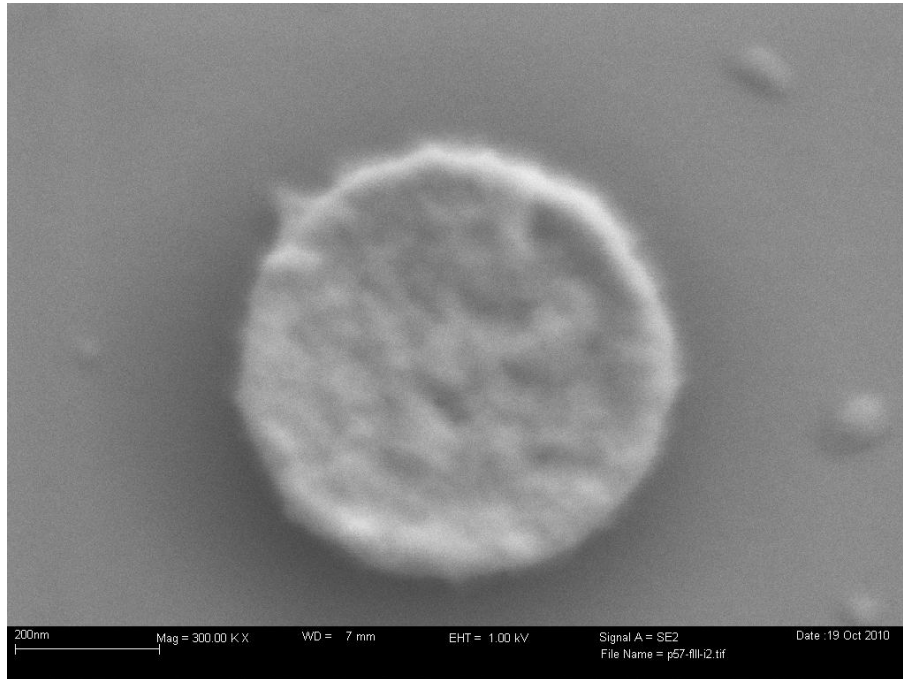


Figure 2.7: Magnified image of one PMMA Cylinder of a 600nm nominal diameter nano-SIL

2.5.3 Comparing 600 nm and 450 nm Nano-SILs

The following graph shows the expected and actual diameters (average of the 3 chips of each) for the two types of lenses. For the 600 nm diameter, columns 1, 3 and 5

shows a higher average measured diameter than the expected, but for the other type of nano-SIL, columns 2 and 4 show a higher average measured diameter.

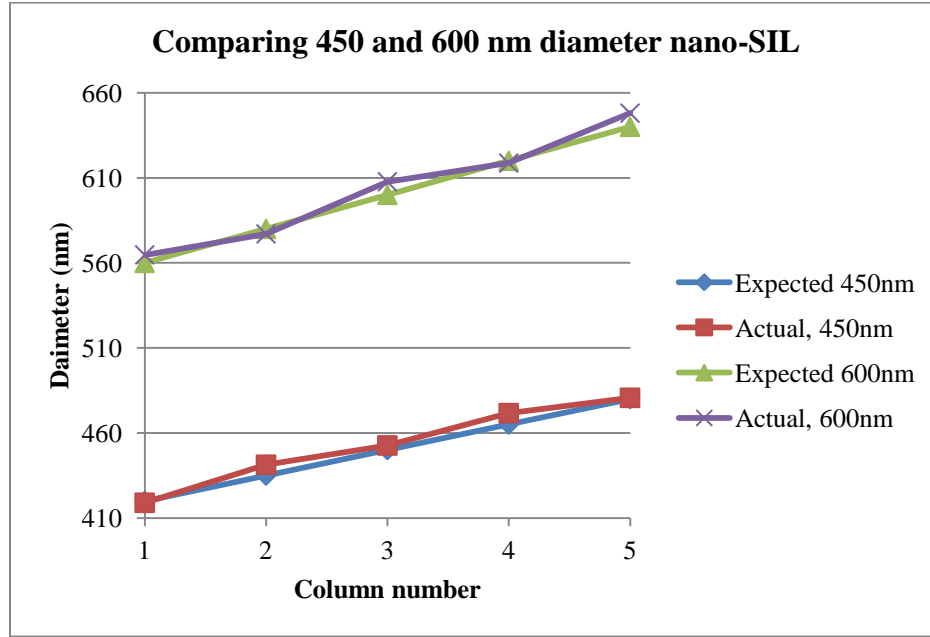


Figure 2.8: Comparing measured and expected diameters after lithography of the two sizes of nano-SILs

Table 2.7: Comparing statistical data between the two types of nano-SILs

| | 450 nm Diameter | 600 nm Diameter |
|------------------------|-----------------|-----------------|
| Max SD for all columns | 12.97nm | 12.28nm |
| Ellipticity | 1.27% | 0.26% |

Both of the nano-SIL designs show similar fabrication tolerances (see Table 2.7). This is of course expected since the size scale is very similar and the fabrication process is essentially the same. The standard deviation among the two types is very similar. The 450 nm diameter samples exhibit a slightly larger ellipticity, but still small enough to be

not too significant, since it corresponds to a bias of about 6 nm between the horizontal and vertical diameters, which is well within the standard deviation.

The line edge roughness is estimated to be approximately 20 nm, for both types of nano-SILs. Although this increases variation in measurement of diameter, it is not a big issue since in subsequent steps the lens will be reflowed.

The shape measurements of these six samples gave us a good idea of what to expect for the actual samples used for characterization. Although there was some variation of size for each cylinder, the average diameters were close to expected.

2.5.4 Issues with 300 nm Diameter Nano-SILs

We fabricated the 300 nm diameter nano-SILs using the same process as the larger sizes. However we had several issues that we discovered after lithography.

The first issue is that the PMMA lenses seem to be more hexagonal in shape than circular. Also since the size scale is smaller, the variation in roughness and shape seems to be more pronounced (i.e. the variation is larger when compared to the diameter). Estimating from a few pictures, the edge roughness is observed to be up to 30-40 nm, which corresponds to 10%-13% of the diameter.

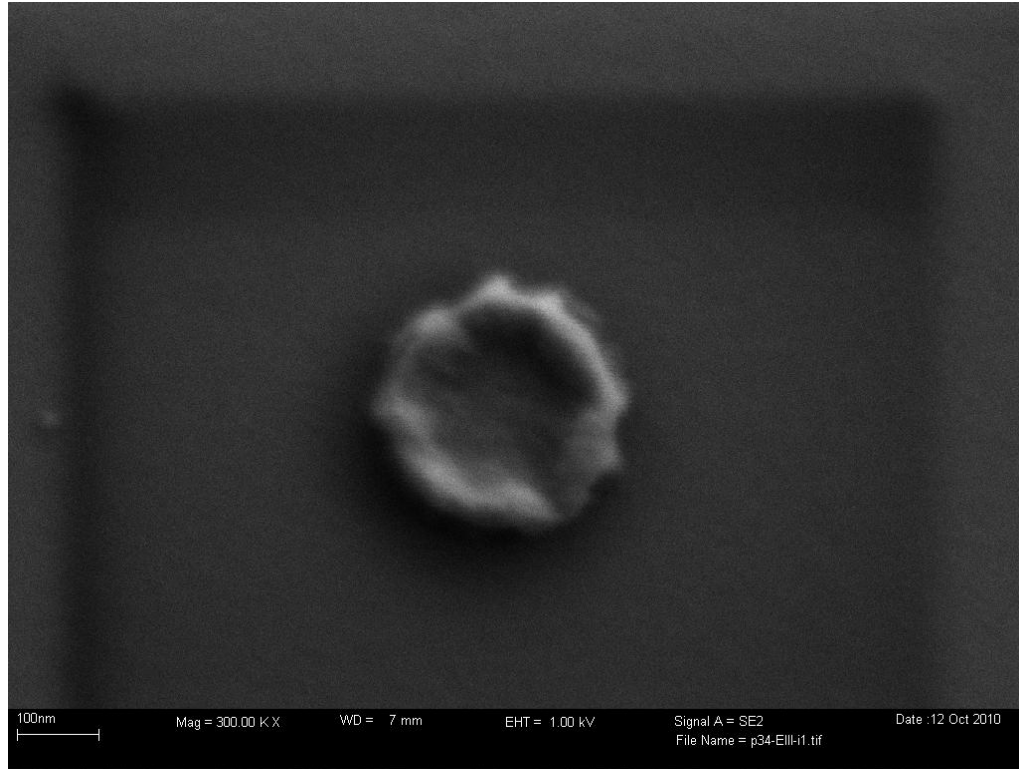


Figure 2.9: Magnified image of a 300 nm diameter nano-SIL

Another issue is that the circular patterns appeared to have a rim, that is, the surface appeared to be slightly raised near the edge of the pattern. This was also present in the larger diameter nano-SILs, but the effect seems to be more pronounced for the smaller diameter samples. Because of these issues we estimated that there would be large uncertainties in the size/shape measurements and also the non-ideal shape may not produce the desired hemispherical lenses after reflow. Thus we discontinued production of this series of nano-SILs.

2.5.5 Shape Measurements After Reflow and Replication

The samples were again measured for diameter and height after the reflow and replication processes (described in Section 2.6.1 below). Once again the samples were

coated with iridium to prevent charging effects and then the diameters were measured in the SEM. To measure the height, Atomic Force Microscopy (AFM) was also used. The height of the lens and the substrate (step height measured at the edge of one of the 4 μm squares) were measured separately. The detailed measurement data of one row of P20 (450nm diameter nano-SIL) is shown in Table 2.8.

Table 2.8: Sample measurement data for 450 nm nominal diameter nano-SIL after reflow and replication (units in nanometers)

| | Height of lens | Height of substrate | x-axis diameter | y-axis diameter | Average Diameter |
|---------|----------------|---------------------|-----------------|-----------------|------------------|
| A1 | 48 | 72 | 509 | 533 | 521 |
| A2 | 54 | 92 | 523 | 555 | 539 |
| A3 | 56 | 87 | 537 | 511 | 524 |
| A4 | 57 | 77 | 532 | 569 | 550.5 |
| A5 | 48 | 85 | 550 | 546 | 548 |
| Average | 52.6 | 82.6 | | | |

The diameters were measured both in x- and y- direction, and then averaged. Note that the difference in diameter between the two axes does not indicate ellipticity, but is due to the very high uncertainty in measuring the diameter (because it is difficult to identify the edges of a sloped object). The very small height difference between the top of the lens and the bottom, and the smooth slanting edge made it difficult to measure the diameters.

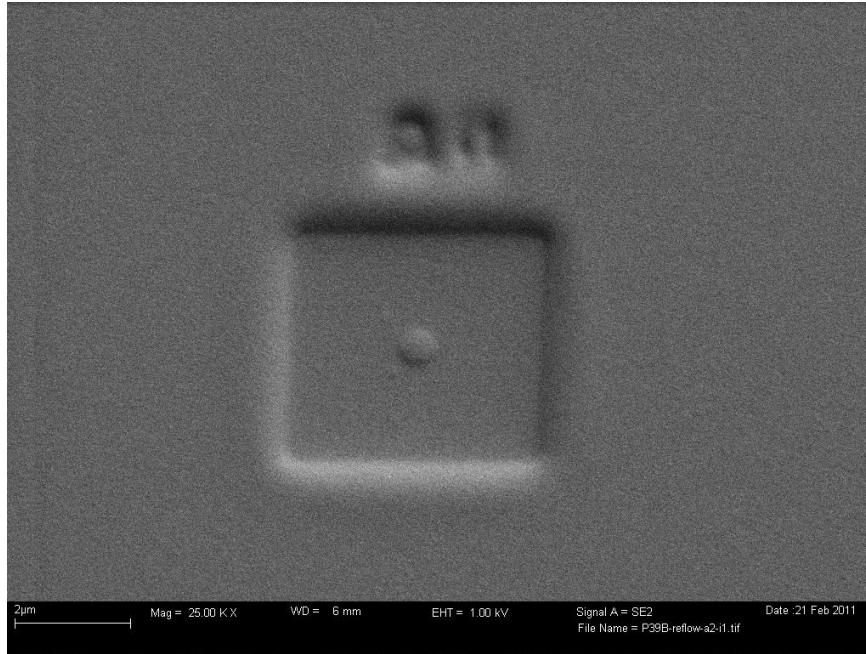


Figure 2.10: SEM picture of a nano-SIL after reflow and replication

After several measurements and averaging, it is estimated that the 600nm cylinder was transformed into a spherical cap with a diameter of 700 nm and a height of 54 nm, which yields a radius of curvature (ROC) of 1.16 μm . The 450nm cylinder was transformed in to 530 nm diameter and 45nm height spherical cap (ROC = 781 nm).

The shape measurements after reflow gave us an estimate of the actual shape of the lenses. This would allow us to better interpret the characterization data.

2.6 Nano-SIL Fabrication and Characterization by our Collaborators

After the lithography of the nano-SIL, the reflow and replication processes were performed by our collaborators. Next, we measured the dimensions of the finished nano-SILs (as described in Section 2.5.7 above), and finally the optical characterization was also done by our collaborators. This is a summary of their work [37].

2.6.1 Reflow and Replication Process

PMMA is a thermoplastic, and a thermal reflow process can be used to change the shape of the cylinders to hemispheres. The 600 nm diameter cylinders are reflowed at 150° C for 20 minutes on a hot plate, and the 450 nm cylinders at 140° for 20 minutes.

Since the lithography was done on a silicon substrate, which is not transparent to visible light, the reflowed lens patterns needed to be transferred to a glass substrate. A soft lithography technique was used to do this [45]. An elastomeric polymer, such as poly-dimethylsiloxane (PDMS) is used as a mold or stamp to transfer the pattern. PDMS is poured over the main sample, and cured and then peeled off. The PDMS retains the surface relief features of the main sample, and it is then pressed on to a glass substrate (borosilicate glass cover slips, thickness = 150 μm , $n = 1.52$) coated with another UV-curable polymer (Norland , NOA 65, $n = 1.52$). Once this polymer is cured, the mold is removed, leaving a replica of the original sample on the glass cover slips.

2.6.2 Optical Characterization

For optical characterization, a high-resolution interference microscope [46] was used to measure the three dimensional field distributions. An immersion objective (100X/NA1.4) was used so that the sub diffraction fields from the nano-SIL could be resolved by the imaging system. To measure the reduction in spot size, the full width half maximum of the intensity profile of the focal spots were compared. The reduction ratio was about 1.35, compared to an ideal reduction ratio of 1.5, which is the refractive index of the nano-SIL. This is probably due to the non-ideal shape of the lens. The peak intensity was also measured to be approximately 50% higher than the reference value.

These results show that the fabricated nano-SILs do indeed work as a sub-wavelength solid immersion lens.

2.7 Conclusion

The fabrication of the nano-SILs gave us an opportunity to test our capabilities in electron beam lithography. We have demonstrated the spinning of precise PMMA layers of different thicknesses. We have calibrated electron beam lithography for the nano-SILs and demonstrated the capability of controlling the feature size of patterns by varying the dose and software mask feature size. These process optimizations and improvements have allowed us to assist in the fabrication of the nano-SILs.

We have contributed to the fabrication of the nano-SILs, by fabricating 450 and 600nm diameter PMMA cylinders. The results of this project are published in Optics Letters [37]. We have performed detailed measurements of the nano-SILs after lithography and after reflow and replication, and analyzed the results.

The fabrication of the nano-SILs has given us an understanding of the lithography process. This experience in process improvement will help us to further calibrate and optimize the lithography processes. Now that we have demonstrated our capabilities of EBL in fairly simple structures, we will move on to more complicated devices such as the AR grating and mid-infrared polarizing beam splitter.

FABRICATION OF ANTI REFLECTIVE GRATINGS IN SILICON

3.1 Introduction

For many optical devices that operate in transmission, such as lenses, a reduction in reflectivity generally improves the performance characteristics. A common method of doing this is using a thin single or multiple layer coating of materials with the right indices of refraction which use the principle of interference to reduce reflection. An antireflective (AR) nanostructure is another method of reducing reflection. The benefit of using nanostructures for this purpose is that the AR layer can be engineered using the same materials as the device. Furthermore, if a common material, such as silicon, is used, the nanostructure could relatively easily be integrated with other devices, such as MEMS. Using a modeling method such as effective medium theory [47], we can design the structure so that for a certain wavelength band the reflectivity is minimized.

The simplest AR structure is a 1-dimensional (1D) rectangular grating etched into a silicon substrate. This grating has a different effective refractive index for different polarization states of incoming light, and thus would be designed to have minimum reflectivity for one linear polarization state. In the literature, there are simulations of 1D rectangular [1-2] and other structural types of gratings [3-4], as well as experimental results from many kinds of AR structures [5-10].

The main motivation for producing this type of structure is its potential for integration with optical MEMS devices. Since optical MEMS uses similar silicon fabrication processes, it would be relatively easy to fabricate this structure on an existing

MEMS device. This would be a good starting point for an integrated device made with one of our collaborators, Dr. David Dickensheets of MSU.

Fabricating the AR grating would require optimizing all the processes up to etching (steps 1 through 7 in Figure 1.1). Since the grating itself is not structurally complicated, using it to do process optimization would be relatively easy and would let us use this simple structure to develop fabrication processes. Many other optical nanostructures, such as the polarizer from Chapter 4, are based on a grating structure, and thus the process optimization for this structure can easily be scaled or adapted for other more advanced devices.

3.2 Calibrating Mask Patterning for 1D Gratings

3.2.1 PMMA Bilayer Spinning and Liftoff Process

The spinning of a resist layer is often the very first step in any nanofabrication process chain. Our standard recipe involves spinning a bi-layer PMMA resist. This technique was developed mainly for liftoff, and was first patented in 1976 by Moreau and Ting [48]. This is a standard technique, and the exact recipe we use was developed by other research groups.

The lower layer of the bilayer is a lower molecular weight PMMA (495000) and the top layer is a higher molecular weight PMMA (950000). This process is used due to the fact that after exposure and development, a profile with a slight undercut is achieved. This is very important in the liftoff process, since it produces cleaner, more sharply defined edges in the mask.

For the first layer we use a 2% solution of 495K PMMA in Anisole. This is spun for 30 s on to the sample at a spin speed of 4500 RPM. The sample is then soft baked on a hotplate at 115°C for 30 s. This evaporates away most of the solvent from the PMMA. The second layer is a 3% solution (in Anisole) of 950K PMMA. This is spun at 4000 RPM for 30 s, followed by a soft bake of 1 minute and 45 s at 115°C.

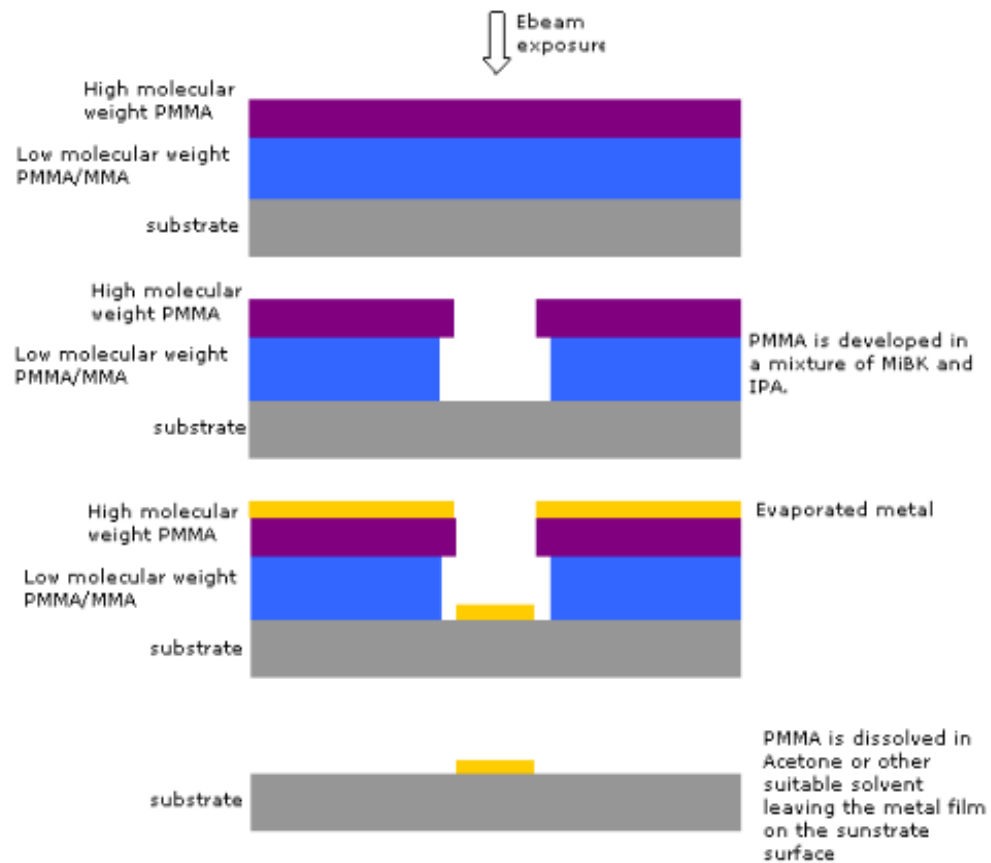


Figure 3.1: Bilayer PMMA and liftoff process

After lithography, the required pattern is realized in the resist. However the resist, PMMA, is too soft to be used as an etching mask for ICP etching, since the plasma would etch away the resist too quickly. Thus the pattern must be transferred to a harder mask,

such as aluminum. This is done by a lift-off process which leaves the inverse of the PMMA mask pattern in the aluminum.

First the aluminum is deposited using an evaporation tool. We use an electron beam evaporation tool, the Amod Evaporator by Angstrom Engineering, to deposit 80nm of aluminum on top of the patterned PMMA bilayer. Aluminum adheres to the silicon in places in the pattern where the PMMA is removed by development, and everywhere else the aluminum layer sits on top of the PMMA. This aluminum on top of PMMA is then removed or “lifted off” by dissolving away the PMMA layer. This is done by soaking the sample in acetone in an ultrasonic bath, which helps the liftoff process with physical motion.

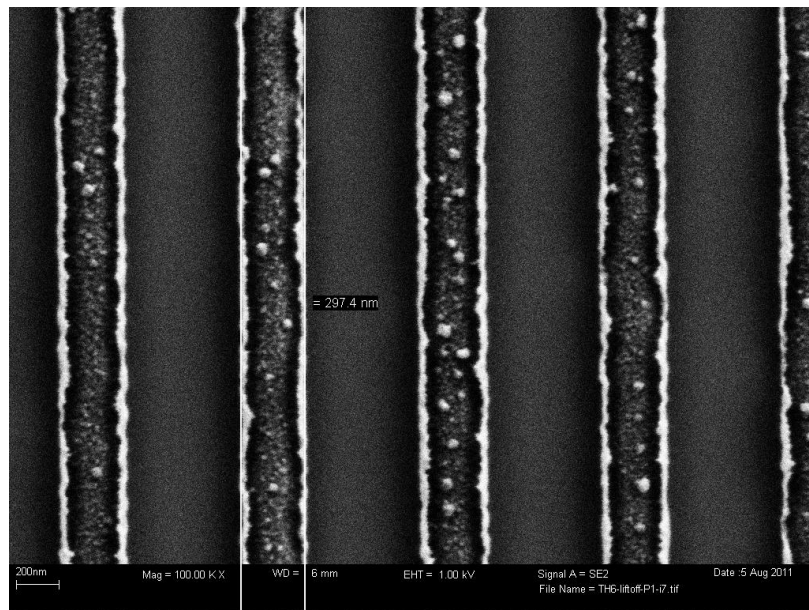


Figure 3.2: SEM image of lifted off grating, showing aluminum mask on silicon substrate

After liftoff, the Aluminum pattern remaining is the direct “Positive” image of the original design mask. An SEM picture of a lifted off grating is shown in Figure 3.2.

The PMMA bilayer and liftoff processes are standard techniques on which we have not done any process improvement, but we have used these processes for the fabrication of different devices and have so far proved to be sufficient for our fabrication requirements.

3.2.3 Calibrating EBL for 1D Gratings

In order to make the AR grating we first performed a calibration of the lithography process to make 1D gratings of the right dimensions. Before we could start with the process calibration, we had to calibrate an inherent error in the magnification of the SEM. This is due to a non-ideal calibration of the SEM. This results in a small scaling error, and thus a small error in the dimensions measured in the SEM. We measured this error by taking multiple measurements of the period of a calibration sample at different magnifications. We found that the horizontal scaling was 102.29% and the vertical scaling was 102.48%. Thus all measurements needed to be adjusted down by these scaling factors.

To calibrate the relationship between the software mask line width (LW) and the actual Aluminum mask (hard mask) line width, we first chose to make a 1-D grating of a line width in the range of 500 nm–600 nm. This was chosen for one of our other devices, the infrared polarizer (discussed in Chapter 4). We made an array of gratings with increasing line width, and after lithography and liftoff, we measured the line width of the aluminum hard mask. We expected the final LW to be about 80nm larger than the

software LW, a value estimated from previous tests. Note that in this case the software mask has to be made smaller than the expected final feature size, whereas in Chapter 2 we have shown that for the PMMA cylinders, the reverse was true. The difference is that for the PMMA cylinders, we were actually exposing the square area around the desired circular feature, and not the target area itself. Table 3.1 shows the data and the relationship between the input (software mask) and output (Aluminum hard mask) line width.

Table 3.1: Table showing data relating software and hard mask line width. All units are nanometers.

| Pattern number | Software Mask line width | Expected final line width | Al hard mask line width | Difference of soft- and hard- mask LW |
|----------------|--------------------------|---------------------------|-------------------------|---------------------------------------|
| P1 | 410 | 490 | 481.64 | 71.64 |
| P2 | 430 | 510 | 502.49 | 72.49 |
| P3 | 450 | 530 | 522.70 | 72.70 |
| P4 | 470 | 550 | 534.10 | 64.10 |
| P5 | 490 | 570 | 562.13 | 72.13 |
| P6 | 510 | 590 | 594.06 | 84.06 |
| P7 | 530 | 610 | 615.24 | 85.24 |
| P8 | 550 | 630 | 640.34 | 90.34 |
| P9 | 570 | 650 | 659.89 | 89.89 |

Next we repeated this test with a smaller spread of line widths. This test gave us a second set of data and gave us information about reproducibility. The results of both of these tests were plotted together, with the software mask LW (input) on the x-axis and Aluminum Hard mask LW (output) on the y-axis (see Figure 3.3). Also included in the same graph is the data from another sample with a smaller range of feature sizes

(experiment described in Section 3.7). This gives us an approximate look up table which we can reference later to get data on how to design the software mask for a certain required feature size. The linear best fit line for each data set does not coincide very closely, but they do show a similar trend. These differences are probably due to errors and various fabrication and measurement inconsistencies which result in a small difference in feature size from one run to the next. Note that all these three tests were performed with a dose of $260 \mu\text{C}/\text{cm}^2$, and a different dose will surely give a different trend.

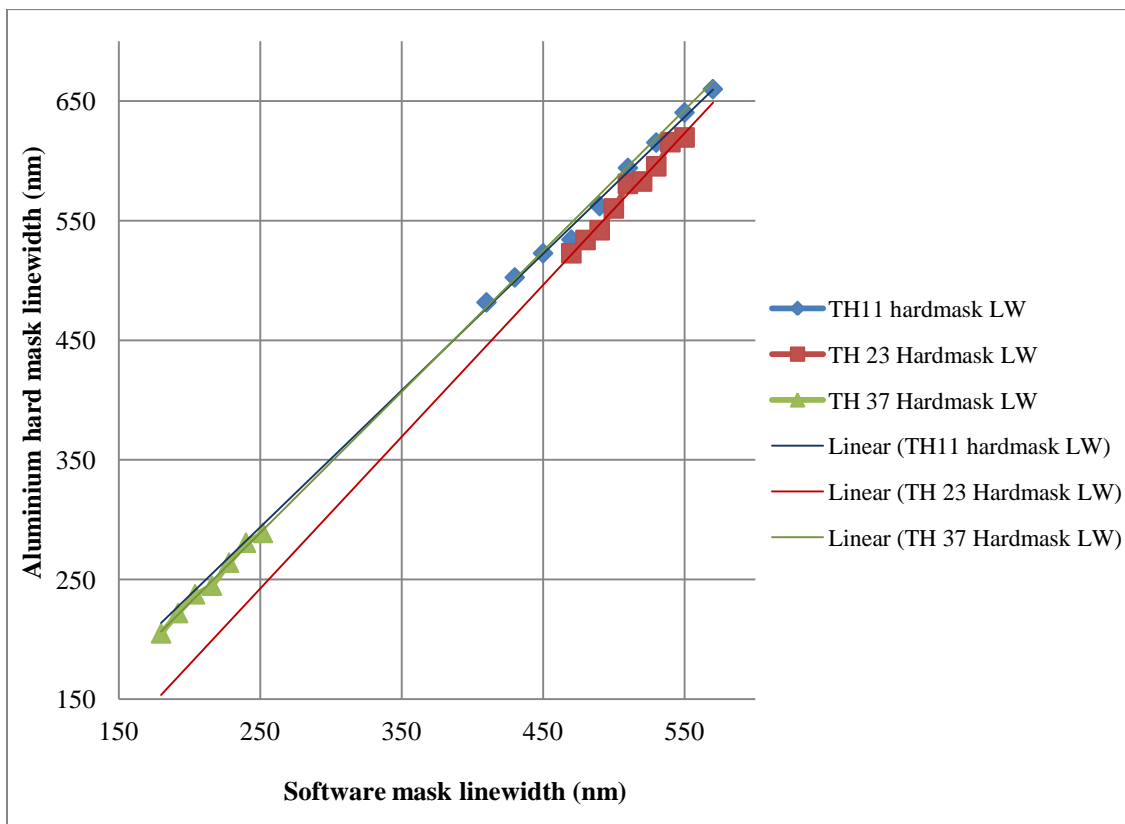


Figure 3.3: Graph showing relation of software and hard mask line width for 3 different samples. The linear trend lines are also plotted.

We may use this graph to predict the size of structures to be implemented in the design software which will give us the required final hard mask feature size. This can only be used as an approximation, but it can help us by saving us from performing at least one round of calibration whenever we make a new device. Thus we have completed a preliminary calibration of EBL for the line width of 1D gratings.

3.5 Etching

3.5.1 ICP-RIE Etching

After the liftoff process the sample has the metal hard mask, and now the pattern can be etched into the silicon substrate using a dry etching step. We use an Inductively Coupled Plasma – Reactive Ion Etching (ICP-RIE) process. The equipment for this is an Oxford Plasmalab System 100 [49]. This dry etching process uses a combination of physical bombardment of ions and chemical reactions to etch away the silicon substrate, leaving the Aluminum mask mostly intact. The recipe we use uses SF_6 and CHF_3 gases. SF_6 supplies Fluorine, which is the main etchant for silicon, and the CHF_3 helps in the passivation of the sidewalls, which decreases etching in the horizontal direction.

The RIE-ICP etching process is very sensitive to different chemicals and molecules in the chamber [50-51]. We have noticed that even very slight contamination will cause a significant change in the etching chemistry and thus alter the etch rate and process. We have learned from trials that previous use of the machine (especially if different gases have been used) and the opening/venting of the chamber will affect the

next run. Thus we implement several processes before the actual etch run to clean the chamber and create a stable and consistent starting point for the etching.

Table 3.2: ICP-RIE recipes used for silicon etching

| | Oxygen plasma clean | Seasoning | Etching recipe |
|-------------------------|---|--|--|
| RIE Power (W) | 30 | 10 | 30 |
| ICP Power (W) | 1200 | 1200 | 1200 |
| Temperature (°C) | 25 | 20 | 20 |
| Plasma pressure (mTorr) | 40 | 15 | 15 |
| Gas Flow rates (sccm) | O ₂ - 10 SF ₆ - 50 | CHF ₃ - 50 SF ₆ - 7.5 | CHF ₃ - 50 SF ₆ - 7.5 |
| Time(min) | 15 | 15 | varies |

First we perform an oxygen plasma clean process. This process flows oxygen through the chamber and the oxygen plasma, being highly reactive, oxidizes any organic materials in the chamber, and the by-products are pumped out through the vacuum system.

Next we perform a “seasoning run”. This uses the same recipe as our actual etching step, but is run for a longer period of time. This step “seasons” the chamber, coating the chamber walls with the same chemicals being used for the etching process. This creates a stable initial environment for the etching, thus minimizing the effects due to previous users of the system. After some preliminary testing, we have settled on a 15min seasoning time as the standard process in our work.

The various process parameters for the cleaning, seasoning and etching steps are shown in Table 3.2.

3.5.2 Etchrate Calibration

One of the main problems we faced when calibrating the etching recipe is an etch rate inconsistency. The rate varied quite a bit from run to run. There are several factors which we know can affect the etching rate.

We have previously used the thermal oil “Fomblin” to obtain good contact between the sample chip and the handle wafer which is loaded into the instrument. However we have noticed that this oil is not completely removed with standard solvents when we tried to clean the wafer after the etching is completed. It left residues which affected the next time the handle wafer was used in etching. Later we switched to “Santovac” thermal oil, which is completely removed by acetone, and thus leaves no residues. Switching to the new oil itself did not seem to have any effect on the etching rate itself, as was expected.

The handle wafers used gradually get dirtier with each subsequent use, with the collection of residues from the oil or the handling using tweezers. We noticed that the condition of the wafers is also a factor which affects etch rate.

Even after considering all of these issues and trying to control them, we still had a significant etch rate inconsistency. As can be seen in Fig. 3.4 the rate varies from about 3.0 to 3.7nm/s. There are a few conclusions we can deduce from this graph. The points in the graph in red (run numbers 3, 11 and 14) are the etch runs which used new handle wafers. For the first two, we did not clean the handle wafers before using them in etching, and we can see that these both times there was a large dip in the etch rate. The third time the handle wafers were cleaned using an RCA clean process (a standard wafer cleaning

process involving a sequential organic clean, oxide strip and ionic clean) and this did not result in an etch rate dip. This indicates that using a new wafer without cleaning will decrease the etch rate and if cleaned will not affect the rate. There are still other jumps and variations in the graph which we haven't found an explanation for. Thus we have identified several issues which potentially affect the etch rate, and although we have improved the stability, it is still not good enough for our requirements.

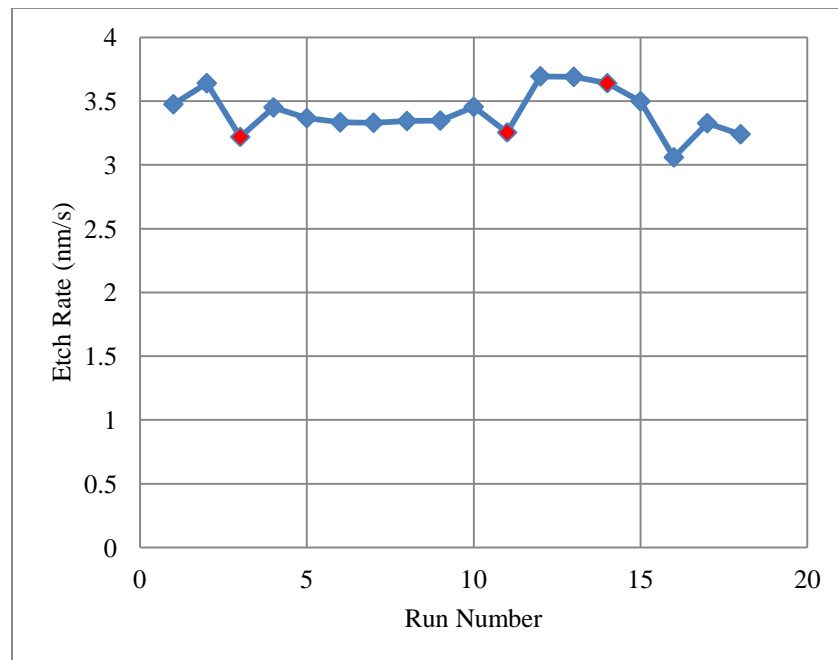


Figure 3.4: Graph showing variation of etch rate over several trials

Although we could not stabilize the etch rate itself we found a solution which enables us to achieve very precise etching even with this slightly unstable etch rate. This “multi-step etching process” is simply an incremental etching which is done on the same sample. The idea is that we etch the sample for some time and then check the depth, and then etch it some more based on how much more etching needs to be done.

To test out this process we used a sample which was already lifted off and ready to etch. This sample was a 1-D grating with a period of 800nm and a fill factor of 50%. We know that this device could potentially work as an AR grating and thus after simulation we found that it would give lowest reflectivity with an etch depth of 360nm. Thus we aimed to etch this device for 360 nm depth.

Along with the actual device, DH5, we also put in three other samples: TH11, BA (etch test gratings) and TH23 (sample with same exact grating as original device). For the first round we wanted to etch for slightly under the 360nm required depth, since we can etch it again if it is under-etched, but if it is over etched we cannot compensate.

Using the average etch rate of 3.405 nm/s, the required etch time is 106 s. Thus we decided to etch for 100 s. Also we calculated that if the etch rate was higher, then the highest recent etch rate (3.6 nm/s) would give us 360 nm depth. Thus we were within the margin of tolerance for the inconsistent etch rate.

After the first etch run we took out sample TH11 and we found the depth to be 325 nm. So for the remaining 35nm, we etched the samples for 10 more seconds. After etching we checked the depth using the TH23 chip and found it to be 354 nm. We could not check the depth of the actual sample, DH5, since that requires cleaving the sample which would make optical characterization of that sample impossible. We however checked the depth of the other sample, BA, and it was found to be 351 nm. Since both the depths for BA and TH23 agreed to within 3 nm, we assumed the DH5 sample to have a depth very close to these values. The etch profile was also as expected, with a sidewall angle of 4.36° with the vertical.

Table 3.3: Multistep etching results of DH5 sample, showing expected and measured etch depths after first and second round of etching

| | First round etching | Second round etching |
|--|---------------------|------------------------------|
| Time | 100 s | 10 s |
| Expected depth calculated using average rate | 341 nm | 360 nm |
| Measured final depth | 325 nm (TH11) | 354 nm (TH23) 351 nm (BA) |

With the successful etching of this device we can conclude that even though we did not solve the etch rate inconsistency, we found a solution to etch samples precisely, within less than ± 10 nm variation from the expected depth. Using this method we have also successfully etched two other devices, described in Section 3.7 and Chapter 4 both having less than 10 nm etch depth error.

3.7 Fabrication of AR Gratings

So far we have calibrated the necessary processes and demonstrated the capability to make 1-D gratings in silicon. Thus we can move on to making an antireflective grating which we can model, fabricate and then characterize, demonstrating that it works.

The design specs of the AR grating were chosen by modeling using Rigorous Coupled-Wave Analysis [52]. This design was chosen by first selecting a 800 nm period, and then modeling for the etch depth and fill factor which gave minimum reflection at TM polarization.

The design parameters chosen were a line width of 280 nm on a period of 800 nm (35% fill factor), and a grating etch depth of 280 nm.

While selecting the design parameters, we also need to take into account the sidewall angle of the grating due to etching. After etching we have seen that the grating sidewalls are not perfectly vertical, and have an average of about 6 degrees slant with respect to the vertical. This arises from etching anisotropy, and is shown in Figure 3.5. Taking into account this slant, the average line width of the etched grating will be larger than the aluminum mask line width. Thus we calculated a required aluminum mask line width of 259 nm to get the required line width after etching.

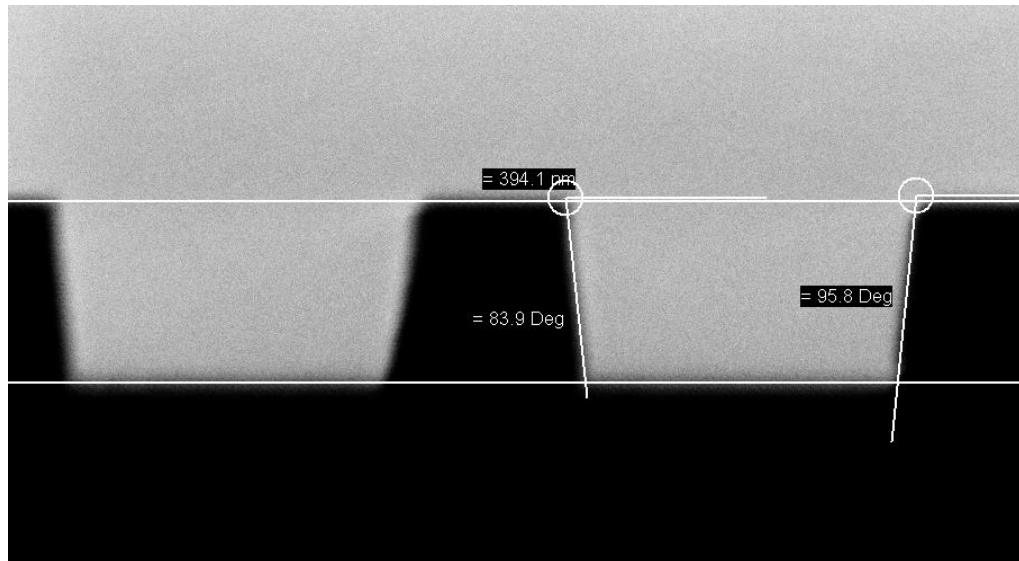


Figure 3.5 SEM profile view of an etched grating showing sidewall slant. The silicon substrate is the top half (lighter area) of the picture.

This is a smaller feature size than previously written, but the trend shown in Figure 3.3 could still be used to estimate the software line width required. Using the graph we estimated the soft mask line width to be 216 nm. We decided to test this by writing an array of seven gratings with line widths varying in increments of 12 nm,

centered on 216 nm. The dose was left unchanged at $260 \mu\text{C}/\text{cm}^2$. After liftoff, we measured the sample and the results of the measurements are included in Figure 3.3.

Following this test we made the final design of the AR grating as a software mask of 3 grating pads spaced 1 mm apart, the center having a line width of 216nm, and the other two with a ± 20 nm line width.

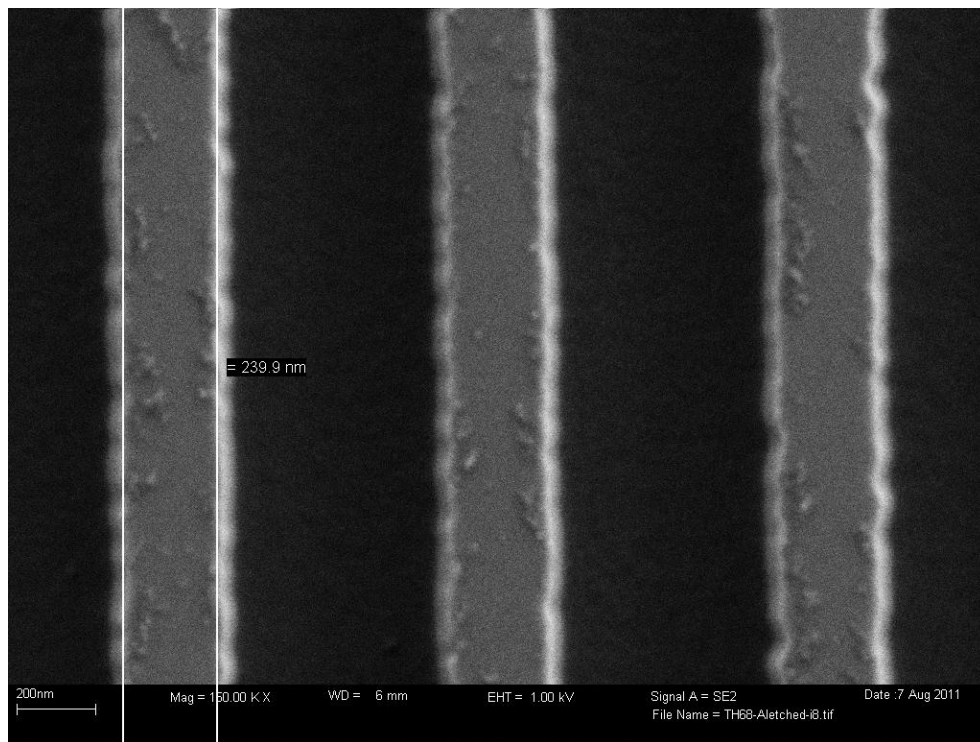


Figure 3.6: SEM picture of TH68 sample, showing a measurement of upper line width

The sample (TH68) was fabricated using the same processes as before, and a multistep etching process was used. We had some fabrication problems during lithography which resulted in parts of the grating being not lifted off. This left some areas of the $300 \mu\text{m}$ grating unusable. However, our characterization set-up needs an area of less than $100 \mu\text{m}$ for free space measurements, so we could still characterize the device.

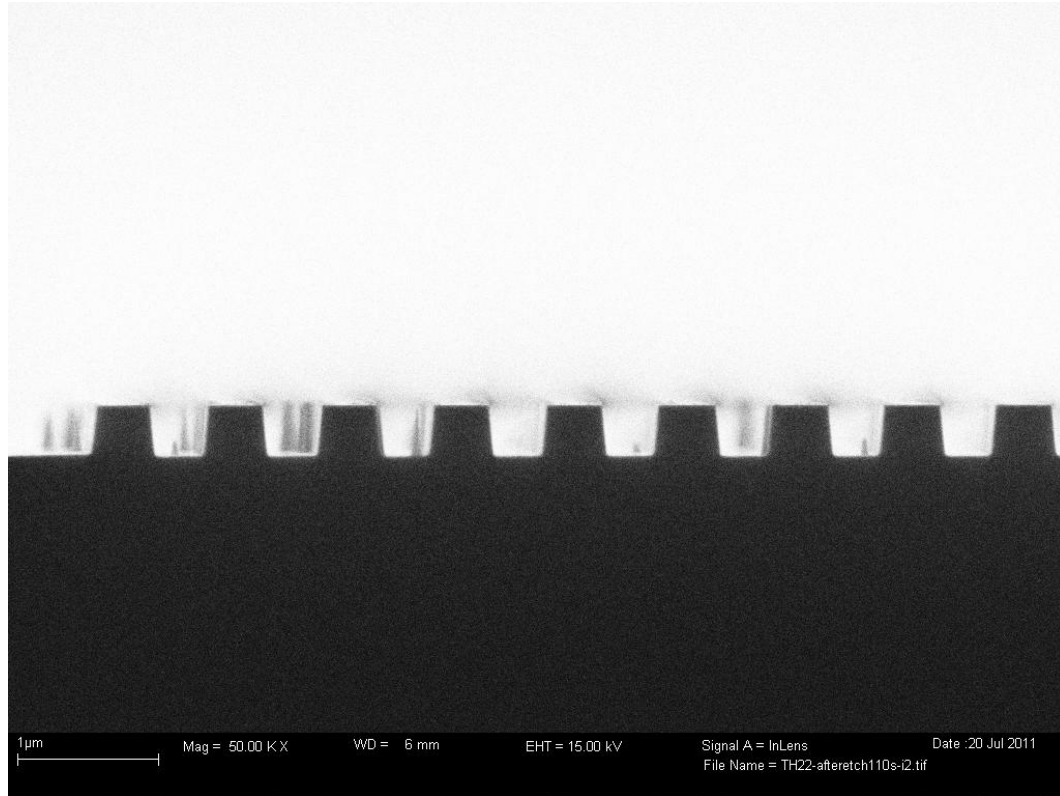


Figure 3.7: SEM picture (profile view) of a cleaved sample TH22, which has the same pattern as the TH68 sample, and was etched together in the multistep etching process.

The device was measured in SEM top view for the line widths. Both the upper and lower line widths are measured (see Figure 3.5 for a sample measurement of the upper line width), and then the average of the two was calculated as a final measurement of the line width. The depth of this same sample was not measured, but another sample which was etched side-by-side was measured. This was done since we could not cleave and measure the actual sample, thus we used another sample etch test grating for that purpose. The results of the measurements of the device are shown in Table 3.4.

Table 3.4: Dimensions of DH5 sample

| | Design goal | Measured dimensions | Fabrication error |
|-------------|-------------|---------------------|-------------------|
| Line width | 280 nm | 268.96 nm | 3.94% |
| Fill factor | 35% | 33.62% | 3.94% |
| Etch depth | 280 nm | 275 nm | 1.79% |

The AR grating was fabricated with a fabrication error of about 4% for the line width and 1.8% for the etch depth. There is some line edge roughness and some roughness on the top surface of the ridge, and a sidewall angle of a few degrees. Besides these fabrication errors, we have fabricated the device according to the design specifications.

3.8 Simulation and Characterization

The simulation and characterization of the devices were performed by other members of our research group. The simulation was done by Ethan Keeler and the optical characterization by Dale Hiscock. The method used for the simulation was Rigorous Coupled-Wave Analysis (RCWA) [52], which is a computational technique for solving electromagnetic equations in a periodic structure.

3.8.1 Device 1 (DH5)

The sample DH5 was used to test the multistep etching process for the first time. Since the etching was successful, and thus the sample device ready for characterization, we decided to characterize this device. The results of the RCWA simulations used to determine the etch depths will also be discussed in this section.

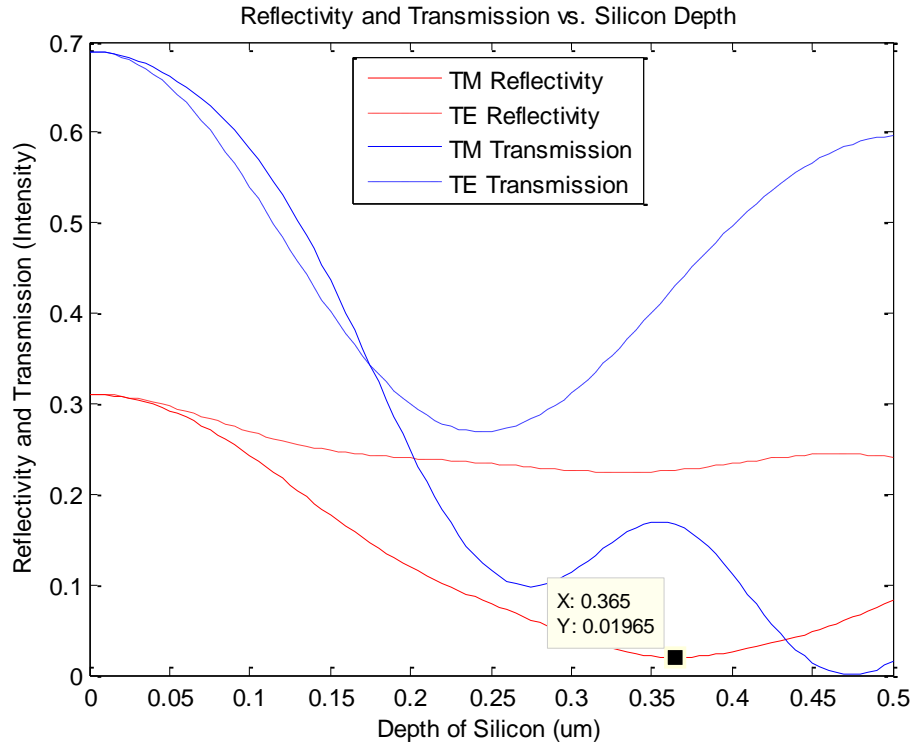


Figure 3.8: RCWA results for a grating of line width 404 nm (800 nm period), showing reflectivity and transmissivity for varying etch depth of the grating. (This modeling work was performed by Ethan Keeler)

The device had three 1-D grating pads with different fill factors. The line width of the aluminum mask was measured in SEM after liftoff (found to be 372, 404 and 432 nm) and the ideal depth needed for minimum reflectivity was found using an RCWA simulation. These line width measurements do not take into account the sidewall slant which changes the line width after etching. The results of the simulation for the grating with 404 nm line width are shown in Figure 3.8.

The grating was designed for minimum reflectivity for the TM polarization, and as can be seen from the red solid line in Fig. 3.6, the reflectivity goes to a minimum of 1.97% intensity for a grating depth of 365 nm. The actual measured etch depth was 354

nm. Note that the Reflectivity and transmissivity do not always add up to unity. This is because the RCWA simulation models the grating with an infinite depth of silicon, and does not take into account power transferred into modes in the silicon substrate.

The device was then optically characterized. Free space reflectivity was measured for all three gratings as well as for a bare silicon surface on the same chip for comparison. The results are shown in Fig. 3.9

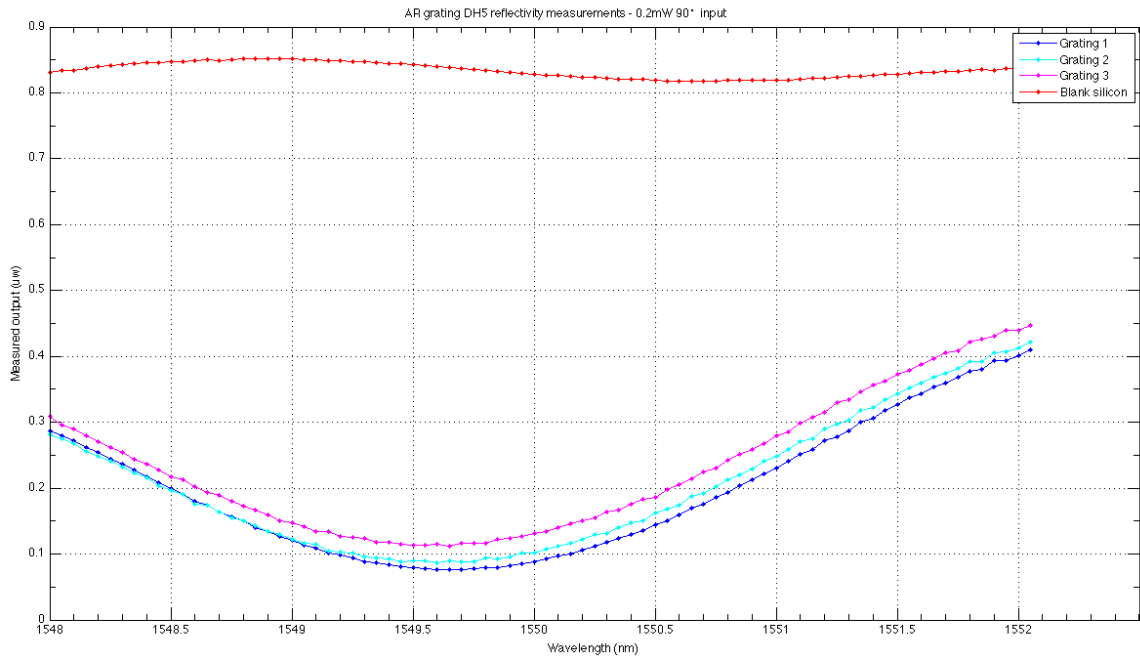


Figure 3.9: Optical characterization results of DH5 sample – measured reflected power plotted vs. wavelength. (This characterization work was performed by Dale Hiscock)
The experimental measurement of the ratio of reflectivity of the AR Grating to bare

Silicon was 9.14%; compared to a RCWA Simulation of 5.39% (values are for the best of the three gratings). Note that this ratio is different from the reflectivity mentioned above, which was the ratio of output power compared to incident power. Although the experimental result was not as good as predicted by the simulations, it still showed a high reduction in reflectivity, by a factor of approximately 10.

3.8.2 Device 2 (TH68)

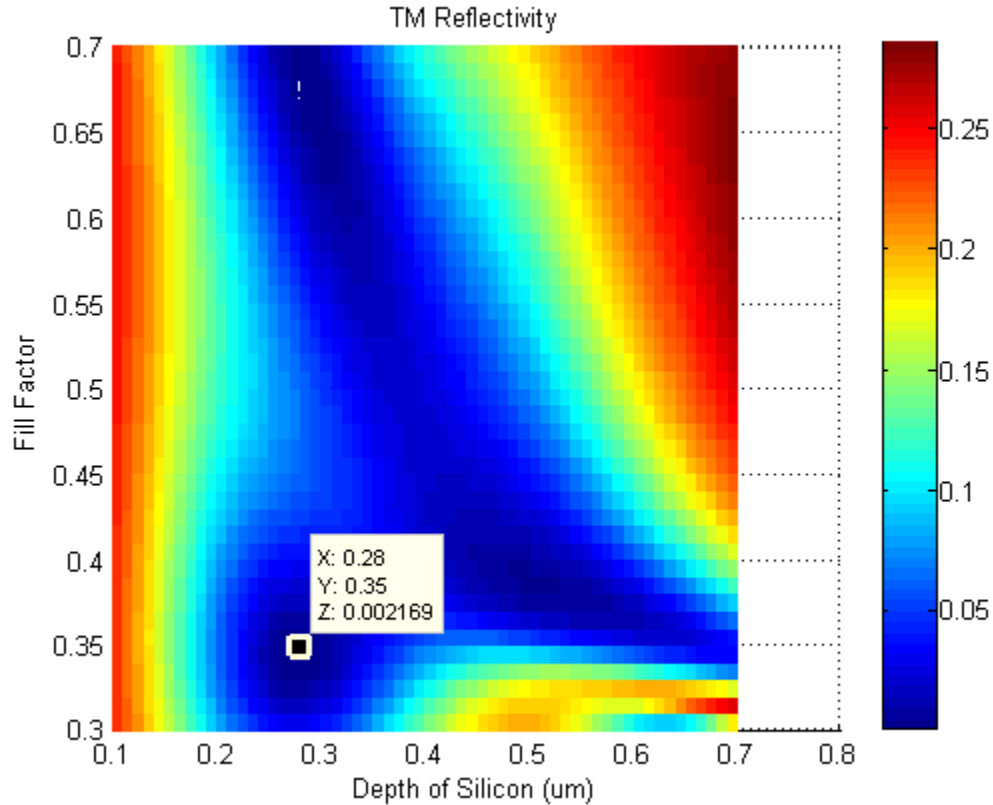


Figure 3.10: Results of RCWA simulation performed to find the design parameters for minimum TM reflectivity for an 800 nm period 1D grating. Fill factor and etch depth of the grating are both varied and the minimum TM reflectivity was found to be 0.217%. (This modeling work was performed by Ethan Keeler)

The second device was designed to have the minimum reflectivity possible in TM with a 1D rectangular grating with 800 nm period. An RCWA simulation was performed varying both the fill factor and the grating depth (see Fig. 3.10).

It suggested a lowest reflectivity of 0.217% for a grating fill factor of 35% and a grating depth of 280 nm. This served as the original design target.

The device was characterized optically and the results shown in Fig. 3.11.

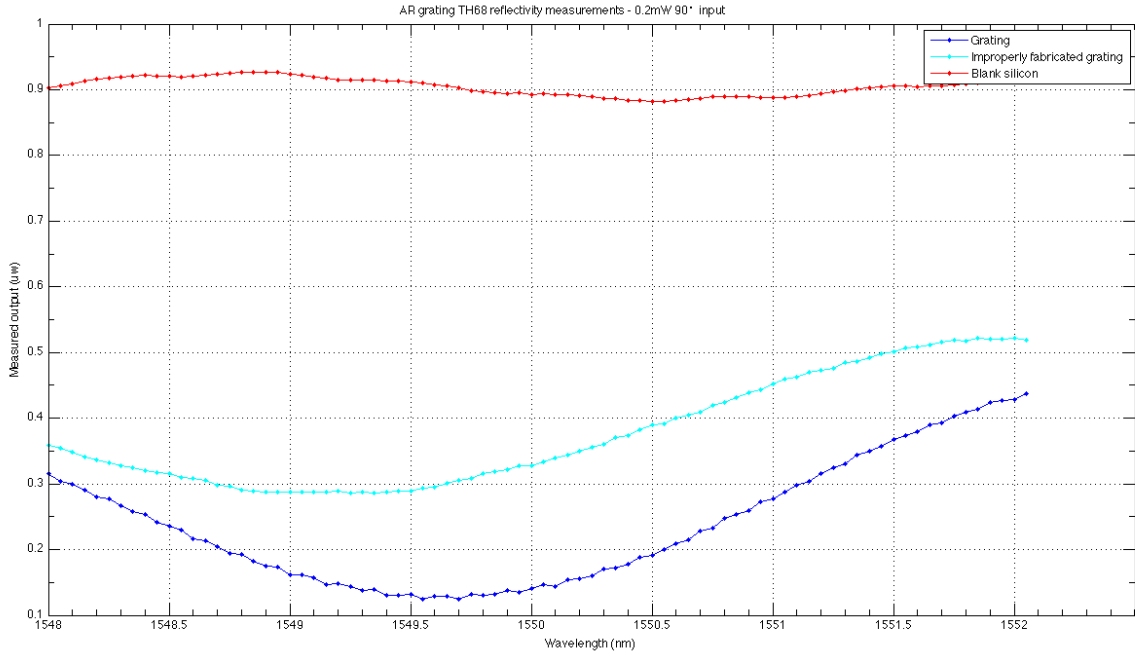


Figure 3.11: Optical characterization results of TH68 sample – measured reflected power plotted vs. wavelength. (This characterization work was performed by Dale Hiscock)

The device did not perform as well as expected, showing a minimum reflectivity ratio (the reflectivity of the grating to the reflectivity of bare silicon) of approximately 14%. This may be due to imperfections in the grating due to fabrication errors, such as slanting sidewalls, edge roughness, etc, which were not taken into account in the simulations.

3.9 Conclusion

We have successfully fabricated a 1-D subwavelength-period rectangular grating which operates as an antireflective structure. The device was characterized, along with another previous sample from the production cycle, and they were both shown to reduce reflectivity by an approximate factor of between 7 and 10. However the reduction was not as high as predicted from RCWA simulations.

We have demonstrated standard fabrication processes such as spinning and liftoff and optimized the ICP-RIE etching process. We have used a bi-layer resist recipe and liftoff process which works for feature sizes down to about 200 nm. We performed a feature size calibration for 1-D gratings in silicon. This calibration enabled us to relate software mask feature size to aluminum hard mask feature size, for line widths in the range of approximate 200–600 nm. Using these data we can approximately predict the software feature size to use for the final required hard mask feature size, thus reducing the number of calibration runs needed in the future to make similar devices. We have tried to optimize the etching process to make the etch rate more stable, by taking into consideration factors such as chamber cleanliness and seasoning. However, although we were able to reduce the variability in the etch rate to some degree, we were unable to reduce it to the required accuracy. Consequently, we found a solution to enable us to achieve precise etching: multi-step etching. This process has been shown to work and can etch to an accuracy of ± 10 nm.

We still have some optimization work to be done. We need to improve the anisotropy of the etching process. Currently our etch recipe produces a less than ideal etch profile, with the sidewalls sloped outwards (see Figs. 3.5 and 3.7). The sidewalls have an average slope of about 6° (with respect to the vertical), which corresponds to anisotropy of 0.895 (a perfectly anisotropic etch with vertical sidewalls would have anisotropy of 1). Increasing anisotropy is possible with this recipe, but it is difficult to get perfectly vertical walls. Several studies have been done analyzing the effects of various recipe parameters [53-55]. Gogolides et al. [53] have shown that by decreasing pressure

and SF_6 gas flow, anisotropy of about .98 can be achieved with this recipe. Our etching recipe already has a much lower $\text{SF}_6:\text{CHF}_3$ ratio than the values used in these studies and we suggest increasing this ratio slightly to improve anisotropy. This will increase horizontal etch rate and, if adjusted properly, could even give a slight undercut profile for the gratings (which is desirable in other devices, see Sec. 4.3.2).

Future work involving process improvements could address a number of factors which would improve our ability to fabricate useful optical nanostructures. One such direction is to decrease line edge roughness after lithography. We will attempt lithography at higher magnifications (currently we use 1000x, we can go to 3000x), and this might decrease line edge roughness due to fluctuations in the electron beam positioning during lithography. We can also try to decrease sample-to-sample feature size variation. One of the reasons for this may be slight variations in the thickness of the PMMA layer. We can try to relate the exact thickness of a sample to the feature size and thus calibrate this effect and attempt to reduce this variation. Finally we can also improve our liftoff process by using a thinner layer of deposited aluminum, which will increase the success rate of the liftoff process.

The optimization of the requisite fabrication processes to date has enabled us to make simple nanostructures with a fair amount of accuracy. In the future we will be able to make gratings and similar structures with feature size of approximately 200-600nm with many fewer trial runs. We can also use these process optimizations to help us make more complicated and smaller structures.

MID INFRARED POLARIZING BEAM SPLITTER

4.1 Introduction

The final device to be discussed in this thesis is the mid-infrared polarizing beam splitter (mid-IR PBS). From a fabrication point of view this device is more complicated and will require all of the fabrication steps outlined in Fig. 1.1. Structurally this device is basically a 1-D grating in silicon with an additional gold layer. To successfully fabricate this device we will need to use all of our skills gained through the previous process optimization work, as well as optimize the gold deposition step, which was not needed for the previous devices.

The mid-IR PBS design was proposed by our collaborator Vincent Paeder [56] from the Swiss Federal Institute of Technology, Lausanne (EPFL). The design consists of a grating on a silicon substrate with a dual layer metal wire grid. The 1D subwavelength grating acts as a form-birefringent structure, or an effective medium with different optical properties for TE and TM polarized light. The gold layers on top of the ridges and in the grooves act as an effective resonant cavity. Properly designed, these two effects are combined to give anisotropic spectral reflectivity [17]. Thus, at 4.36 μm wavelength, the structure will reflect one polarization state and transmit the other. This device will have applications in atmospheric sensing, and the operating wavelength range was chosen so that the device can be integrated with existing systems which our collaborators are already using. The design parameters for the device are shown in Fig. 4.1. Polarizers and PBSs based on subwavelength gratings or wire grid designs exist for different

wavelengths [18-22]. A multilayer PBS has also been demonstrated [23], as well as a double metal wire grid design similar to ours but for visible wavelengths [24], and for very broadband (0.3-5 μm) applications [25].

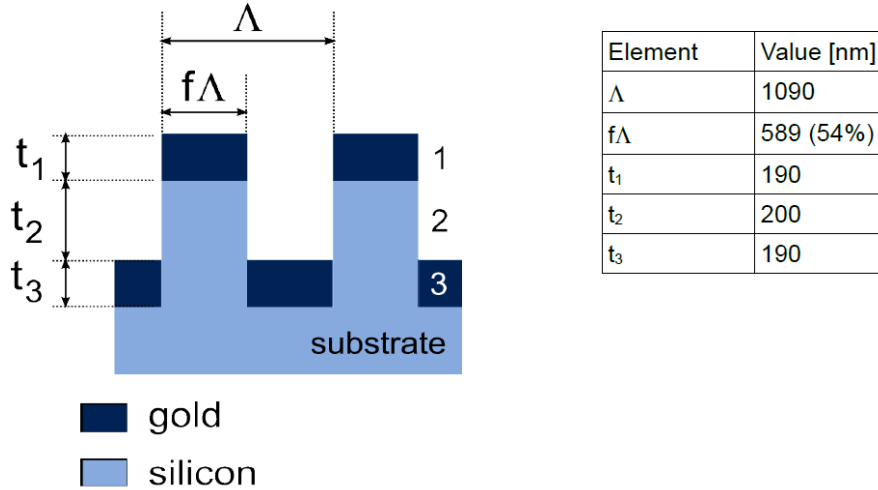


Figure 4.1: Design parameters for the mid-IR PBS [56]

This project is a collaboration with researchers from the Swiss Federal Institute of Technology, Lausanne (EPFL). In addition to the initial proposal, our collaborators have also performed an RCWA simulation of the device and will characterize the device after fabrication.

4.2 Fabrication Steps up to Etching

4.2.1 Field Stitching in Lithography

The device design specifications call for an active area of 1mm x 1mm, since the free space optical characterization setup of our collaborators require this minimum area for measurement. However our lithography system has a maximum write area of 300 μm

square. The write area can be increased by decreasing the magnification during writing, but all of our EBL calibrations have been performed at this magnification and it would require recalibration and many optimization runs if we made this change. Another method to achieving large area lithography is using the Auto-Alignment feature of NPGS. However this feature requires alignment marks in each pattern. Alignment marks cannot be present in the final device for our application, and thus this solution cannot be used.

Another alternative is to make a script to write several 300 μm square pads in an array, making the total area large enough. However this introduces another problem: since our mechanical stage movement is not extremely accurate, there are some alignment errors between each pad.

Table 4.1: Summary of data for stage alignment errors

| | Error in μm |
|--------------------------|------------------------|
| average horizontal error | 3.00 |
| average vertical error | 5.19 |
| total average error | 4.04 |
| Standard deviation | 1.90 |

We did four trials to try to estimate this error by writing 2x2 and 3x3 arrays of grating pads, and we found that usually the mechanical stage would over shoot the given stage movement by a few microns. This error however was random and had a large uncertainty on the order of a few microns. Also since the stage moves several times during the run, the movement errors could add up and potentially introduce large gaps for the last few patterns.

We found that the horizontal movement errors were usually smaller, and the average of all the errors was 4.03 μm . We used 4 μm as the movement compensation, i.e. when writing an array of 300 μm pads, we set the script to move the stage by 296 μm .

4.2.2 Lithography

The method for calibrating the lithography step to obtain the required line width has already been detailed in section 3.2.3. Thus we already knew the dose and software mask feature size needed to produce the required 589 nm line width. Taking into account the etch anisotropy and thus the sidewall angles of $\sim 6^\circ$ of the etched grating, we calculated that a line width of 548 nm would be needed in the aluminum mask to get the correct fill factor in the etched grating.

We decided to fabricate a 1.2 mm x 300 μm grating (sample TH69), so that the grating could be cleaved for cross-section profiling after etching. After lithography the line width was measured to be 547.8 nm (average of 5 readings), almost exactly the expected line width.

4.2.2 Etching and Dimension Measurements

The TH69 sample was etched using a multi step etching process. The etch time calculated using the average etch rate was 117 s, but we decided to be cautious and potentially under etch it by running for 110s in the first round. The second round was etched for 6 s. Two additional etch test samples (TH33, TH36) were etched at the same time and measured for depth. The results are summarized in the table below:

Table 4.2: Etch times and etch depths for multistep etching of mid-IR PBS sample TH69

| | Etch time | TH33 etch depth | TH36 etch depth | TH69 (actual sample) etch depth |
|--------------|-----------|--------------------|--------------------|------------------------------------|
| First round | 110s | 361.3 nm | | |
| Second round | 6s | | 390.1 nm | 388.1 nm |

The actual sample, TH69, was stripped of the Aluminum mask, cleaved and then mounted in the SEM for profile imaging. The line widths at the top and bottom of each ridge were measured and then averaged to get the final average line width. Table 4.3 shows the final device measurements and the calculated fabrication errors. Figs.4.2 and 4.3 show the fabricated device profile and top view respectively. Thus the grating structure without the gold has been fabricated with the correct fill factor and line width (with about 1% error).

Table 4.3: Required and measured dimensions of fabricated TH69 sample along with percentage errors

| Summary: | measured | required | % error |
|-------------------------|----------|----------|---------|
| Etch depth (nm) | 388 | 390 | 0.51% |
| Average line width (nm) | 597 | 589 | 1.36% |
| Sidewall angle (°) | 5.4 | 0 | |
| Period (nm) | 1101 | 1090 | 1.01% |
| Fill Factor (%) | 54.22 | 54.0367 | 0.34% |

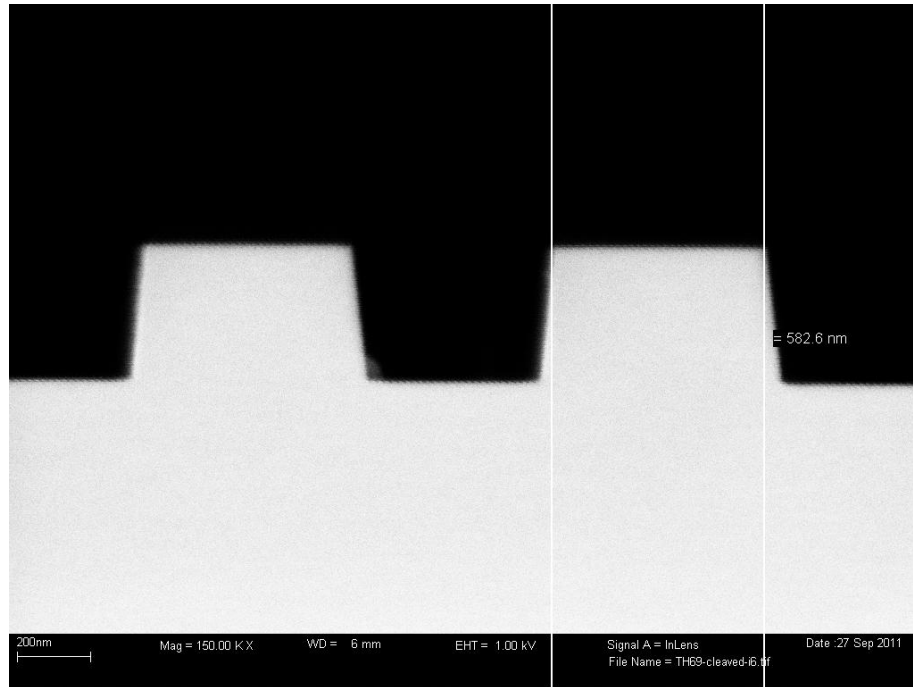


Figure 4.2: Profile view of fabricated TH69 sample. Vertical bars for measuring the upper line width are shown

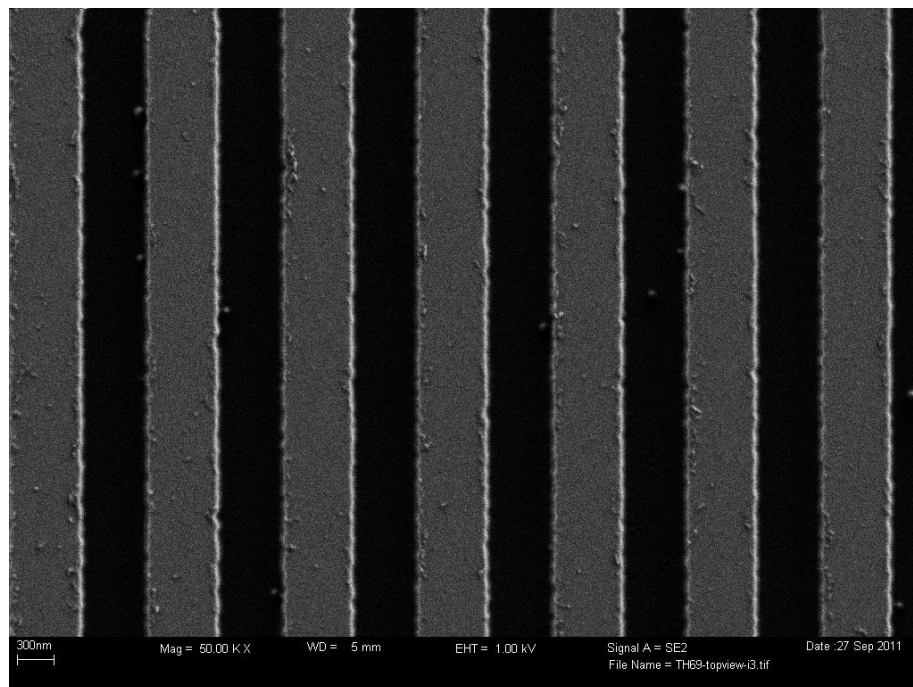


Figure 4.3: Top down view of fabricated TH69 sample

4.3 Gold Deposition

The final step for the fabrication of the device is gold deposition. We use an electron beam evaporator (Amod evaporator from Angstrom Engineering [57]) to deposit thin metal layers such as gold. The gold is held in a graphite crucible and a controlled electron beam is used to heat the metal to the point where it starts to evaporate. The electron beam power can be modulated in real time to control the deposition rate. The deposition is generally directional, smooth and fairly reproducible.

Gold deposition generally requires an adhesion layer, since gold does not adhere well to silicon substrates. We use a chromium adhesion layer of approximately 4nm thickness for this purpose. The chromium is deposited through thermal evaporation from chromium plated rods.

4.3.1 Gold Film Measurements

To deposit 190 nm of gold accurately we needed to make sure that the thickness measurement is calibrated and accurate. The Amod has crystal sensors which can measure the deposited gold layer but they are not accurately calibrated. Thus we performed a few rounds of deposition of gold layers on blank silicon substrates and measured the thickness.

Initially we tried cleaving the gold coated sample and using the SEM to look at a profile view, but it is not possible to measure the thickness of such thin gold layers accurately with this method. To measure it accurately we needed to etch away the gold in some areas on the substrate and then measure the vertical profile using an AFM.

The first step is to perform photolithography on the sample with a mask which has sharp lines or edges. Although the UV lithography aligner (AB-M contact aligner) is designed for wafers and not small chips, we managed to do this since no actual alignment is needed. After lithography and development, areas in the resist were opened up. Next we performed a gold etch using Gold Etchant TFA [58] for 25 s. Then we stripped the remaining resist from the sample. The sample was finally measured in AFM for the gold thickness. The results of the thickness measurements will be discussed in the next section.

4.3.2 Directionality and Thickness Calibration

The directionality of the gold deposition was an issue which needed to be addressed. Our initial trials of gold deposited on a grating showed that there was a significant amount of gold on the sidewalls of the grating (see Fig. 4.4). Even a small amount of gold on the sidewalls of this device may potentially increase the losses in the device. The gold on the sidewalls was deposited because of the physical layout of the deposition chamber in the Amod evaporator. The sample is held upside down above the gold crucible, but not directly above it. Also the sample is typically rotated slowly to get uniform deposition over the surface. The deposition of gold through evaporation in a vacuum is very directional, that is the metal vapor atoms travel in a straight line until they reach the sample, where they accumulate as a film [59].

Thus to obtain directional deposition, we decided to turn off the substrate rotation and mount the sample such that it is perpendicular to the direction of the incoming gold vapor. After measuring the dimensions of the chamber and its setup, we calculated that

the sample had to be mounted at an angle of 22.5° to the horizontal substrate holder. This was achieved by mounting a glass slide with a metal piece underneath and the angle was adjusted to be 22.5° with the horizontal. The actual sample was then mounted with tape on top of the glass slide (see Figure 4.4).

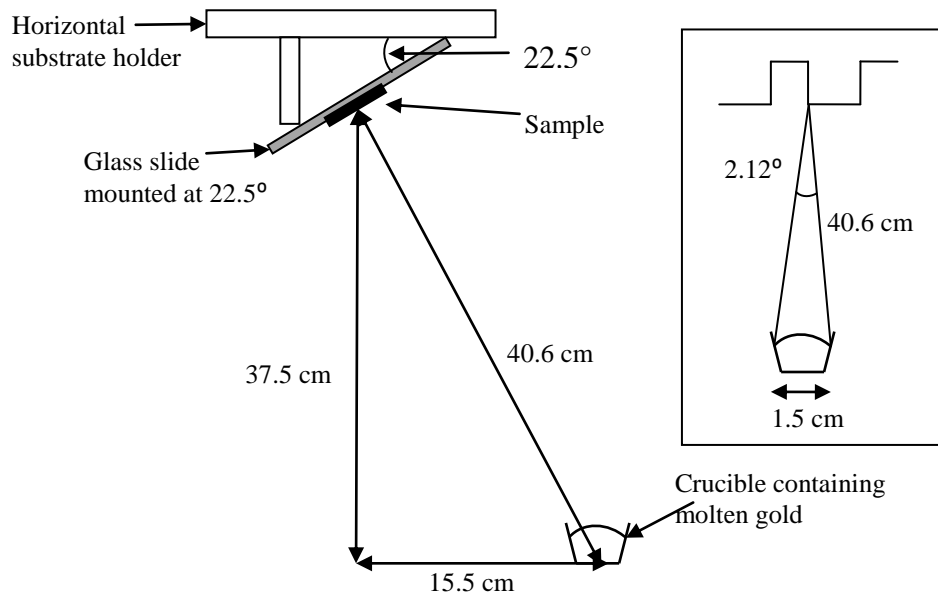


Figure 4.4: Diagram showing orthogonal mounting of sample in the deposition chamber. Dimension measurements in the chamber are also shown. Inset shows the spread of gold vapor due to finite size of the source

It is important to note here that even if the mounting is perfectly orthogonal, there will still be some gold on the sidewalls. This is because the source of the molten gold is not a point source, but is actually a molten pellet with an area of a circle with an approximate diameter of 1.5 cm. Thus gold vapor coming from the edges of the circle will have a slight angular spread when it reaches the sample. We estimate this angular spread to be 2.12° (see Figure 4.4, inset). Thus, to get no gold on the sidewalls, we will

theoretically require a grating with slightly inward sloping sidewalls, or a negative taper, with sidewalls at a 1.06° angle with respect to the vertical.

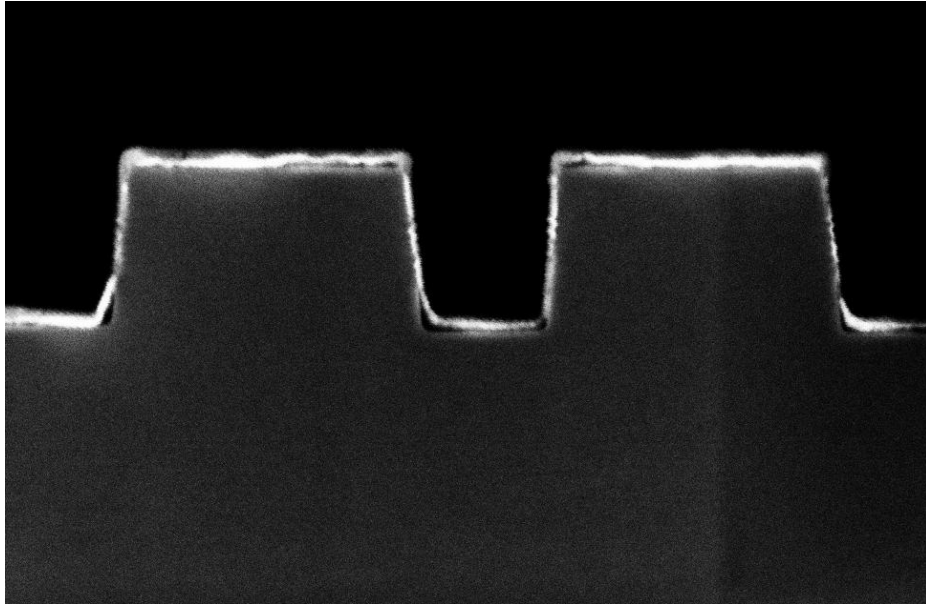


Figure 4.5: Gold deposition without directionality control. The gold layer is brighter compared to the silicon substrate

This method did seem to show a reduction in the amount of gold on the sidewalls (see Figs. 4.6 and 4.7). It is difficult to estimate or measure the amount of gold on the sidewalls, thus difficult to verify the success of this method. From visual inspection of the SEM pictures, there seems to be just small isolated islands of gold on the sidewalls, instead of a layer tens of nanometer thick. Since the sidewalls have a slight slant, a little gold is expected to get deposited on them. To further reduce the amount of gold on the sidewalls, a slight undercut in the etching profile is needed.

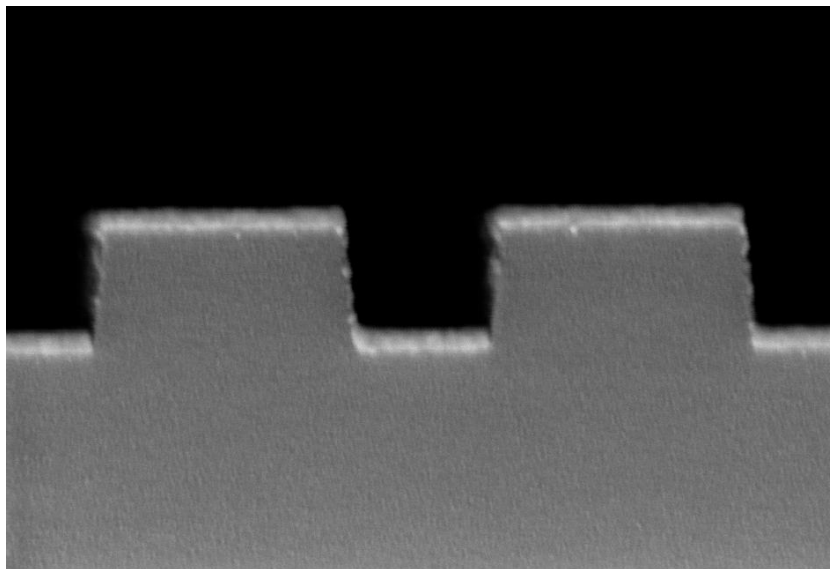


Figure 4.6: First trial of gold deposition with orthogonal mounting of the sample.

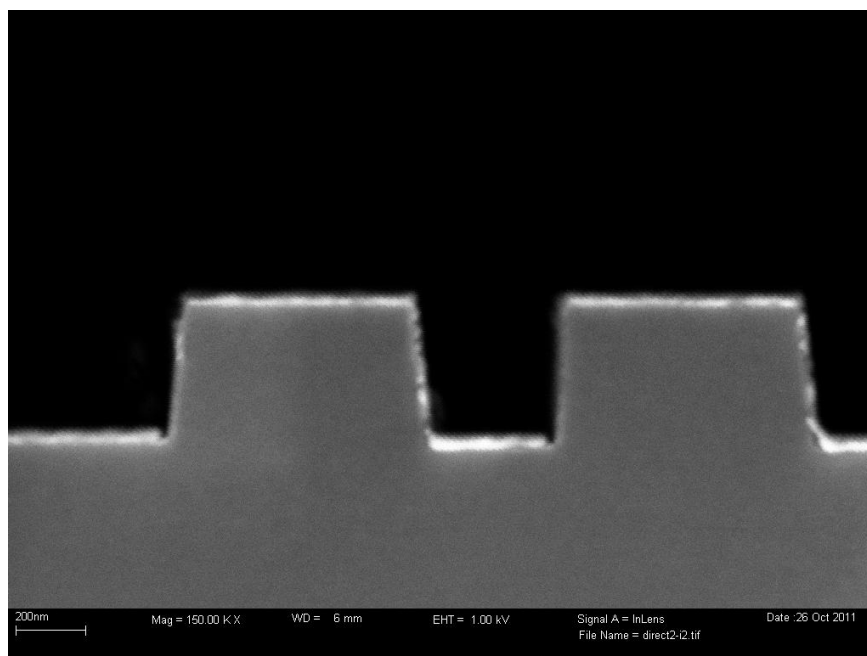


Figure 4.7: Second trial of gold deposition with orthogonal mounting of the sample.

Two trials were done using the orthogonal mounting. The sample from the first trial (Fig. 4.6) had gold deposited after it was cleaved and thus the grating edge was

exposed. The samples shown in Figs. 4.4 and 4.6 were cleaved after gold deposition. This causes the gold layer to appear different in the three pictures.

To calibrate the thickness we did several rounds of gold deposition. We initially tried to deposit 50 nm of gold accurately and then scale it to 190 nm. This was done mainly to save gold costs. The rate and the amount of gold deposited are measured by the crystal monitors, but they have a scaling error which has to be calibrated. We enter the required target thickness in the deposition software, and after deposition we measure the actual thickness of the gold. Initial tests were done without the orthogonal mounting, and thus the calibration data from those tests are not comparable and so are not presented.

The first trial of orthogonal mounting gave a measured gold thickness of 72nm for a 50nm target thickness (as measured by the crystal monitors in the deposition chamber). This large difference was probably mainly due to the fact that the mounting changed the distance from the source to the sample and also due to the orthogonal mounting. In the second trial we tried to deposit 50 nm gold with the scaling factor suggested by the first trial. The results are shown in Table 4.4

Table 4.4: Gold thickness calibration for a target thickness of 50 nm

| | Thickness measured by crystal monitor (nm) | Actual thickness measured by AFM (nm) | Scaling factor |
|--------------------------|---|--|-------------------|
| First directional trial | 50 | 72 | 1.44 |
| Second directional trial | 34.7 | 47 | 1.35 |

These two trials have a similar scaling factor, which suggests that the deposition rate is fairly consistent. We have seen that the deposition rate is stable over many runs from previous trials as well. We have not yet attempted to deposit a layer thickness of

190nm, and it is debatable if the scaling factor will remain constant for a layer 3-4 times thicker. In the future we will try depositing 190 nm gold with this scaling factor and after a few trials, demonstrate the deposition of gold with accuracy and reproducibility.

4.4 Conclusion

We have not yet completed the fabrication of this device. We have, however, made the grating structure without the gold layer, within about 1% of the fabrication tolerances. The grating lithography and etching was done using the process optimization described previously in this thesis. The gold deposition process optimization is not yet complete. We have demonstrated a method to deposit gold directionally and have shown that it reduces gold on the sidewalls, but not completely.

Some work remains to be done before we can fabricate the actual device. A complete calibration of the thickness of the gold deposited is yet to be done, so that we can deposit the desired 190nm thickness accurately. We also need to optimize the etching recipe to achieve a slight undercut or negative taper to reduce the amount of gold on the sidewalls. Once we achieve these process optimizations we can finally fabricate the actual device.

This device incorporates all of the steps in our nanofabrication process, and is structurally more complex and less tolerant to fabrication errors than the other two devices discussed before. Thus fabricating this device will test our skills and abilities in nanofabrication and will require us to further optimize our processes.

CONCLUSION

We have improved our capabilities in nanofabrication, such that we are capable of producing subwavelength scale optical devices for various applications. We have assisted in the fabrication of subwavelength-size Solid Immersion Lenses, specifically in the lithography of PMMA cylinders of specific height and diameter. These nano-SILs were later characterized for shape and finally optically characterized for performance. We have produced 1-D antireflection gratings in silicon, with 800 nm period and line widths of 280 and 400 nm. The devices were characterized and simulated and the principle shown to work, although admittedly not as well as expected. The fabrication of a third device, a mid-infrared polarizing beam splitter, is currently in progress.

In order to realize the devices presented above, we have developed and optimized a number of fabrication processes for Silicon nanostructures with optics applications. We have demonstrated the capability to spin coat precise (± 5 nm thick) layers of PMMA and fabricate a bilayer PMMA which can be used for liftoff. The liftoff process has been shown to work for feature sizes down to approximately 250 nm. We have used electron beam lithography (EBL) to make cylinders of PMMA of precise diameters in the range of 450–600 nm. We have also calibrated EBL for 1-D gratings, and demonstrated line widths precise to within ± 10 nm of expected values. We have also carried out some trials of dose versus line width, which can aid in estimating the required dose for lines in the range of about 250–600 nm width. We have improved our ICP etching process, and tried to stabilize the etch rate by paying attention to wafer cleaning, chamber cleaning and chamber seasoning. However, we could not stabilize the etch rate to within our

requirements. To solve this issue we instituted a multistep etching process which we have demonstrated to work, and now we have the capability to etch accurately to within ± 10 nm depth. We have demonstrated a method which improves the directionality of gold deposition. This results in less gold on the sidewalls when depositing gold on a multi-level nanostructure (such as a grating).

Process optimization and control is a continuous process and we will continually improve them. We have suggested changes to the etching recipe which will increase etching anisotropy or achieve a slight undercut. We have discussed possible reasons for and ways to decrease line edge roughness and sample-to-sample variation in feature size due to lithography. Other future work may include depositing thinner aluminum layers for liftoff, and depositing smoother gold layers.

We can fabricate simple optical structures in size scale of 250-600 nm within reasonable fabrication tolerances. In the future when we make similar structures we can do so with much less process optimization, thus making it much easier and faster to make those devices. Also we can move on to more complicated or smaller scale structures, building on our present capabilities. A lot of potential extensions of our work exist. The nano-SILs did not perform as well as expected due to the non-ideal shape, and we can try producing nano-SILs of different dimensions which might perform better. AR gratings can be optimized for polarization independence and we can actually fabricate AR gratings integrated with other optical or MEMS devices. We can scale down the design of the PBS for shorter wavelengths. We can apply subwavelength scale nanostructures for other applications: gratings for coupling light into waveguides, form birefringent

structures for sensing applications, polarization selective resonant structures in waveguides, nanostructured gold surfaces for plasmonic sensing, etc. Finally, in the long term, we will also find interdisciplinary applications for nanostructure-based optical device, explore potential avenues for integration of these devices with other areas of optics, and use all these capabilities to find solutions to real world challenges in optics.

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