A data acquisition and recording system
by John Emil Somppi

A thesis submitted in partial fulfillment of the requirements for the degree of MASTER OF SCIENCE in Electrical Engineering
Montana State University
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Abstract:
When a program controlled data acquisition and recording system is desired, several important areas beyond a central processing unit, memory, and input/output must be considered. Specifically, these are: system control, interfacing of data, monitoring transducers and mass data storage. In this theses, designs for these additional features are presented. They are designed to complete one such data acquisition and recording system centered around the central processing unit, memory and input/output on an existing microcomputing system.

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Date May 20, 1977

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ABSTRACT

When a program controlled data acquisition and recording system is desired, several important areas beyond a central processing unit, memory, and input/output must be considered. Specifically, these are: system control, interfacing of data, monitoring transducers and mass data storage. In this theses, designs for these additional features are presented. They are designed to complete one such data acquisition and recording system centered around the central processing unit, memory and input/output on an existing microcomputing system.

CHAPTER 1

INTRODUCTION

In the field of real time data acquisition, there are systems which cannot be monitored by conventional means. Either they are too complex or too dynamic for data to be adequately compiled by human observation. A logical alternative then is to automate the data acquisition process.

To fulfill this problem the Electronics Research Laboratory of Montana State University was approached by the United States Forest Service and asked to build an automatic data acquisition system to fit the following specifications:

1. The system must be able to monitor and store data while operating with little human interaction.
2. The system must have some intelligent decision making capability for real time data evaluation.
3. It should be able to monitor moderately high speed systems. (Data rates up to 3 K Hz.)
4. It should be versatile enough to effectively monitor various data acquisition situations.
5. It should be small in size to allow ease in portability.
6. Power consumption should be low, as it would be battery powered
7. It should be rugged enough to withstand an outdoor operating environment.

To meet these criteria, we engineered and built a microcomputer based data acquisition system. Its computer-like operation and architecture made it a natural to fit the operational and system specifications. The electrical and mechanical design of the system using low power electronics and small, sturdy, modular construction fulfilled the criterion.

CHAPTER 2

SYSTEM OPERATION

In the data acquisition process it was desired to have the system do all the data monitoring and data accumulation with a minimum of human intervention. As a result, the operation of the data acquisition system centers around the programmable microcomputer. It is this microcomputer which monitors and processes the data from its various sensors (or transducers). It retains as accumulated data pertinent information it has monitored. This information can later be retreived for detailed evaluation. This process is controlled by a system program executed by the microcomputer. This operation of the microcomputer in turn is under complete operator control.

In a typical situation, the operator initiates microcomputer operation by loading the operating program into the microcomputer from the mass storage medium. This storage medium is the permanent storage area where operating programs as well as retained monitored data is kept for permanent continual or future referral. With the execution of this controlling program, the operation of the data acquisition begins. The operator may interact with the system either in supplying necessary parameters for operation or by examining monitored data if desired. However, the data acquisition is primarily controlled by the operating program.

As data is being accumulated, minor analysis may be done, but primarily pertinent data is being accumulated in the mass storage medium.

Here it remains for later referral. When detailed examination and analysis of this data is desired it is transferred from the mass storage area to larger computing facilities for evaluation.

The primary task for this system is data acquisition. In-depth analysis of the data is left to larger computing systems more specifically suited to that task.

CHAPTER 3

SYSTEM ARCHITECTURE

The architecture of the Data Acquisition and Recording System (DARS) is modular in concept. Fundamental functions in the operation of DARS are done by separate units. These units then interact to perform the complete data acquisition process. With the general system operation distributed between these subsystems, no particular portion of the system is overtaxed and a high degree of versatility is maintained.

A diagram of DARS is shown in Figure 1. There are four subsystems comprising the system The primary one of these is the microcomputer system. It is the intellect of the system. It contains and executes the controlling program governing DARS operation. The microcomputer system is also the decision making portion of the system. It is the heart of DARS as it enables and directs the operation of the monitoring and data accumulating operations.

Working closely with the microcomputer system is the Front Panel Unit (FPU), which is used for system control. This is the system which controls the microcomputer system operation. It is the primary interface between the operator and the data acquisition system. System operation can be initiated, terminated, monitored or modified by operator action with this unit.

The Data Acquisition System (DAS) is the portion of the DARS through which all monitoring of data is done. It is the interface between the data being monitored and the microcomputer. The purpose of

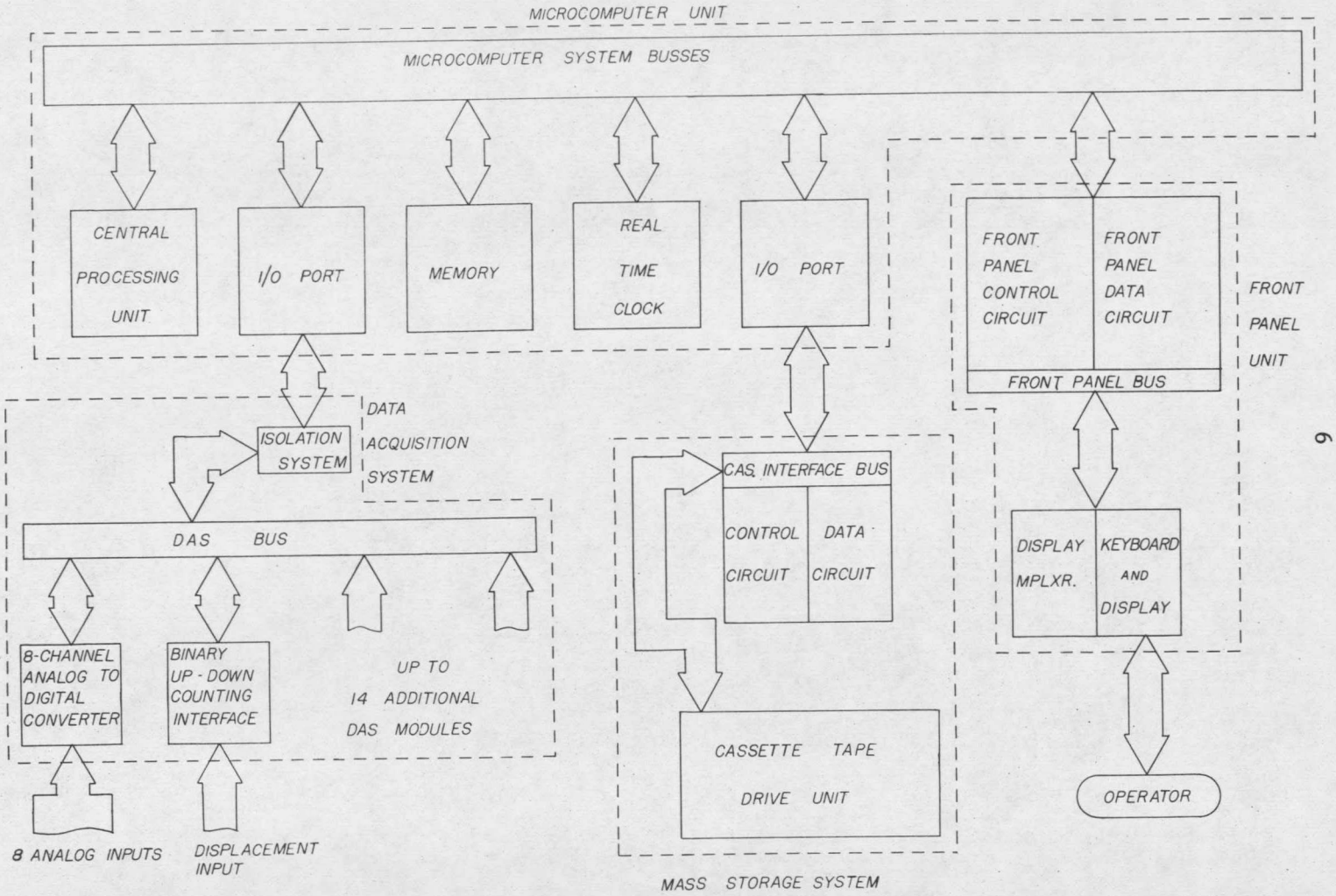


FIGURE 1: DARS SYSTEM ARCHITECTURE

of this system is to change the form of the monitored data into a meaningful representation understood by the microcomputer.

The final subsystem of DARS is the mass storage medium. This system is used for semipermanent information storage. Operating under microcomputer control information may either be stored on or retrieved from this unit. This information may be the data monitored by DARS being retained for later use or an actual program used to control the microcomputer system. Using this type of system the entire operation of DARS becomes independent and self-contained.

CHAPTER 4

MICROCOMPUTER UNIT

The microcomputer unit is responsible for complete operation of the system. It is a basic low-power microcomputer with processor, memory, and input/output capablity. This system was designed by Darrell B. Irvin (1).

MICROCOMPUTER ARCHITECTURE

The architecture of the microcomputer is a bus structured system consisting of four major sections. These sections are the Central Processing Unit (CPU), Memory, Input/Output ports (I/O) and a Real Time Clock (RTC). These are all connected by the system busses. These busses are the Data Bus (D Bus), the Address Bus (HL Bus) and a Control Bus.

MICROCOMPUTER OPERATION

The Central Processing Unit controls the operation of the Microcomputer system. It performs all the arithmetic and logical operations as well as controls program execution when in operation. It interacts with the three other supporting microcomputer sections through the bus systems. The CPU fetches program instructions as well as stores and retrieves data from the Memory section of the Microcomputer. It is able to interact with devices external to the Microcomputer system, such as the Mass Storage Unit or the Data Acquisition System, through the Input/Output ports. I/O is the link between the CPU and the external systems.

The Real Time Clock aids the system by enabling the monitoring of time as well as data. Measuring the passage of time is necessary in acquisition, but it is extremely difficult to do accurately with only the CPU. The RTC accurately measures time under control of the CPU.

THE CENTRAL PROCESSING UNIT

The power of the CPU lies with an Intel 8ØØ8 Microprocessor. The 8ØØ8 is an eight bit parallel microprocessor. It can address up to 16 kilobytes (16K bytes, one K byte is 1Ø24 bytes) of memory and has complete I/O capability. It may operate with external interrupts using a vectored interrupt scheme. It is a moderate speed microprocessor well suited to moderately high speed data acquisition.

Instruction Format

The processor instructions are in the multibyte format. Instruction size varies from one to three bytes depending on the instruction. One memory cycle is used to fetch each byte from memory. The time of each cycle also varies depending upon the complexity of the instruction being executed.

Single cycle instructions include non-memory reference operations. These instructions need no additional data other than the instruction for exection. Two and three cycle instructions are memory reference instructions and I/O instructions. The memory reference instructions are two cycles if an 8 bit data byte is needed. They might be three cycles is a 16 bit two byte address is required. One 8 bit byte is

retrieved each memory cycle. The first cycle is referred to as the Instruction Cycle since the instruction is fetched during this time. The second and third cycles are termed Data Cycles since data is fetched at this time. All I/O instructions are 2 cycle with data input from or output to the I/O port in the second cycle or the I/O Cycle.

Timing and Control

Any instruction contains from 3 to 5 separate state times per memory cycle. The first two states are always the outputting of the low and high order bits respectively of the program counter from the microprocessor to memory. The third state is the fetch phase, where the contents of memory at the address indicated by the program counter are sent to the CPU. The fourth and fifth times are optional, depending upon the instruction being executed. The instruction is executed following the fetching of the memory information of the final memory or I/O cycle. These five states' times are referred to a T1, T2, T3, T4, and T5 respectively.

In addition to these five states, there are three more states: T1I, STOP and WAIT. T1I has the same function as T1 except it indicates that the processor is responding to an interrupt request. STOP indicates that the CPU is not executing any instructions; it has been halted. WAIT indicates the processor is waiting between T2 and T3 for a slow device or memory to furnish the data being fetched.

Besides these eight timing signals, there are other control signals

generated or monitored by the CPU. These control signals which are of interest to DARS operation are shown in Table 1 with their functions. The Control bus contains all state time and CPU control signals.

TABLE 1

CPU CONTROL SIGNAL DESCRIPTION

CPU CONTROL SIGNAL	FUNCTION
CLR	Initializes and resets all bus connected units
I/O	Indicates and input or output processor cycle
DATA	Indicates a data fetch from memory processor cycle
INST	Indicates an instruction fetch from memory processor cycle
DSTB	Portion of any timing state when bus data is transferred
DRST	Signal to reset data transmission circuitry following DSTB in T3
INT	Interrupt request to the CPU
PRIOUT	Priority Out signal enabling an interrpt request may be made if necessary
PRST	Priority Reset signal enabling PRIOUT
$\overline{\text{DMA}}$	Acts to disconnect the memory address register on the CPU from the H-L Bus

Bus Structure

The 8ØØ8 has one 8 bit parrallel data port through which the Data and Address Busses are multiplexed. It is a bidirectional port through

which all addresses, instructions and data pass.

The Address Bus or HL Bus is a 14 bit unidirectional bus. It is comprised of two smaller busses, the H Bus and the L Bus, six bits and eight bits wide respectively. The H Bus contains the six high order address bits output to memory during a fetch cycle. The L Bus contains the eight lower order address bits during a fetch cycle. Also, during an I/O cycle data output from the processor is output on the L Bus. By concatinating the H and L Busses the full 14 bit address to memory is formed.

The Data Bus or the D Bus is an eight bit bidirectional bus to the processor. All data input to the processor is done on the D Bus. This data may be either instructions or data bytes from Memory, I/O Ports or the RTC.

In the case of the D and HL Busses, the data sense on each bus is positive. (For further explanation of level and data senses see Appendix I). When the D and HL Busses are not in use, however, they will be at a true or high level. When valid data is on any bus it will be in the upright form or positive true sense.

MEMORY SYSTEM

The memory system for DARS consists of a maximum of 16K addressable bytes of data. The upper 2K bytes, address locations of 38ØØ' through 3FFF', (the suffix " ' " denotes base 16 or hexidecimal notation), are Read Only Memory (ROM). Here special tables and permanent programs may

be stored. The remaining lower 14 bytes is Random Access Memory (RAM). This area is used for temporary data and program storage.

INPUT/OUTPUT SYSTEM

The scheme used in the microprocessor unit for data transfer to and from the CPU centers around the Input/Output Port. The I/O Port is designed for bidirectional data transfer between the microcomputer processor and the I/O device with additional device control and operation monitoring capability. This enables the processor not only to exercise data interaction with the I/O device but also control and monitor the device's operations. The I/O Port is not limited to interacting with a single device however, as it will be shown in the Data Acquisition System that multiple input and output devices can be serviced through a single port.

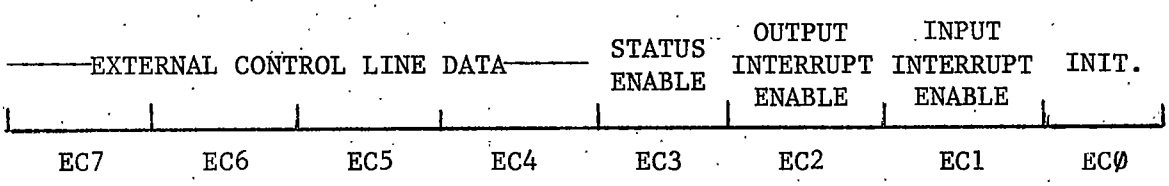
The input, output, control and status monitoring sections of an I/O Port are completely seaparate. Each function may be exercised separately without affecting the other functions. Inputting and outputting of data is done on a single byte basis. Data is transferrred a byte at a time. Due to the separate nature of input and output portions, however, byte outputting may be done simultaneously. Control and status monitoring is done by Externals Control and External Sense lines respectively between the port and the device.

I/O Port Archetecture

The input, output and control sections of the I/O Port have

individual unique addresses which are different from any other port section. In this manner each can be accessed independently by the processor. The architecture of the I/O Port reflects this. These are the major sections of an I/O Port, the input section, output section and control section.

The control section directs operation of both the I/O port and the I/O device. Its center is a control data register which contains a data byte output by the processor to the port. One half (or four bits) of this control byte is used for controlling port operation while the other half is used for the External Control line information. These External Control lines direct the operation of the I/O device. Figure 2 shows the format of the control data byte.



CONTROL BYTE FORMAT

FIGURE 2

In a similar manner, the output section of an I/O port utilizes a output data register. This register contains the data byte output from the processor. Here the data byte is stored for access by the I/O device. Two additional communication lines are used in the output section to facilitate the data transfer. One is the Output Ready line (OUTRDY). OUTRDY indicates to the device that data output from the processor is